Instability Issue of Paralleled Dies in an SiC Power Module in Solid-State Circuit Breaker Applications

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***Abstract*—Paralleled dies in a power module could have instability issues during high current switching transients. The instability is caused by the differential-mode oscillation among paralleled MOSFETs. Conventional analyses of paralleled MOSFETs' stability are normally limited to a single operating point, which ignores the influences of the switching trajectory and nonlinear device parameters on stability. This article reveals that the switching trajectory can significantly influence parallel stability. The analysis is improved by solving eigenvalues of state-space modeling system matrices of all operating points that the switching trajectory goes through considering nonlinear device parameters. Higher voltage and current stresses result in greater real parts of complex eigenvalues, which explains why the paralleled MOSFETs are more unstable with higher voltage and current stresses. To improve stability in solid-state circuit breaker applications, we propose a method to manipulate the switching trajectory to avoid the unstable region where the conventional hard switching trajectory normally goes through. Experimental results show that the turn-OFF current capability can be increased from ∼five times of rated current with the gate oscillation using the conventional turn-OFF trajectory to ∼ten times of rated current without the gate oscillation using the optimal turn-OFF trajectory.**

***Index Terms*—Parallelled MOSFETs, paralleling stability, SiC MOSFETs, and solid-state circuit breaker.**

I. Introduction

In HIGH power applications, high current rating switching devices are required for power converters and solid-state protection equipment [1]. The high current carrying capability requires more paralleled discrete switches or more paralleled dies in one power module due to limited current ratings per discrete switch or die. Paralleling switches bring challenges, including unbalance current sharing and instability issues. This article mainly focuses on the paralleling instability issue of power MOSFETs.

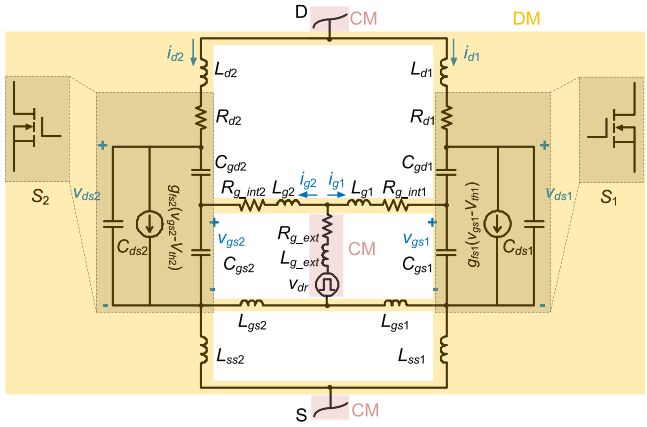

Fig. 1. Paralleled MOSFETs equivalent circuit.

Paralleled MOSFETs instability has been found by researchers since the 1980s. In [2], the authors proved that the paralleled MOSFETs equivalent circuit can be unstable with a divergent natural response to differential-mode (DM) signals. Fig. 1 shows an equivalent circuit of paralleled MOSFETs. DM signals can be any voltage and current differences among paralleled MOSFETs. For example, they can be the uneven current distribution generated by parameter mismatches between paralleled MOSFETs [3]–[5]. These DM signals can excite the oscillation of the paralleled MOSFETs if the natural response of the circuit is divergent. By applying the Routh Hurwitz criterion, whether the circuit response is divergent or convergent can be determined. Equivalent methods have also been used for stability analysis, including the Bode plot and Nyquist criterion in [6] and [7], Colpitts oscillator theory in [8], and state-space modeling in [9].

The key issue of previous analyses is that they mainly focus on a single operating point. However, during the switching transient, the operating point keeps changing with the switching trajectory. Therefore, with different switching trajectories, the parallel stability analysis results of the switching transient can be quite different.

Another issue, which is also difficult to be explained with previous analyses focusing on a single operating point, is that the paralleled MOSFETs instability happens more likely under

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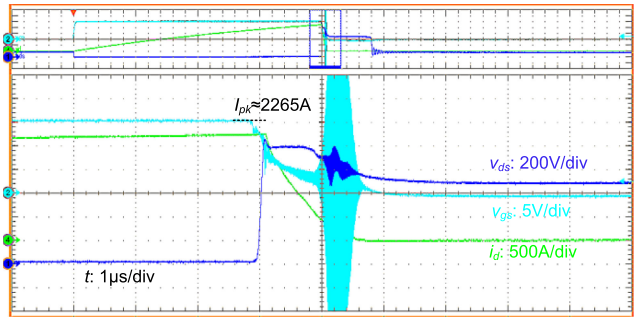

Fig. 2. Parasitic oscillation of paralleling dies in power module during turn-OFF at high current levels.

higher voltage and current conditions. As an example, in Fig. 2, the SiC power module HT3220 [10] has a severe gate oscillation when the turn-OFF current level reaches around 2265 A during short-circuit protection. However, it can successfully turn OFF a fault current lower than this value. The power module is used with 250-A rated current at 60 °C ambient temperature, and the short-circuit protection current is defined as 2250 A (nine times of the rated current). Such a high protection current is normal in solid-state circuit breaker (SSCB) applications [11]–[13]. The turn-OFF gate resistance R_{g_ext} is selected as 5.5 Ω to reduce the turn-OFF overvoltage. In [14], similar oscillation and failure have been noticed for paralleled discrete SiC MOSFETs. Moreover, the authors found that failure is more likely to happen at a higher voltage. In their case, the MOSFETs fail at 750-V bus voltage while they can successfully turn OFF a similar current level with bus voltage less than 750 V.

To avoid MOSFET paralleling instability, two common solutions include increasing DM gate resistances (R_{g_int1} and R_{g_int2} in Fig. 1) [2], [6], [7], [14] and using ferrite beads at the gate of every single MOSFET to help eliminate the parasitic oscillation [15]. However, both solutions require modifying the circuit structure or parameter inside the power module, which is impractical for most users. Therefore, it is important to explore a method to minimize the instability by only changing circuits or parameters outside the power module.

The research objectives of this article are to first analyze the stability during the whole switching transient and investigate the influence factors, including the switching trajectory, and voltage and current stresses; second, explore a method to improve the power module stability by changing only the external circuits in SSCB applications.

The remainder of this article is organized as follows. Section II analyzes the stability of paralleled MOSFETs and discusses the influence of the voltage and current levels on the stability considering nonlinear device parameters influences, especially the transconductance of SiC MOSFETs with the channel length modulation. Section III analyzes the switching trajectory influence on paralleled MOSFETs stability and addresses the challenges brought by the instability during short-circuit protection. Then, in Section IV, we propose a method to improve the stability of the paralleled MOSFETs during short-circuit protection in SSCB applications. Section V introduces a nondestructive test to obtain the oscillation turn-OFF current threshold of the power module. In Section VI, experimental tests are conducted to validate the analysis and proposed solution. Finally, Section VII concludes this article.

II. Paralleled MOSFETs Stability Analysis

Among the stability analysis methods, the state-space modeling can provide a complete overview of the system oscillatory modes and damping factors by the eigenvalues [9], [16], [17]. Therefore, it is applied in this article to analyze the paralleled MOSFETs stability.

A. State-Space Modeling for Paralleled MOSFETs Stability Analysis

State-space modeling is applied to determine the system stability at different operating points. The eigenvalues of the system matrix, which are the same as the system characteristic polynomial roots, can reflect the response of the system. Computer-aided analysis can be used to calculate and visualize the real parts of eigenvalues at different voltage and current levels.

The general state-space model of the circuit can be written as

$$\dot{\vec{x}} = A \cdot \vec{x} \tag{1}$$

where $\vec{x}$ and $\dot{\vec{x}}$ is the state-space vector of the circuit and its derivative, respectively. A is the system matrix, which can be either manually derived or automatically generated with MATLAB and PLECS [18]. The eigenvalues λ of the system matrix A can be solved by the following equivalent:

$$|A - \lambda \cdot I| = 0. \tag{2}$$

Each single eigenvalue λ_i corresponds to a particular solution of the state-space variable. The solutions can be expressed as

$$\vec{x}_i = [K_{i1},\ K_{i2},\ K_{i3}, \ldots, K_{in}]^T \cdot e^{\lambda_i t} \tag{3}$$

where n is the number of state variables and K_{in} is the coefficient determined by initial values of state-space variables.

Complex eigenvalues can be decoupled into the real part α and the imaginary part β. Based on the Euler rule, the solution without the coefficient can be expressed as

$$\begin{aligned} e^{\lambda t} &= e^{(\alpha + i\cdot\beta)\cdot t} = e^{\alpha\cdot t}\, e^{i\cdot\beta\cdot t} \\ &= e^{\alpha\cdot t} \cdot (\cos(\beta \cdot t) + i \cdot \sin(\beta \cdot t)). \end{aligned} \tag{4}$$

The factor $e^{\alpha\cdot t}$ determines the envelope of the circuit response. For α less than zero, the circuit response is convergent, as shown in Fig. 3(a). The more negative the α value, the faster the convergence speed. For α greater than zero, the circuit response is divergent, as shown in Fig. 3(b). The greater the α value, the faster the divergence speed.

B. Nonlinear Transconductance and Capacitances Considered in Modeling

The nonlinearity of transconductance g_{fs} and capacitances C_{gs}, C_{gd}, and C_{ds} of the device is considered to solve the

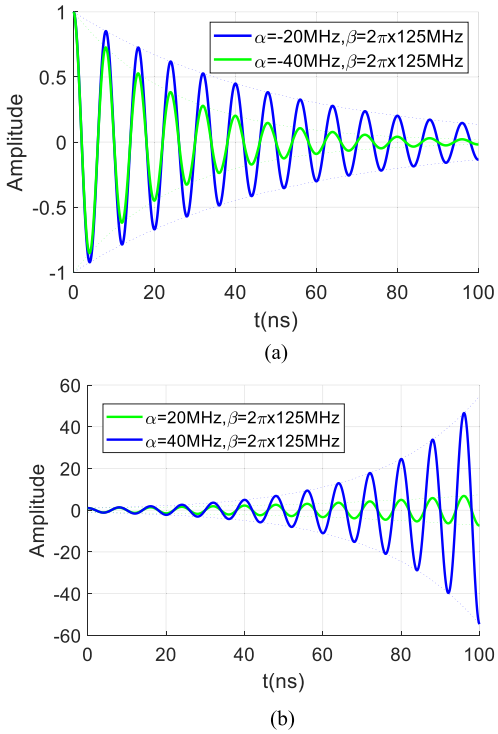

Fig. 3. Influence of eigenvalue real part on system stability. (a) Negative real part: convergent. (b) Positive real part: divergent.

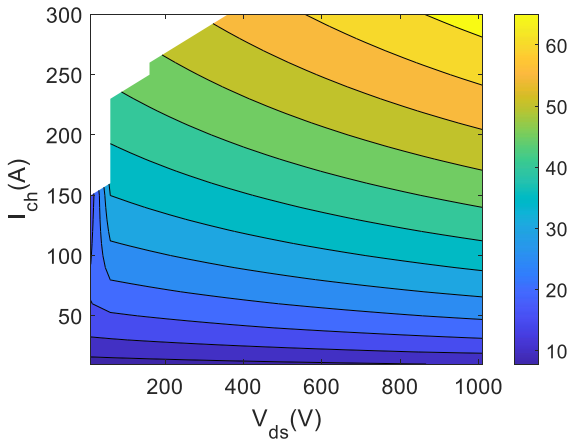

Fig. 4. Nonlinear transconductance under different V_{ds} and I_{ch} conditions.

system matrix eigenvalues under different voltage and current conditions.

The power module HT3220 contains ten SiC dies CPM2-1200-0025B (1.2 kV, 25 mΩ) [10]. The transconductance is characterized by the official SPICE model of the die [19]. Fig. 4 shows the small-signal nonlinear transconductance g_{fs} ($= \partial i_{ch}/\partial v_{gs}$) under different V_{ds} and I_{ch} conditions. Transconductance increases with the drain-source voltage and channel current. For SiC MOSFETs, the channel length modulation is more obvious to make transconductance increase with V_{ds}. Nonlinear capacitances C_{gs}, C_{gd}, and C_{ds} are also considered, and the relationship with V_{gs} and V_{ds} can be found in [20].

Fig. 5. Common source power module HT3220 disassembly.

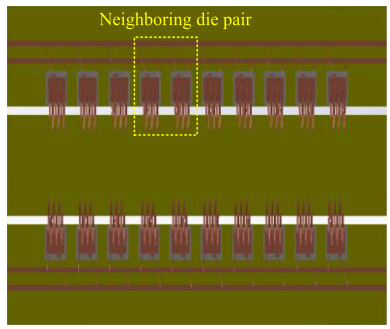

Fig. 6. Top view of the 3-D model of the common source power module.

TABLE I
EXTRACTED PARASITIC INDUCTANCES OF NEIGHBORING DIE PAIR

Inductance	L_g	L_d	$L_{gs}\|\|L_{ss}$
Value (nH)	4.13	0.32	0.83

C. Parasitic Extraction of the Power Module

The parasitic inductances of the power module are extracted with the 3-D model generated based on SiC dies layout inside the power module. The common source power module HT3220 is disassembled, as shown in Fig. 5. The 3-D model of the highlighted part of the power module in Fig. 5 is generated by SolidWorks and given in Fig. 6. The DM parasitic between neighboring die pair is extracted by ANSYS Q3D and listed in Table I. The total internal gate resistance R_{g_int} of each die is 2.1 Ω. Note that the DM parasitic inductances are between two dies. As an example, the relationship between L_g in Table I and L_{g1} and L_{g2} in Fig. 1 is that $L_g = L_{g1} = L_{g2}$. The CM part, e.g., the external parasitic L_{g_ext}, is ignored for the analysis owing to the half-circuit assumption, which has been justified in [2] and [9].

D. Solutions Under Various Operating Points and Discussion

The paralleled circuit can also be simplified from Fig. 1 to be the DM circuit in Fig. 7 with the half-circuit assumption because the DM signals are dominant in the oscillation [2]. The assumption of the half-circuit approximation is the symmetry of Fig. 1. Note that the approximation is to reduce the order of

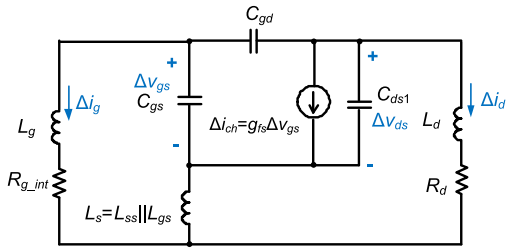

Fig. 7. DM equivalent circuit of paralleled MOSFETs.

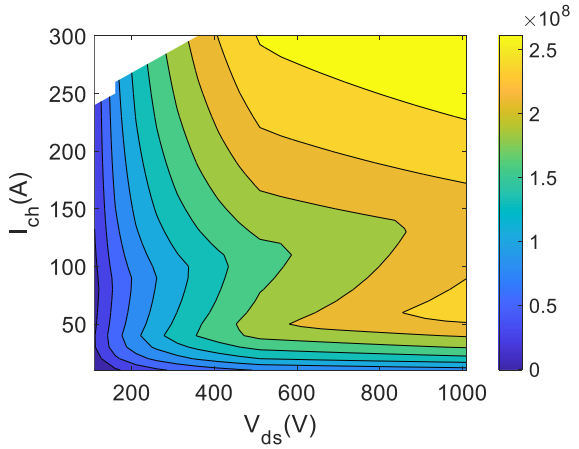

Fig. 8. Real parts of complex conjugate eigenvalues under various voltage and current levels for neighboring die pair.

the analyzed circuit but does not change the parallel stability issue itself. The state-space vector $\vec{x}$ of the DM circuit can be expressed as

$$\vec{x} = [\Delta i_g,\ \Delta i_d,\ \Delta v_{gs},\ \Delta v_{ds}]^T\ . \tag{5}$$

From the physics standpoint, the equivalent circuit in Fig. 7 can be described as a feedback amplifier model. Transconductance is the amplification unit that gives a gain of g_{fs} from Δv_{gs} to Δi_{ch}. There are two ways Δi_{ch} provides feedback to Δv_{gs}:through C_{gd} and through L_s. For the first way, the variation of Δi_{ch} causes the variation of Δv_{ds} and induces current through C_{gd} to influence Δv_{gs}. For the second way, the variation of Δi_{ch} causes the variation of the current through and voltage across L_s, which can influence v_{gs} based on KVL of the gate loop. The unstable oscillation happens when positive feedback exists from Δi_{ch} to Δv_{gs}. The closed-loop gain and phase shift are determined by g_{fs} and impedance networks of the gate, source, and drain parts. In this article, we focus on the eigenvalues of the system matrix, which is equivalent to the analysis of the phase or amplitude margin of the system and can give more comprehensive information about the system.

The system matrix of the linearized state-space model of the DM equivalent circuit can be found in [21, pp. 5–36]. The eigenvalues are solved with the extracted parasitic and nonlinear transconductance and capacitances. With four independent state variables, four eigenvalues can be solved. Among the four eigenvalue solutions, the two real eigenvalues are always negative during all voltage and current levels. Only the two complex conjugate eigenvalues are possible to have and share a positive real part, causing instability or divergent response of the circuit. The real parts of the complex conjugate eigenvalues are given in the contour, as shown in Fig. 8. As given in (4) and Fig. 3, a positive real value means the oscillation amplitude would increase at the operating point.

Note that positive α solutions exist at high-voltage and high-current regions. The low-voltage or low-current part is normally stable with negative α solutions. Moreover, the trend is that the higher voltage and current, the greater the real part value or the more unstable the system is. This explains why the instability issue is more likely to occur at high-voltage and high-current stresses.

To model the DM oscillation for the number of paralleled dies greater than two, the entire power module with ten paralleled dies can be modeled and solved by MATLAB with PLECS for eigenvalues. The parasitic inductance between each neighboring pair is twice the DM parasitic inductance, as given in Table I. There are 38 sets of solutions, and 18 of them are possible to give positive real parts of complex conjugate eigenvalues. All the real parts of complex conjugate eigenvalues have the same trend that the higher voltage and current, the greater the value of the real part. Due to limited space, only one set of typical eigenvalue solutions is given. The contour curves of real and imaginary parts are shown in Fig. 9. The imaginary parts indicate a natural frequency between 130 and 170 MHz, which covers the observed oscillation frequency of around 150 MHz in the experiment.

III. Influence of Switching Trajectory on Parallel Stability

The stability analysis can be used for both turn-ON and turn-OFF processes. In this article, the turn-OFF process is the focus of the analysis because SSCB application has high-current turn-OFF for short-circuit protection.

A. Conventional Turn-Off Trajectory

The soft turn-OFF is normally used for short-circuit protection by slowing the turn-OFF speed to reduce the overvoltage, which can cause hard switching with a large overlap of v_{ds} and i_{ch}. The simulation waveforms of die CPM2-1200-0025B turning OFF ~200-A current with 55-Ω gate resistance is shown in Fig. 10(a). The gate resistance is designed largely for soft turn-OFF during the short-circuit protection. The voltage first increases to around 700 V, then the current begins to decrease. This generates a large overlap of voltage and current. The turn-OFF trajectory of V_{ds}–I_{ch} is shown in Fig. 10(b).

B. Influence of Conventional Turn-Off Trajectory on Stability

Fig. 11 shows the turn-OFF trajectory overlapped with the contour curve of real parts of complex eigenvalues given in Fig. 8. The trajectory goes through the unstable region where both voltage and current are high, which causes instability of the paralleled dies in the power module. However, the switching

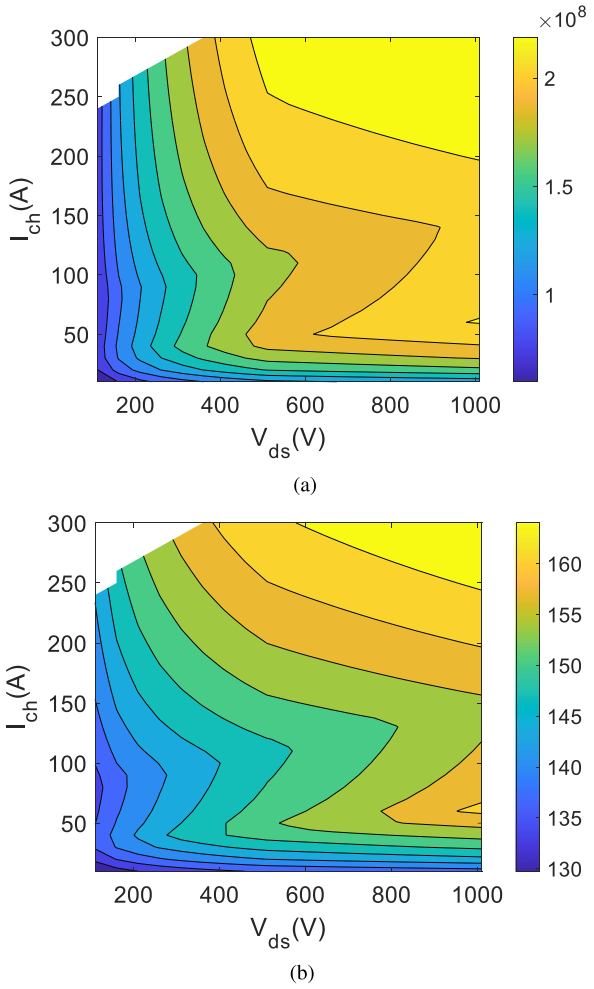

Fig. 9. Real and imaginary parts of a complex conjugate eigenvalue set under various voltage and current levels for the entire power module. (a) Real part. (b) Natural frequency: imaginary part divided by 2 π (Unit: MHz).

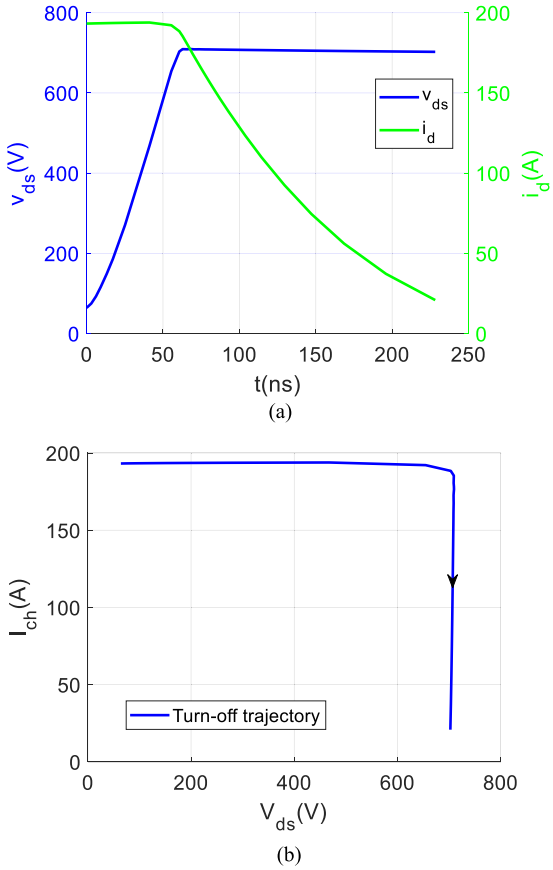

Fig. 10. Turn-OFF waveforms and trajectory on *I–V* curve of CPM2-1200-0025B. (a) Turn-OFF waveforms. (b) Turn-OFF trajectory.

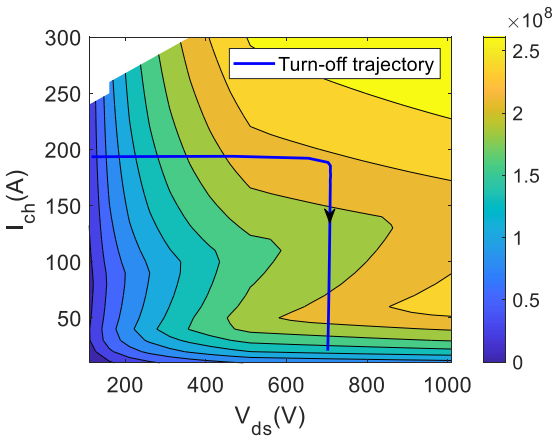

Fig. 11. Turn-OFF trajectory on the stability contour.

trajectory varies for different switching conditions, which means it can be possible that certain switching trajectories can go through a region with smaller real parts to realize a more stable switching transient than the conventional trajectory.

C. Influence of Model Accuracy on Analysis Results and Limitations of the Analysis

The SPICE model provided may not reflect accurate device characteristics, especially the transconductance. To check the influence of the SPICE model accuracy on the analysis results, a sensitivity analysis is given here. In Fig. 12, the transconductance has been scaled to 70% and 130% of the original value to check the influence. It can be found that for both cases, higher voltage and current results in worse stability for the parallel MOSFETs, which is the same as the previous analysis result.

One of the key factors contributing to the result is the channel length modulation of the SiC MOSFETs. The transconductance increases with the drain-to-source voltage in the saturation region. This phenomenon has been explained based on semiconductor physics in [21] and experimentally verified in [23]. This also supports the analysis results even if the SPICE model has inaccuracies.

One limitation of the model is that the dwell time is not included for a comprehensive analysis of the sufficient conditions for the observable gate oscillation. The switching trajectory that goes through the unstable region with positive real parts is a necessary but not sufficient condition for the observable gate oscillation. It could be possible that no gate oscillation is

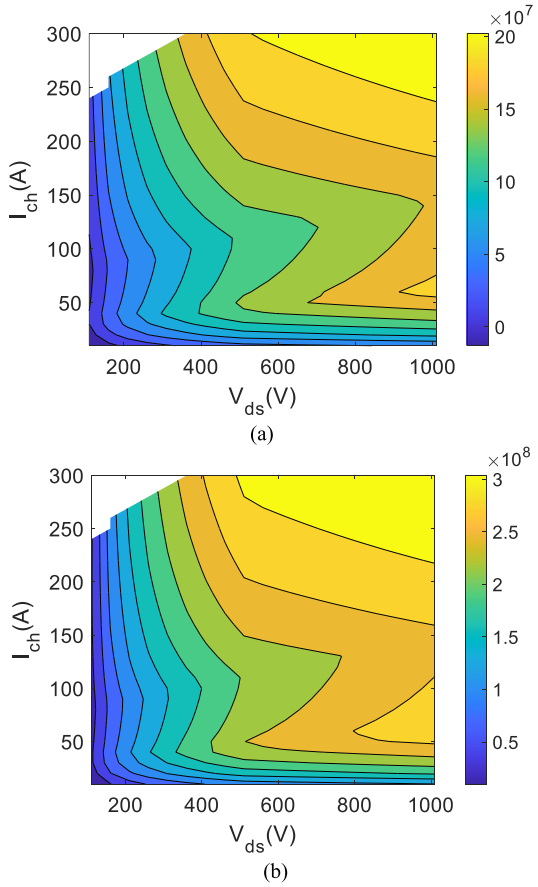

Fig. 12. Transconductance sensitivity influence on the analysis results. (a) 70% of the original transconductance. (b) 130% of the original transconductance.

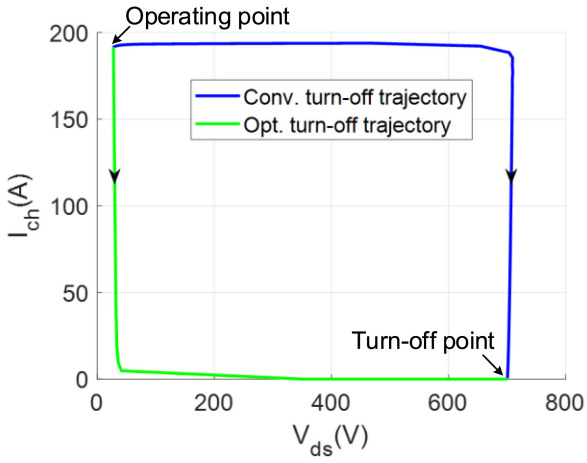

Fig. 13. Optimal switching trajectory.

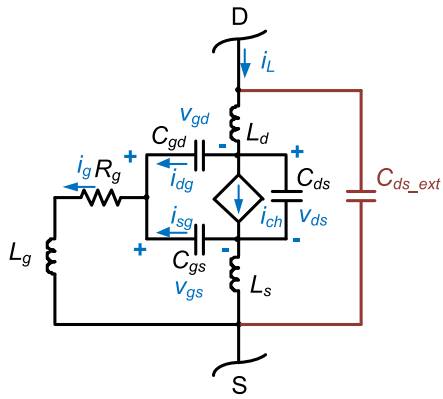

Fig. 14. MOSFET equivalent circuit during turn-OFF.

observed if the device quickly passes through the unstable region with very limited dwell time.

Another limitation of the analysis is that dynamic thermal imbalance is not considered during switching due to the half-circuit approximation. The thermal domain could be considered to give a more comprehensive analysis in the future.

IV. Proposed Method to Improve Parallel Stability of Power Modules by Manipulating the Switching Trajectory

In this section, a method is proposed to enhance the turn-OFF current capability limited by the paralleled MOSFETs oscillation issue for SSCBs, where high short-circuit protection current is required (as large as 6–12 times of the rated current [11]–[13]). Since the turn-ON of the switch is normally under the soft-start function of SSCBs, which is under low-voltage stress with limited current spike, the analysis focuses on the turn-OFF process of paralleled MOSFETs.

A. Optimal Turn-OFF Trajectory for Paralleled MOSFETs Stability

The idea is to manipulate the switching trajectory to avoid the unstable region with both high voltage and current so that the switch can remain in a stable region during the switching transient. The optimal turn-OFF trajectory is shown in Fig. 13. During turn-OFF, the channel current decreases before the drain-source voltage increases to avoid the unstable region.

B. Manipulate the Turn-OFF Trajectory

To achieve the optimal turn-OFF trajectory, an extra drain-source capacitance can be applied in Fig. 14. The equivalent switch represents the multiple paralleled dies. During the turn-OFF transient, the gate current i_g discharges C_{gd} and C_{gs}. At the same time, the load current i_L would charge C_{ds} to ensure that v_{ds} is almost equal to v_{dg} ($-v_{gd}$) because v_{ds}-$v_{dg} = v_{gs} \approx 0$ V. Therefore, with very fast C_{gd} discharge speed or large C_{ds}, most load current i_L would charge C_{ds} instead of flowing through the MOSFET channel. Then, the overlap of channel current and drain-source voltage can be avoided during the turn-OFF transient. To enable this, the requirement of the total drain-source capacitance value C_{ds_tot} ($= C_{ds}+C_{ds\_ext}$) is that $I_g/C_{gd} >> I_L/C_{ds\_tot}$.

Another way to understand this requirement is that during the turn-OFF transient, the *dv/dt* of v_{dg} is close to the *dv/dt* of v_{ds} and $I_{dg}/C_{dg} \approx I_L/C_{ds\_tot}$. With $I_g/C_{gd} >> I_L/C_{ds\_tot} \approx I_{dg}/C_{gd}, I_g >> I_{dg}$. This means the main part of I_g discharges

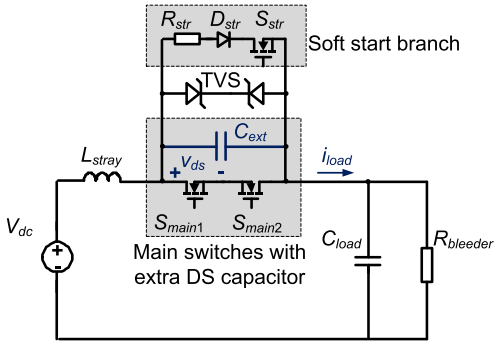

Fig. 15. Soft-start circuit of SSCB.

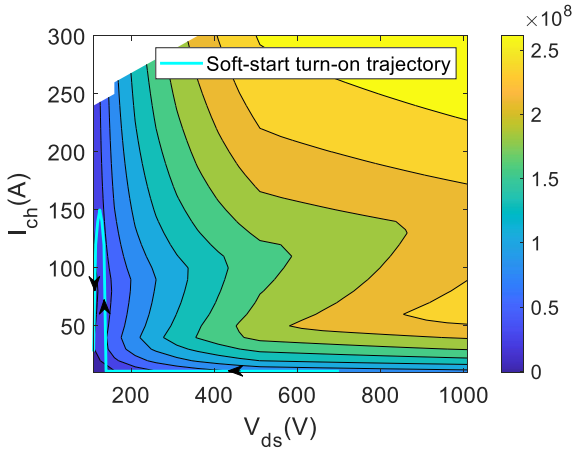

Fig. 16. Turn-ON trajectory on the stability contour with soft-start function.

C_{gs}, resulting in a quick decrease of v_{gs} and i_{ch} while v_{ds} slowly increases. This makes the overlap of v_{ds} and i_{ch} small to achieve the optimal turn-OFF trajectory.

The required drain-source capacitance can be calculated as

$$C_{ds\_\mathrm{tot}} = \frac{3.5 I_L C_{gd}}{I_g} = \frac{3.5 I_L C_{gd}}{V_{\mathrm{Miller}}/R_g} = \frac{3.5 \times 2250\,\mathrm{A} \times 200\,\mathrm{pF}}{8.5\,\mathrm{V}/5.5\,\Omega} = 1.02\,\mu F$$

where V_{Miller} is the Miller plateau voltage and C_{gd} is gate-to-drain capacitance at $V_{ds} = 200$ V. With C_{ds} of the power module around 2.2 nF at $V_{ds} = 200$ V, the extra paralleled capacitance value is selected as 1 μF. This method avoids changing the structure and parameters inside the power module and can be easily implemented.

Note that the proposed method is mainly for SSCB applications where the pulsewidth modulation operation is normally not required. Thus, the extra DS capacitor would not induce charge and discharge loss. For general applications, it would be possible to utilize some other techniques, e.g., active gating or soft switching, to achieve the optimal switching trajectory to improve the parallel stability.

C. Manipulate the Turn-ON Trajectory Using Soft Start

Adding an extra drain-source capacitance may result in a current spike during the turn-ON transient. The soft-start functions commonly used in SSCBs can help avoid this issue [21]. As shown in Fig. 15, the soft-start branch, which consists of a low power switch S_{str}, a soft-start resistor R_{str}, and a diode D_{srt}, is paralleled with the main switches. S_{str} of the soft-start branch can be turned ON first to charge the load capacitance to reduce the drain-source voltage across the main switches. Then, the main switch can be turned ON with low drain-source voltage stress to avoid the unstable region.

The turn-ON trajectory of S_{main1} in Fig. 15 with soft start is shown in Fig. 16. The voltage first decreases to a threshold voltage, which is normally much lower than the voltage stress of the device, with zero channel current of the main switches since DS capacitance is discharged through the soft-start branch. Then, the main switches are turned ON when DS voltage is equal to or lower than the voltage threshold. A limited current spike would happen during turn-ON. Since now the DS voltage is below the threshold voltage, the turn-ON trajectory can be limited to the region with small or negative real parts of eigenvalues to improve the parallel stability.

V. Nondestructive Test of Power Module Instability Issue

The gate oxide of the power module can be damaged by the gate oscillation caused by the paralleled MOSFETs instability. Thus, it is important to use a nondestructive test method. Tests are done by gradually increasing the turn-OFF current. Test waveforms before the failure of the power module are given in Fig. 17. The gate voltage oscillation can be observed before the oscillation amplitude exceeds the maximum allowed gate voltage to make the device fail. In Fig. 17(a), when turning OFF 2065 A, no high-frequency oscillation can be observed in the gate voltage. In Fig. 17(b), when the turn-OFF current is increased to be 2245 A, high-frequency (∼150 MHz) oscillation of the gate voltage can be observed, and the amplitude of the gate oscillation is around 3-V. In Fig. 17(c), when the turn-OFF current is increased to 2425 A, high-frequency (∼150 MHz) oscillation is more obvious (around 6.5-V oscillation amplitude) than Fig. 17(b). If the turn-OFF current keeps increasing after this, the gate oscillation exceeds the maximum allowable voltage and damages the power module. Therefore, to conduct the nondestructive test, the key is to observe the gate waveforms for the high-frequency gate oscillation while gradually increasing the turn-OFF current. Once the high-frequency gate oscillation is observed, the turn-OFF current can be taken as an oscillation current threshold and should not be increased anymore to avoid parallel instability.

Note that the probes and scopes must have higher bandwidth than the oscillation frequency. For the test waveforms given in this article, the scope used is DPO5104B (2-GHz bandwidth) from Tektronix, and the voltage probe used is a THDP0200 (200-MHz bandwidth) differential probe from Tektronix, which is good enough to observe the oscillation. The current probe used is

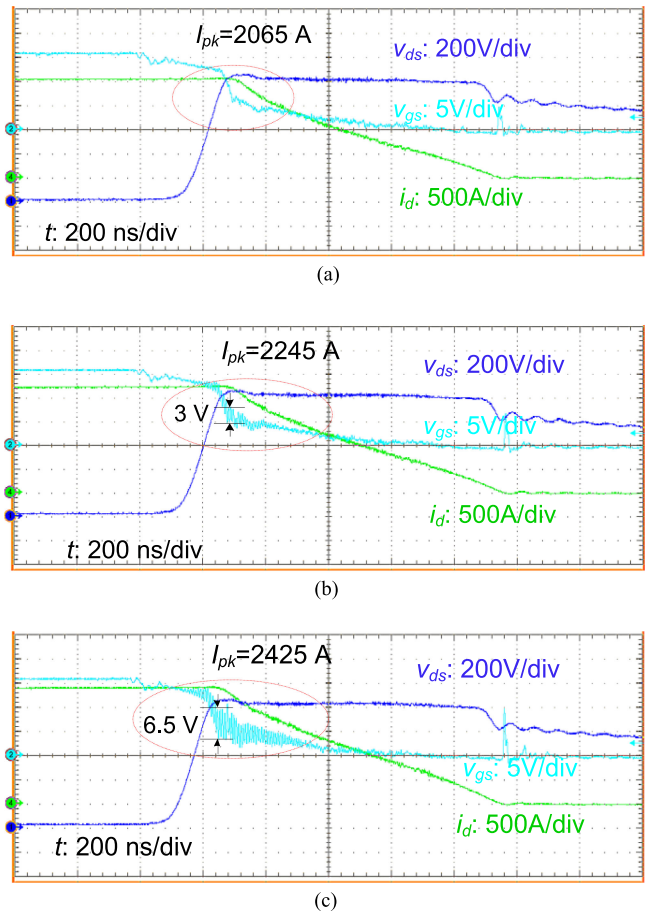

Fig. 17. Oscillation can be observed before the failure of the power module. (a) Turn-OFF current: 2065 A. (b) Turn-OFF current: 2245 A. (c) Turn-OFF current: 2425 A.

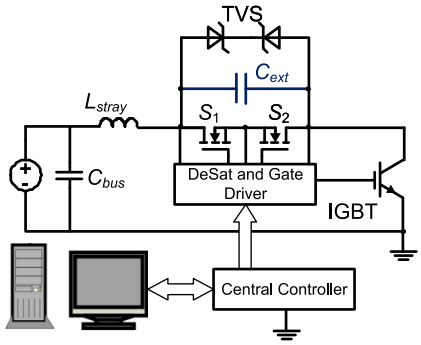

Fig. 18. Test diagram of DUT in SSCB.

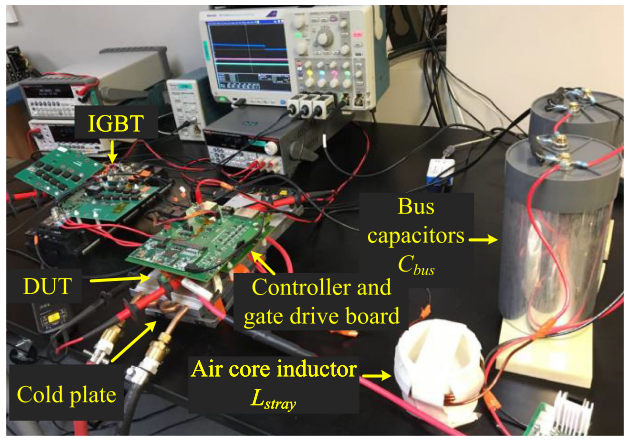

Fig. 19. Experimental test platform of dc SSCB.

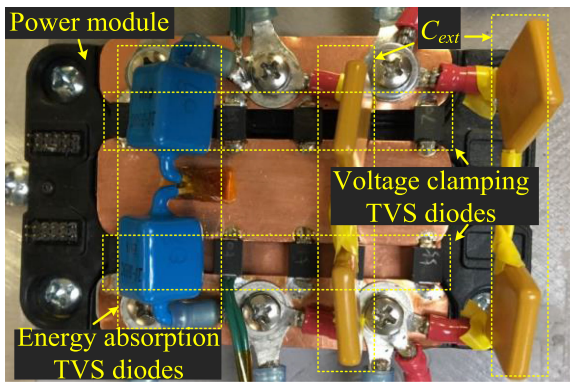

Fig. 20. Power module with paralleled capacitors.

CWT15 (16-MHz bandwidth) Rogowski coil from PEM, which cannot be relied on to observe the oscillation due to the low bandwidth.

VI. Experimental Results

Experiments are conducted to verify the analysis and proposed solution in SSCB applications. The SiC common source power module HT3220 [10] is used as the device under test (DUT). The antiseries switches inside it enables the bidirectional application. It is used with 250-A rated current at 60 °C ambient temperature. At the rated condition, the junction temperature is around 90 °C. The target short-circuit protection current is 2250 A, which is nine times of the rated current.

A. Test Platform and DUT

The test diagram and platform are shown in Figs. 18 and 19, respectively. A high-power IGBT is used for protection in case the power module fails to turn OFF the high current. The conduction time or input voltage can be adjusted to change the turn-OFF current, so the turn-OFF current can be increased slowly to observe the oscillation to keep the DUT safe. The temperature of the device can be controlled by the inlet coolant temperature of the cold plate.

Fig. 20 shows the DUT used for the test. An equivalent capacitance of 1 μF and some TVS arrays are paralleled with the power module. The detailed information of all the parts is listed in Table II. The TVS arrays are designed separately to absorb the energy and clamp the overvoltage during the short-circuit protection [25]. The turn-OFF gate drive resistance used is 5.5 Ω.

TABLE II
DUT RELATED PARAMETERS

Power module	HT-3220 (1.2 kV 642 A@T_c=25°C)
Energy absorption TVS diodes	AK10-380C × 2 (V_{br}=401 V)
Voltage clamping TVS diodes	ATV50C401JB × 12 (V_{br}=447 V)
Extra capacitance	1 μF × 4 (2 in series and 2 in parallel)
Gate drive IC	IXDD609+Si4564DY
S_{str}	C3M0065100K (1000 V 32 A@T_c=25°C)
D_{str}	GB01SLT12-214 (1200 V 1 A@ T_c=160°C)
R_{str}	SQP10AJB-200R (200Ω, 2 in series)

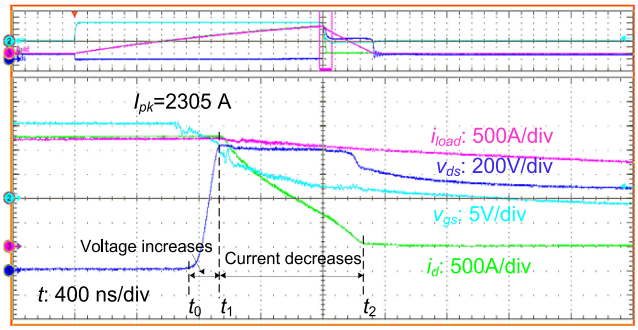

Fig. 21. Waveforms of turning OFF 2300 A @25 °C using the conventional turn-OFF trajectory.

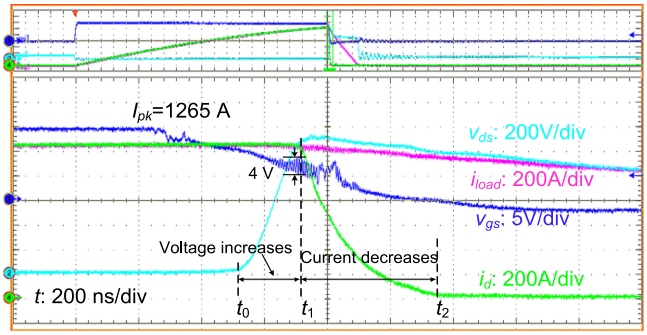

Fig. 22. Waveforms of turning OFF 1265 A @90 °C using the conventional turn-OFF trajectory.

B. Temperature Influence on Stability

Fig. 21 shows the key turn-OFF waveforms with the conventional turn-OFF trajectory at 25 °C. The turn-OFF current is 2305 A. The power module can successfully turn OFF this current at 25 °C. During the turn-OFF transient, the voltage increases first (from t_0 to t_1) to around 1050 V, and then the current drops to zero (from t_1 to t_2). The overlap of voltage and current has the same characteristic as the conventional turn-OFF trajectory given in Section III.

It is found that higher temperatures can worsen the parallel stability. Fig. 22 shows the key turn-OFF waveforms with the conventional turn-OFF trajectory at 90 °C. The temperature is selected to emulate the junction temperature at the rated condition. When the turn-OFF current is 1265 A, the gate oscillation can be noticed in the waveforms with an amplitude of around 4 V in Fig. 22. If the turn-OFF current further increases, the oscillation amplitude also increases and results in similar waveforms with

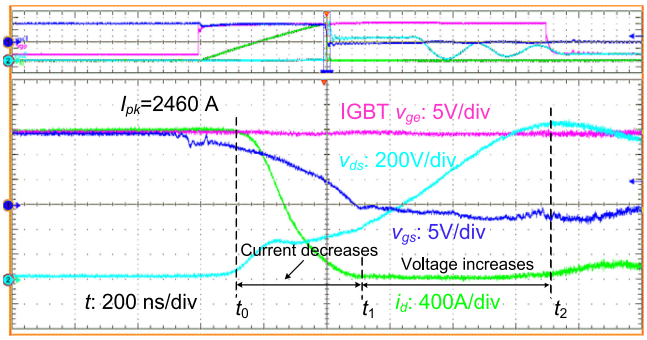

Fig. 23. Waveforms of turning OFF 2460 A @90 °C using optimal turn OFF trajectory.

TABLE III
COMPARISON OF TESTED RESULTS

Case	1	2	3
Temperature (°C)	25	90	**90**
Optimal or conventional turn-off trajectory	Conventional	Conventional	**Optimal**
Maximum turn-off current tested (A)	2305	1265	**2460**
Gate oscillation happens or not?	No	Yes	**No**

The bold entities show how the proposed method help improve the stability.

Fig. 2. The testing results show that the device has a lower turn-OFF oscillation current threshold at a higher temperature, which could be due to the higher transconductance at the higher temperature.

C. Verification of Proposed Switching Trajectory Manipulation Solution

Fig. 23 shows the key turn-OFF waveforms with the optimal turn-OFF trajectory at 90 °C. The turn-OFF current is 2460 A. The power module can successfully turn OFF this current at 90 °C. Based on the waveforms, the voltage slowly increases and keeps below 400 V when the current drops to zero (from t_0 to t_1). Then, the voltage increases to the TVS breakdown voltage from t_1 to t_2. By manipulating the turn-OFF trajectory this way, the device can avoid the unstable region during turn-OFF. The turn-OFF current capability increases from 1265 A with the conventional trajectory to 2460 A (1.94 times) with the optimal trajectory. Note that the turn-OFF current can be greater than 2460 A with the optimal switching trajectory. The reason we stop increasing the turn-OFF current after this test is that it has already exceeded the target short-circuit protection current of 2250 A.

The soft-start function is also implemented to verify the feasibility of manipulating the turn-ON switching trajectory. The load capacitor in Fig. 15 is 2 mF. The soft-start waveforms are given in Fig. 24. The auxiliary switch turns ON first to discharge the voltage across the DUT. When the drain-source voltage across the DUT is around 10 V, the main switch turns ON, which avoids the unstable region of the $I_{\rm ch}$–$V_{\rm ds}$ curve.

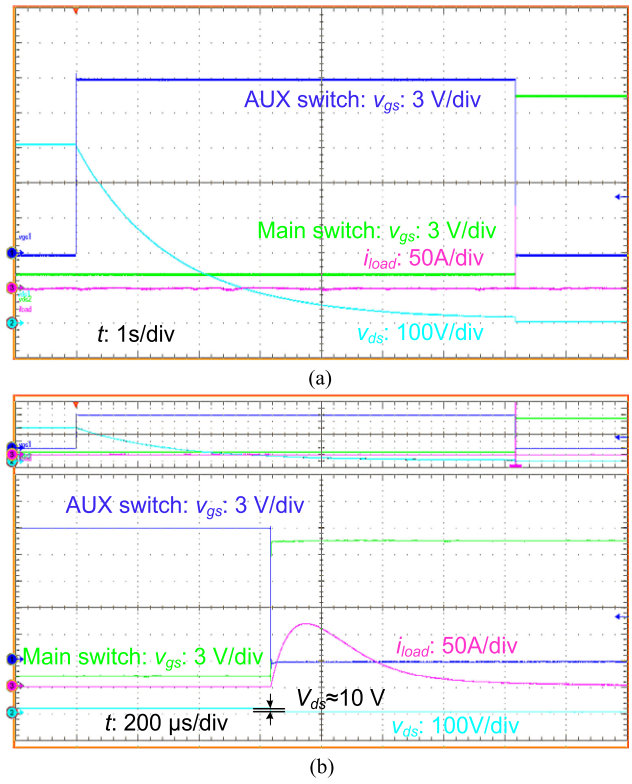

Fig. 24. Soft-start waveforms for DC SSCB. (a) Soft-start waveform. (b) Zoomed in soft-start waveform.

D. Comparison of the Turn-OFF Oscillation Current Threshold

Table III compares the turn-OFF current capability under different temperatures and with different switching trajectories. The comparison of case 1 and 2 shows that higher temperature worsens the parallel instability issue. The comparison of case 2 and 3 shows that the turn-OFF current capability increases from 1265 to 2460 A with the optimal trajectory, which is 1.94 times of turn-OFF oscillation current threshold with the conventional turn-OFF trajectory.

VII. Conclusion

Paralleled MOSFETs can have instability issues, and the issue can also happen with paralleled dies in a power module. Different from previous analysis focusing on one single operating point, this article analyzes the stability of the paralleled MOSFETs under various voltage and current conditions considering the switching trajectory influence and nonlinear device parameters. The analysis results show that the higher voltage and current region corresponds to the greater real part of complex eigenvalues, which explains why the instability is more likely to occur at high-voltage and high-current stresses.

The conventional hard switching trajectory goes through the unstable region of the *V–I* curve due to the overlap of voltage and current, which can cause the DM oscillation of the paralleled switches. To improve the stability of paralleled switches during the high-current turn-OFF, we propose a method to manipulate the switching trajectory to avoid the unstable region mainly in SSCB applications. The optimal turn-OFF trajectory is implemented by paralleling extra capacitance across the drain to the source of the device. The optimal turn-on trajectory is realized by the soft-start function.

To verify the analyses without damaging power modules, a nondestructive test method is used for testing the turn-OFF oscillation current threshold. Experimental results verify that the proposed trajectory optimization method can improve the parallel stability in the SSCB application. The turn-OFF current can be increased from 1265 A (5.1 times of rated current) with the gate oscillation by the conventional turn-OFF trajectory to 2460 A (9.8 times of rated current) without the gate oscillation by the optimal turn-OFF trajectory at 90 °C. In addition, experimental results show that higher temperature makes paralleled SiC MOSFETs more unstable, which could be caused by transconductance variation but still needs verifications by future work.

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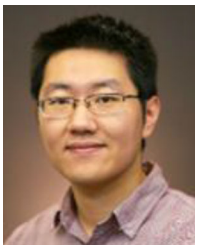

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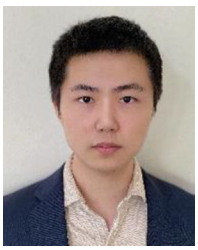

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