Methodology of Low Inductance Busbar Design for Three-Level Converters

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***Abstract*- Three-level converters are more susceptible to parasitics compared with two-level converters because of their complicated structure with multiple switching loops. This paper presents the methodology of busbar layout design for three-level converters based on magnetic cancellation effect. The methodology can fit for 3L converters with symmetric and asymmetric configurations. A detailed design example is provided for a high power three-level active neutral point clamped (ANPC) converter, which includes the module selection, busbar layout, and DC-link capacitor placement. The loop inductance of the busbar is verified with simulation, impedance measurements, and converter experiments. The results match with each other, and the inductances of short and long loops are 6.5 nH and 17.5 nH respectively, which are significantly lower than the busbars of NPC type converters in other references.**

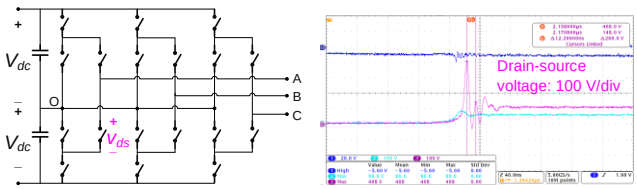
I. Introduction

In electric propulsion systems such as electric vehicles (EV) and more electric aircraft (MEA), high efficiency and high power density are the critical requirements. For instance, the U.S. Department of Energy (DOE) has set the power density target of 33 kW/L for electric traction drive systems (ETDS) in EVs by 2025 [1]. The National Aeronautics and Space Administration (NASA) also has proposed a roadmap to achieve 25 kW/kg specific power and 99.5% efficiency for inverters in aircraft electric propulsion drives [2].

To achieve these challenging goals, there have been some trends in traction inverter design recently. First, higher DC bus voltage is preferred to enable higher power delivery capability and decrease the weight and loss on the cable [3]. In such cases, the voltage stress across the power semiconductor devices in the conventional two-level (2L) converters is an issue. Three-level (3L) converters are more attractive since the voltage stress on power devices is reduced. In addition, they have higher power quality and lower electromagnetic noise [4], [5].

The adoption of wide bandgap (WBG) power semiconductor devices, especially silicon carbide (SiC) devices, is another trend in traction drive systems [6]. These emerging devices can provide higher voltage blocking capability, lower conduction loss, higher switching speed, and better thermal performance. Nevertheless, parasitics play a more important role due to the increase of *dv*/*dt* and *di*/*dt*, which necessitates better circuit layout.

In high power converters, busbar is the commonly used connector for power modules, capacitors and filters, and it not only bears high voltage and delivers high current in steady state, but also transmits high frequency voltage and current during switching transitions. The resonance between the loop inductance of the busbar and the parasitic capacitance of power semiconductor devices can cause voltage and current overshoot. A poor design of the busbar with high parasitic inductance produces higher harmonics, and the overshoot can damage the power devices. As shown in Fig. 1, the peak of the drain-source voltage of the device in a 3L-ANPC converter during the switching transient is much higher than its steady state value. This issue becomes even more severe and complicated in 3L topologies, where multiple switching loops exist during the switching transient [7-11]. The overvoltage can be mitigated by using snubbers [12], [13]. However, commonly used passive snubbers introduce extra energy loss and decrease the switching speed of the device. Active snubbers increase the cost and complexity and reduce the reliability of the converter system. In all, without a proper design of the busbar with low loop inductance, the high switching speed capability of SiC power devices cannot be fully utilized. In addition, the sub-μH loop inductance influences the current rise during a short-circuit, while the device failure mainly happens after the current saturates due to the generated high energy [14]. Therefore, lower loop inductance has little impact on short-circuit withstand capability of the circuit.



(a) (b)

Fig. 1. 3L-ANPC converter and voltage overshoot. (a) Topology. (b) Severe voltage overshoot caused by poor loop inductance.

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Design guidance of busbar layout has been discussed extensively [15-22]. However, most of them focused on 2L converters, and the design method may not be suitable for 3L converters with multiple switching loops. In [23-31], busbars have been designed for 3L converters such as neutral point clamped (NPT) and T-type converters. Nevertheless, there is no generalized design methodology that can be implemented in busbar design for different 3L converter topologies.

Based on the review and analysis above, this paper proposes a methodology for busbar layout in 3L converters considering multiple switching loops in different topologies. With the methodology, a detailed example is demonstrated to design a busbar with low loop inductance for a high power 3L active neutral point clamped (ANPC) converter.

This paper is organized as follows. Section II analyzes the switching loops in 3L converters. Based on the loop analysis, Section III proposes the design methodology for busbar layout. Following the methodology, Section IV shows the detailed design of the busbar for a 200 kVA 3L ANPC converter. Section V gives the simulation and experimental verification of the designed busbar, and Section VI provides a conclusion.

II. Evaluation of Switching Loops in Three-Level Converter

To optimize the layout of 3L converters, it is necessary to have comprehensive understanding on the switching loops and parasitic distribution in different topologies. According to the structure of the switching loops, 3L converter topologies can be categorized into two main groups: converters with symmetric and asymmetric switching loops.

A. Converter with Symmetric Loops

A typical example of the 3L converter with symmetric switching loops is the 3L T-type converter. Fig. 2 plots the configuration of a single phase-leg of the 3L T-type converter with switching loops and busbar parts highlighted. The phase-leg contains two high frequency commutation loops.

As shown by the modulation in Fig. 2, S_H and S_N operate complementarily at high switching frequency during the positive half line cycle to provide the positive and neutral output voltage. The main commutation loop involves S_H and S_N, which is a typical 2L structure. Meanwhile, as the voltage across S_N jumps between $V_{dc}/2$ and 0, the voltage across S_L also changes between $V_{dc}/2$ and V_{dc} even though S_L is a non-active switch. Therefore, both switching loops exist during the half line cycle. Assuming each busbar part is independent and is not coupled with other busbar parts, the total parasitic inductance of each loop equals to the sum of the ESL of the decoupling capacitors, the stray inductances of S_N and S_H, and the inductances of positive and neutral busbar parts.

From the schematic point of view, the two switching loops have identical and symmetric structure, and the sources of the two loops are different decoupling capacitors. Therefore, in the layout design, the two loops should also be identical to have the same parasitics.

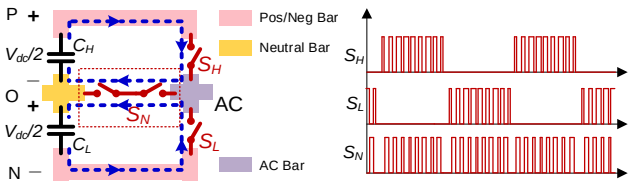


Fig. 2. Phase-leg of 3L T-type converter and the corresponding modulation.

B. Converter with Asymmetric Loops

For 3L converters with asymmetric switching loops, a typical example is the NPC type converter. The equivalent circuit of a single phase-leg in the 3L ANPC converter is illustrated in Fig. 3. Different busbar parts, parasitic inductances, and switching loops are highlighted. One example of the modulation scheme [11] is plotted in Fig. 3 as well, and it is divided into four states during one line cycle as listed in Table I. S_{1H}, S_{3H}, S_{1L} and S_{3L} operate at high switching frequency while S_{2H} and S_{2L} operate at line switching frequency.

During the half line cycle with negative output voltage, the operation state changes between N and O$^-$, which means that S_{1L} and S_{3L} operate at high frequency while S_{2L} and S_{3H} keep in ON state, and S_{2H} and S_{1H} are OFF.

As shown in Fig. 3, there are two switching loops. One goes through S_{1L} and S_{3L}, and it is marked by red color. This is the main commutation loop and is similar to the conventional loop in a 2L phase-leg. The parasitic inductance resonates with the output capacitance of S_{1L} or S_{3L}, depending on which one is the synchronous switch.

The other switching loop is shown by the green line. Since S_{2L} and S_{3H} are in ON state, S_{2H} is equivalently paralleled with S_{3L}. As a result, when S_{3L} is commutating with S_{1L}, the drain-source voltage of S_{2H} follows the drain-source voltage of S_{3L} even though S_{2H} is a non-active switch during the half line cycle. The parasitic inductance resonates with the output capacitance of S_{2H}.

Assuming each busbar part is independent and is not coupled with other busbar parts, the total parasitic inductance of the two loops can be evaluated as follows.

For the red commutation loop, it includes the decoupling capacitors, neutral busbar, negative busbar, and two power switches S_{1L} and S_{3L}. Thus, the total parasitic inductance L_{st} of the red loop is

$$L_{st} = L_C + L_o + L_n + 2L_s \tag{1}$$

where L_C is the ESL of the decoupling capacitors, L_o and L_n are the inductances of the neutral and negative busbar parts, and L_s is the inductance of each power switch.

In terms of the green loop, it consists of the decoupling capacitors, neutral busbar, two parts of middle busbar, negative busbar, and four power switches S_{1L}, S_{3H}, S_{2H} and S_{2L}. Thus, the total parasitic inductance L_{lg} of the green loop is

$$L_{lg} = L_C + L_o + L_n + 2L_m + 4L_s \tag{2}$$

where L_m is the inductance of the middle busbar part.

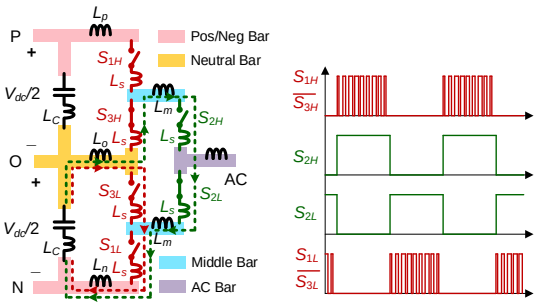


Fig. 3. Phase-leg of 3L ANPC converter and the corresponding modulation.

TABLE I. OPERATION STATES OF SINGLE PHASE 3L-ANPC CONVERTER.

State	S_{1H}	S_{3H}	S_{2H}	S_{2L}	S_{3L}	S_{1L}
P	On	Off	On	Off	On	Off
O^+	Off	On	On	Off	On	Off
O^-	Off	On	Off	On	On	Off
N	Off	On	Off	On	Off	On

It can be concluded that the green loop has larger parasitic inductance than the red one does, which matches with the analytical result in [9]. Therefore, the red loop is named as short loop, while the green loop is the long loop. Different from T-type converters, the two loops in a 3L ANPC converter are not identical. In addition, the two loops share the same decoupling capacitor as the source. This asymmetric structure is more complicated and requires special attention to the long loop since it normally has higher parasitic inductance.

III. METHODOLOGY OF BUSBAR DESIGN CONSIDERING MULTIPLE LOOPS

A. Magnetic Cancellation Effect

To minimize the loop inductance, the magnetic cancellation effect [32] should be utilized. For a typical busbar with two laminated plates in Fig. 4, the parasitic inductance of a plate includes two parts: self-inductance and mutual inductance [33].

The self-inductance L of one plate can be calculated with the equation from [15], [21]

$$L = \frac{\mu_0 \mu_r l}{\pi}\left(\frac{1}{8} + \frac{2h}{h+w}\right) \qquad (d \gg h \,\|\, d+h \gg w) \tag{3}$$

where μ_0 and μ_r are the vacuum permeability and the relative permeability of the insulation material; l, w and h are the length, width and thickness of the plate; d is the distance between two adjacent plates.

The mutual inductance M between two plates is calculated as

$$M = \frac{\mu_0 \mu_r l h}{\pi\sqrt{4(d+h)^2 + kw^2}}\cos\varphi \tag{4}$$

where k is the correction coefficient and φ is the angle between the current direction of two plates. When the currents have opposite directions, φ=180° [15], [21].

If the two plates have the same shape and the current directions are opposite, the magnetic fields generated by the currents on two plates have a canceling effect. In such a case, the mutual inductance can cancel part of the self-inductance, and the total parasitic inductance of the busbar is

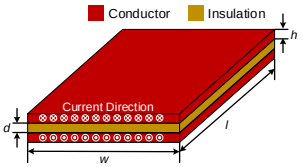


Fig. 4. Typical structure of two-layer busbar.

$$L_{sum} = \frac{\mu_0 \mu_r l}{\pi}\left(\frac{1}{4} + \frac{4h}{h+w} - \frac{2h}{\sqrt{4(d+h)^2 + kw^2}}\right). \tag{5}$$

From (5), the effective way to decrease the total loop inductance is to decrease the distance, and increase the overlap area of the two plates. This provides the theoretical basis of the layout design.

B. Methodology of Busbar Layout Design

A procedure is proposed here to provide the guidance for designing two-layer laminated busbars for 3L converters as shown in Fig. 5.

1) Place the power modules. The placement of the power modules significantly influences the busbar layout. In most cases, all the power modules are located in the same plane. Hence, this step can be accomplished in a 2-D planar layout. The primary design criteria include two aspects. a) For symmetric loops, an identical layout should be kept to achieve the same parasitics. b) The connection between the busbar and modules should be designed for ease of manufacturability. In a multi-layer busbar, holes have to be drilled on the bottom layers so that the connectors on the upper layer can go through and touch the power module. As a result, the effective area of the bottom layers reduces, and the current flow can be affected. More explanations on this point will be shown in the design example in the next section.

2) Determine the available busbar parts and find the parts shared by multiple loops. The composition of each loop should be listed to understand the involved busbar parts. For example, the upper loop of the T-type converter in Fig. 2 consists of three parts. The positive busbar part connects the upper side decoupling capacitor with the drain of upper side switch S_H. The neutral busbar part connects the decoupling capacitors with S_N. The AC busbar part connects the common source switch S_N with the other two switches. Similarly, the lower loop also includes three parts, and the neutral and AC busbar parts are shared by the two switching loops.

3) Place the busbar parts. This step is conducted in 3-D. First, the returning path should be selected from the shared parts by multiple switching loops, and it should be placed in one layer. For example, the neutral or AC busbar can be the returning path for both loops in Fig. 2. Second, place the rest of the busbar parts side by side in one layer, and they serve as the outgoing paths. Note that the symmetric loops should have the same layout.

4) Increase the area of the returning path to fully overlap with the outgoing paths. Based on the above analysis, the outgoing

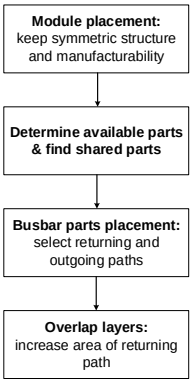


Fig. 5. Flowchart of design methodology.

and returning paths should be overlapped to maximize the magnetic cancellation effect. Normally, there is only one returning path and multiple outgoing paths based on the design above. Therefore, the area of the returning path should be increased to cover all the outgoing paths.

Note that this is a general methodology that can be followed in the design. However, the detailed layout is highly dependent on the geometry of the components in the system such as power modules, coldplates and DC-link capacitors. A design example based on a 3L ANPC converter will be presented in the next section.

IV. Design Example of Busbar for Three-Level ANPC Converter

In this section, a layout example following the aforementioned design methodology is demonstrated for a 3L-ANPC converter, which is designed for future MEA applications proposed by NASA [2]. The objective is to design, build, and test a technology demonstrator high efficiency and high power inverter operating at cryogenic temperatures for eventual use in aircraft electric high-speed superconducting motors. Here, the designed three-phase converter is rated at 500 kVA at cryogenic temperatures. For room temperature verification, the power rating is 200 kVA with water-cooling. The input DC voltage is 1 kV, the output fundamental frequency is 3 kHz, and the switching frequency is 60 kHz.

A. Power Module Selection

Power modules should be selected before the busbar design based on the electric specification. In addition, power modules also contribute to the parasitic inductance in the switching loop. The ideal module is a single 3L-ANPC module with all the devices integrated. However, it is difficult to obtain because of limited commercial availability especially for high current ratings. Alternatively, half-bridge modules are preferred to reduce the external connection between switches. For a 3L-ANPC converter, three modules are required for each phase-leg.

With the development of packaging technology, the stray inductance inside the module is progressively getting lower. Here, the HT-3000 series SiC MOSFET power module from Wolfspeed is adopted. Fig. 6 shows a picture of the module packaging. According to the manufacturer, the stray inductance of the module can be lower than 5 nH.

Fig. 6. HT-3000 series SiC MOFET module and equivalent circuit [34].

B. Busbar Design

The detailed design procedure is presented here following the layout methodology in Section III-B.

1) Place the power modules. To keep the symmetric structure of the upper and lower side of the converter, there are mainly three ways shown in Fig. 7 to place the power modules in one plane. The colored lines represent the busbar connection among the terminals of the power modules and the capacitors.

Options (a) and (b) are the two cases of side-by-side placement. For option (a), the main issue is the conflict between busbar parts and the gate-source terminals of the modules (marked as "GS" in Fig. 7). To implement the gate drive boards, holes have to be drilled unavoidably on the busbar parts especially for the module in the middle. It decreases the effective conduction area and makes the loops less symmetric. In addition, the terminal for the ac busbar part is in the center and surrounded by other terminals, which makes it difficult for the connection of the ac output. Therefore, option (a) is not an ideal placement.

In terms of option (b), the ac output can be extended easily. However, there is a conflict between the neutral busbar (yellow line in the middle) and the middle busbars (blue lines). Assuming the neutral busbar is in the upper layer while the middle busbars are in the lower layer and they overlap with each other, holes have to be drilled on the middle busbars so that the neutral busbar can be connected with the module terminals.

Compared with (a) and (b), option (c) is more like the schematic of a 3L-ANPC converter. Because the line switching frequency module is not in the same row with the other two modules, the conflict between busbar parts and module terminals can be avoided. Therefore, option (c) is selected as the placement for further busbar layout. Although the length of the middle busbars seems longer than (a) and (b), it is not a critical issue because of the magnetic cancellation effect, which will be verified later in this paper.

2) Determine the available busbar parts and find the shared parts by multiple loops. Here, the loops in the lower side of the phase-leg as highlighted in Fig. 3 are taken as the design example. In terms of the short switching loop, it only includes two busbar parts: the neutral busbar and the negative busbar. The long switching loop is more complicated and critical, which consists of four busbar parts: the neutral busbar, negative busbar and two middle busbars. The neutral and negative busbar parts are the shared parts by two loops.

3) Place the busbar parts. Since the short loop only includes the neutral and negative busbar parts, only one of them can be selected as the returning path, and they should be laminated and located in two layers. Considering that the neutral busbar is also shared by the loops in the upper side of the phase-leg, the neutral busbar is selected as the returning path, and it is placed in one layer. All the other busbar parts are located in the other layer.

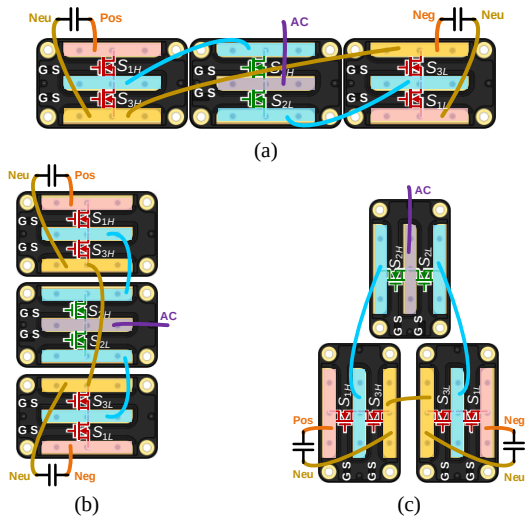


Fig. 7. Options of module placement.

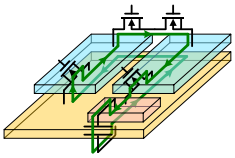


Fig. 8. 3-D view of busbar layout with long switching loop.

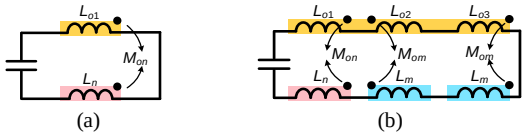


Fig. 9. Equivalent circuits of switching loops. (a) Short loop, (b) Long loop.

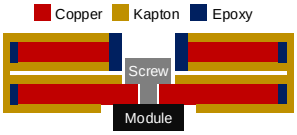


Fig. 10. Cross section of laminated busbar layers.

4) Increase the area of returning path to fully overlap with the outgoing paths. Fig. 8 plots the conceptual 3-D view of the busbar layout for the long switching loop. The middle busbars (blue) and the negative (orange) busbar are placed in the same layer. The neutral busbar (yellow) is a whole layer and serves as the returning path of the switching loop. With such design, the busbar parts are coupled, and the magnetic field can be canceled with the opposite current flowing direction, resulting in lower loop inductance. The layout of the loops in the upper side of the phase-leg follows the same procedure.

The equivalent circuits of the switching loops considering the busbar structure are illustrated in Fig. 9. For the short loop, the negative and neutral busbar are coupled, and the mutual inductance is M_{on}. For the long loop, the negative and middle busbars are coupled with the neutral busbars. The mutual inductance between the middle and neutral busbars is M_{om}. Note that the overlapped area between the negative and neutral busbar only accounts for a small portion of the total busbar area. Thus, the effective self-inductance of the neutral busbar in the short loop (L_{o1}) is smaller than that in the long loop (L_o=L_{o1}+ L_{o2}+ L_{o3}).

Based on Fig. 9, the total loop inductance calculation in (1) and (2) is modified as

$$\begin{cases} L_1 = L_C + L_{o1} + L_n - 2M_{on} + 2L_s \\ L_2 = L_C + L_o + L_n + 2L_m - 2M_{on} - 4M_{om} + 4L_s \end{cases}. \quad (6)$$

In terms of the implementation, Kapton sheets and epoxy are selected as the insulation material. Kapton sheets are mainly used between two layers while the epoxy is used to seal the edge of the holes and bars. Fig. 10 shows the cross-section of the busbar structure. The distance between two layers is 0.5 mm. The dielectric strength of the Kapton sheets and epoxy is 300 kV/mm and 15.7 kV/mm, which is sufficient for 1 kV voltage. However, if higher voltage rating is required, the distance may need to increase, resulting in higher loop inductance according to (5).

C. DC-Link Capacitor Selection and Placement

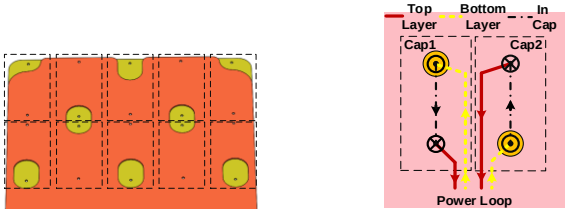
Film capacitors should be used for the DC-link capacitor due to their higher current capability and lower ESL compared with electrolytic capacitors. There are two options for the capacitor selection. One is to choose a single bulky capacitor, and the other is to use multiple capacitors in parallel.

Table II shows the comparison of the examples of the two options. Based on the simulation, the total required capacitance of the three-phase converter is 300 µF to maintain the stable DC voltage. To achieve 100 µF capacitance for a single-phase, ten smaller capacitors need to be paralleled. As the converter example here is for aircraft applications, weight reduction is a high priority in the design. From Table II, the total weight of ten smaller capacitors is less than a single bulky capacitor. Therefore, paralleling small film capacitors is adopted for the designed converter. In other applications, a single bulky capacitor can also be used as it is simpler for design. However, the ESL of one bulky capacitor is higher than 20 nH, which means that extra decoupling capacitors are required to reduce the ESL in the switching loop. On the other hand, ideally no decoupling capacitor is needed for small capacitors in parallel since the overall inductance is low enough. Nevertheless, paralleling capacitors requires more attention in layout to guarantee good current distribution.

As recommended in [35], the adjacent two paralleled capacitors are placed oppositely as shown in Fig. 11(a). There are ten capacitors arranged in two rows of five. The orange plate is the negative/positive busbar while the yellow one is the neutral busbar. Fig. 11(b) sketches the top view of the placement of the capacitors on the busbar plate. The red line represents the current on the top layer (positive/negative busbar), and the yellow dotted line is the current on the bottom layer (neutral busbar), while the dark dashed line is the current inside the capacitors. For the left side capacitor, the current flows into the capacitor on the bottom layer, while the current flows out of the right side capacitor through the top layer. Therefore, current on two laminated plates is in opposite directions, which enhances the magnetic cancellation, reduces the total inductance, and helps spread the current distribution.

TABLE II. CAPACITOR COMPARISON.

	Part	Value	ESL	Weight	Price	Qty
	FFVE6K01 07K	100 µF	25 nH	350 g	$ 60.00	1
	MKP1848C 61060JK2	10 µF	15 nH	15 g	$ 4.20	10



(a) (b)

Fig. 11. Paralleled DC-link capacitors on busbar. (a) Designed busbar parts for capacitors. (b) Top view of busbar with capacitors placement and current flow directions.

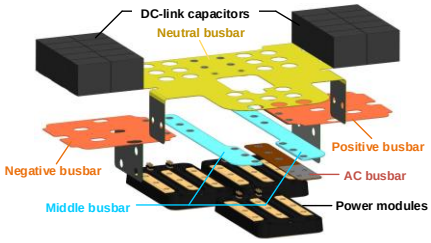


Fig. 12. Designed laminated busbar for single phase-leg.

The finalized exploded view of the busbar design for a single phase-leg is shown in Fig. 12. The neutral busbar is in the top layer and covers the area of the bottom layer, where the positive, negative, middle and AC busbars are placed laterally.

D. Equivalent Circuit and Common Mode Noise Analysis

With the designed busbar layout and selected power module and capacitors, an equivalent circuit of the 3-phase 3L-ANPC converter including the major parasitics is illustrated in Fig. 13. The blue parts are the parasitic inductances and capacitances on the busbar. The red parts are the stray inductances on the power modules and DC-link capacitors. The green parts are the parasitic capacitances between the power modules, load and ground.

In each phase, there are three major switching points, namely A_H, A_L and A in Phase A. The voltages on these three points serve as the common mode (CM) voltage sources. Due to the parasitic capacitances between the module package and the ground, CM current is generated during the switching transient. With different switching speed, the CM noise is impacted by the *dv/dt* and overvoltage.

Assuming all the parasitic capacitances between device and ground are the same, and neglecting the parasitic inductances on the busbar, the equivalent circuit of the CM noise with the three sources can be modeled as Fig. 14(a) [36], where v_{CM}= (v_{AO} + v_{BO} + v_{CO})/3, v_{CMH}= (v_{AHO} + v_{BHO} + v_{CHO})/3, and v_{CML}= (v_{ALO} + v_{BLO} + v_{CLO})/3. Based on the superposition theory, the time domain waveform of a noise source consists of two parts shown in Fig. 14(b): a switching frequency rectangular waveform v_{Rec}, and a high frequency noise waveform with turn-on/off slope and ringing v_{Hf}. With the modulation in Fig. 3, v_{Rec}= v_{RecH} + v_{RecL}. On the other hand, the *dv/dt* and ringing of v_{CM} is related to the long loop inductance, while that of v_{CMH} and v_{CML} is influenced by the short loop inductance. As a result, the high frequency noise is different for v_{CM} and v_{CMH} / v_{CML}. Hence, the equivalent circuit can be simplified to Fig. 14(c), where v_{Hf_st} is the combined high frequency noise of v_{CMH} and v_{CML}, and v_{Hf_lg} is the high frequency noise of v_{CM}. The rectangular noise v_{Rec} is independent of the busbar layout, and the parasitics mainly influence the high frequency noise v_{Hf_st} and v_{Hf_lg}.

A typical drain-source voltage during the switching transient and its spectrum envelope are plotted in Fig. 15. In the spectrum, there are three major frequency points. First, the -20 dB/dec region starts from the switching frequency f_{sw}. Second, the -40 dB/dec region begins from f_r, which is the minimum value of voltage rise and fall time during switching transient. In addition, a resonant peak occurs at f_{oc}, which is the resonant frequency caused by loop inductance and device output capacitance.

With the same switching speed, higher loop inductance only enlarges the resonant magnitude around f_{oc}. However, with lower loop inductance, higher switching speed can be adopted. In such case, the corner frequency f_r increases, resulting in higher noise in the high frequency range. In general, there is always a trade-off between high switching speed and high frequency EMI noise. The busbar design methodology in this paper provides the potential to increase the switching speed. However, a careful systematic design is needed to select the proper switching speed in real converter design.

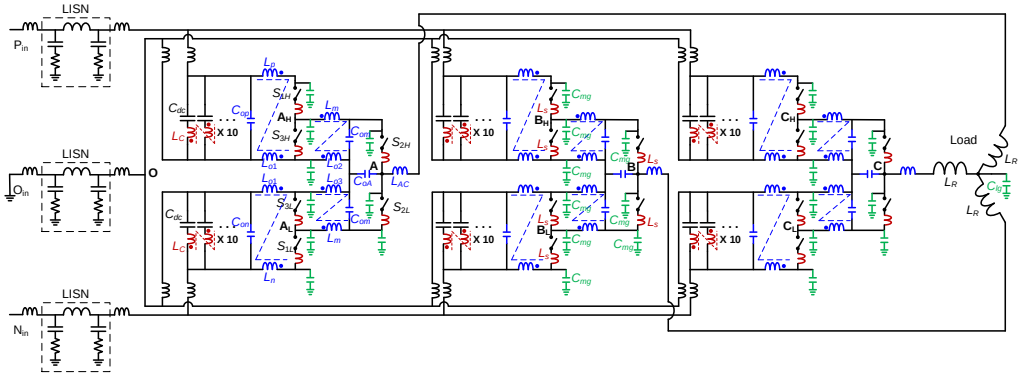


Fig. 13. Equivalent circuit of 3-phase 3L-ANPC converter with busbar.

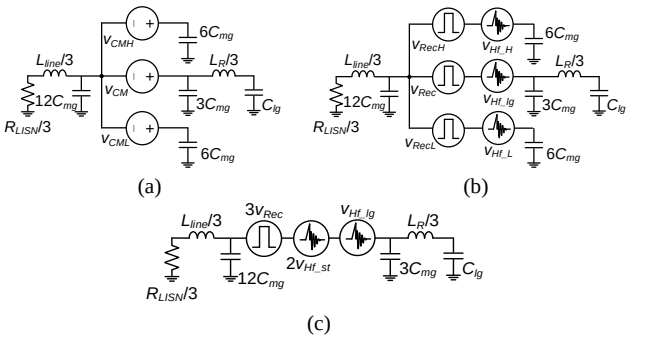


Fig. 14. Model of CM noise in 3L-ANPC converter. (a) Model with separate CM sources. (b) Composition of CM source. (c) Simplified model.

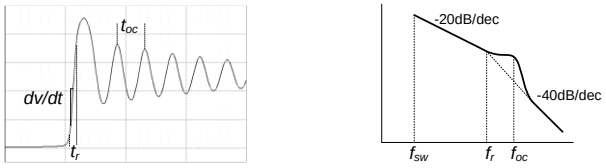


Fig. 15. High frequency noise from device drain-source voltage. (a) Typical drain-source voltage during transient. (b) Spectrum envelope.

V. Simulation and Experimental Verification

A. Simulation Evaluation

To obtain the loop inductance of the designed busbar, one way is to calculate the inductance based on equations such as (5). However, because of the complicated structure in Fig. 13 and the irregular shape of the busbar parts, it is difficult to get an accurate result with numerical calculation. Using finite element analysis (FEA) tools like Ansys Q3D, the parasitic inductance can be extracted from the 3-D drawing. Based on the simulation result, the busbar inductance of the long loop is 12.6 nH when the applied frequency is 20 MHz.

Fig. 16 illustrates the surface current density of the neutral busbar with two designs. Remarkably, the current does not flow along the shortest path A in the proposed layout. Instead, it follows path B, which overlaps with the middle busbar parts. If the area of the neutral busbar is reduced and does not fully overlap with the other busbar parts as shown in Fig. 16(b), the high frequency current on the returning path (neutral busbar) cannot follow the outgoing path (middle busbar). The simulated inductance of the long loop is 79.4 nH, which is 6.3 times higher than the proposed layout. This comparison verifies the effectiveness of the magnetic cancellation in the proposed layout.

The Simulation Program with Integrated Circuit Emphasis (SPICE) model of the equivalent circuit of the busbar with parasitics is extracted from Q3D and simulated in Saber along with the SiC MOSFET module model. As the inner structure of the power module is unknown, the stray inductance of each MOSFET is assumed to be 2.5 nH, and there is no mutual inductance. Fig. 17(a) illustrates the switching transient waveforms of the MOSFET drain-source voltage. The resonant frequency of the short loop is 34.5 MHz while that of the long loop is 18.9 MHz. Based on the output capacitance value from the module datasheet, the total parasitic inductances of the short

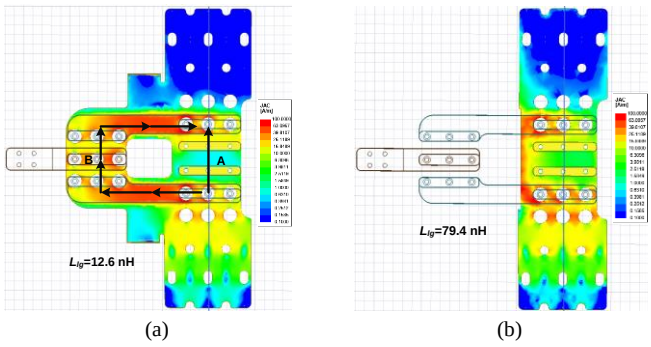


Fig. 16. Simulated surface current density on neutral busbar. (a) Proposed layout. (b) Layout without full overlap.

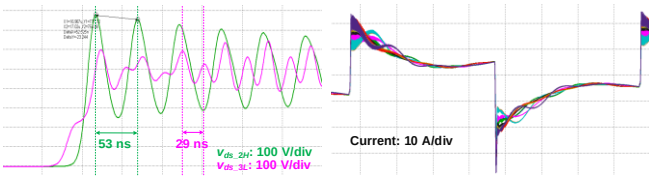


Fig. 17. Simulated waveforms with module, capacitor and busbar models. (a) Switching transient. (b) Current of paralleled DC-link capacitors.

and long loop including busbar parts, capacitors and power modules are calculated as 6.5 nH and 17.5 nH, respectively.

Fig. 17(b) plots the simulated current waveforms of ten paralleled DC-link capacitors in one switching cycle at full load conditions with the busbar model. The current RMS value of each capacitor is ~8 A, and the largest RMS difference among the capacitors is 0.6 A, which indicates good current balancing in the capacitors.

To evaluate the effect of busbar design on EMI noise, circuit models with different loop inductances and switching speed are simulated. C_{mg} and C_{lg} are assumed to be 100 pF. The simulation results of the DC side EMI noise spectra from 10 kHz to 100 MHz are plotted in Fig. 18. Comparing the spectra with different loop inductances, higher peaks occur on the red curve with higher inductances. Except at the resonant point, the two spectra overlap even in the high frequency range. On the other hand, increasing switching speed not only enlarges the resonant peak magnitude, but also increases the noise in the frequency range higher than 20 MHz in the green curve. This result matches with the analysis in Section IV-D.

B. Experimental Verification

Based on the design, the busbar prototypes are fabricated in the lab and by a busbar manufacturer, which are presented in Fig. 19. A hipot test is conducted and passed at 3 kV DC. The partial discharge test with an inception voltage of 2.2 kV and an extinction voltage of 1.9 kV with a limit of 10 pC also verifies the insulation of the busbar. An impedance analyzer is used to measure the impedance of the busbar loops including the DC-link capacitors but without the power modules. From Fig. 20, the measured short and long loop inductances of the lab-fabricated busbar are 2.5 nH and 10 nH, respectively. Considering the inductance of one power switch L_s is around 4 nH, the result matches with the simulation in Fig. 17.

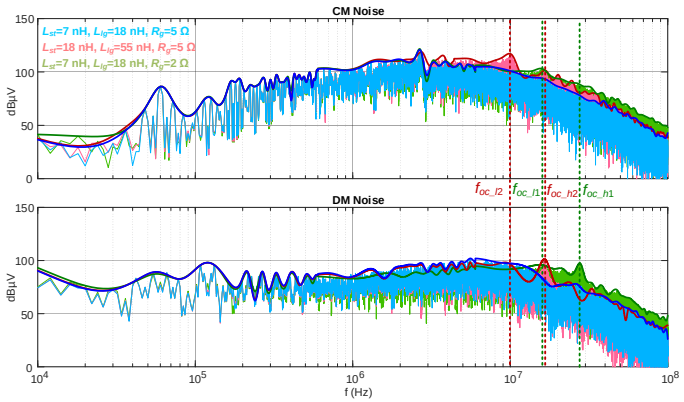
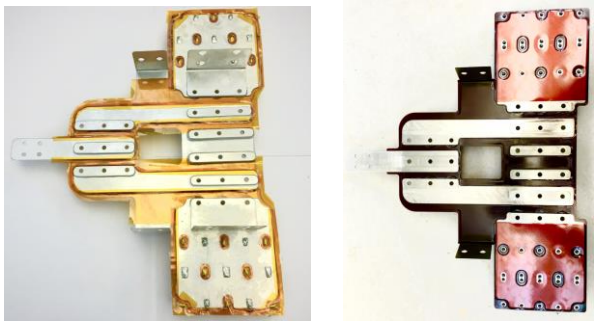


Fig. 18. Simulated EMI noise spectra with different loop inductances and switching speed.



(a) (b)

Fig. 19. Fabricated busbar. (a) Lab prototype. (b) By manufacturer.

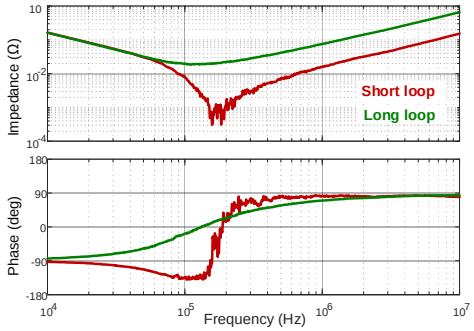
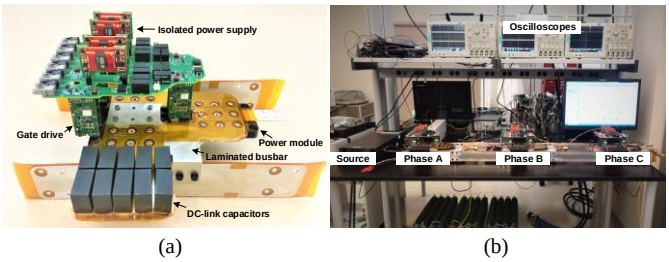


Fig. 20. Measured impedance spectra of busbar.

Fig. 21(a) shows the prototype of a single-phase 3L-ANPC converter equipped with the fabricated busbar. Fig. 21(b) illustrates the testing platform of the three-phase converter. Water-cooled coldplates are utilized for room temperature test. The testing conditions follow the specifications given at the beginning of Section IV. An inductive load is used, and the rated power is 200 kVA.

A continuous power test is conducted to evaluate the function of the converter. Fig. 22 illustrates the tested output current waveforms of the three-phase 3L-ANPC converter. The output current is 292 A, which corresponds to 210 kVA power. There is a little current unbalance among three phases due to the load inductor unbalance and the open loop operation. The maximum measured temperature on the busbar is 41 °C. The highest temperature of the DC-link capacitors is 38 °C, and the temperature difference among the capacitors is within 5 °C.



(a) (b)

Fig. 21. Prototype and testing platform. (a) Single phase-leg prototype. (b) Platform for three-phase testing.

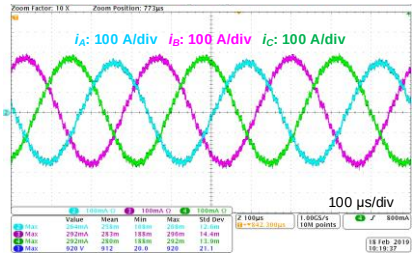


Fig. 22. Tested output current of 3L-ANPC converter at 200 kVA.

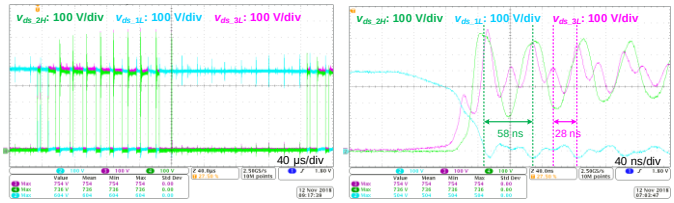
The tested switching transient waveforms are plotted in Fig. 23. The resonant frequencies of the short and long loops are 35.7 MHz and 17.2 MHz, which are very close to the simulation results in Fig. 17. With the low loop inductance, the *dv/dt* of the active switch can be 10 V/ns at full load condition. The peak drain-source voltage of S_{2H} is 736 V and S_{3L} is 754 V, which is lower than the voltage rating of the SiC MOSFET module (900 V). No additional snubber circuit is required in the converter.

Table III compares the loop inductances of the busbar in this paper and those in other NPC type converters. The proposed busbar achieves significantly lower parasitic inductances for both short and long loops.

VI. Conclusions

Based on the loop analysis for three-level (3L) converters with symmetric and asymmetric configurations, a methodology for busbar layout utilizing the magnetic cancellation effect is proposed in this paper. The four-step design procedure can be utilized for most 3L converters. Following the design methodology, a busbar layout example for a 200 kVA 3L ANPC converter with SiC MOSFET power module is demonstrated in detail. Paralleled film capacitors with special placement are adopted to serve as the DC-link capacitors without extra decoupling capacitors.

Different methods including finite element analysis, SPICE circuit model simulation, impedance measurements, and continuous power tests are conducted to verify the performance of the busbar design. The busbar can work properly at 210 kVA output power condition. The parasitic inductances of the short and long loop are 6.5 nH and 17.5 nH, respectively. Compared to the high power NPC type converters in other references, the proposed busbar achieves at least 84% and 77% reduction in short and long loop inductances.



(a) (b)

Fig. 23. Tested waveforms of switching transient. (a) One line cycle. (b) Switching transient.

TABLE III. LOOP INDUCTANCE COMPARISON.

References	Proposed	[3]	[11]	[23]	[24]	[25]	[26]
Power (kVA)	500	1000	200	750	N/A	N/A	475
DC bus (kV)	1	2.4	1.2	2	N/A	N/A	1.1
Short loop (nH)	**6.5**	N/A	55	78	96	47.9	95
Long loop (nH)	**17.5**	115	135	208	150	76.2	118

N/A: Not available

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