A Test Scheme for the Comprehensive Qualification of MMC Submodule Based on 10 kV SiC MOSFETs under High *dv/dt*

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Keywords

«Modular multilevel converter», «MMC submodule», «10 kV SiC MOSFET», «High dv/dt», «Qualification»

Abstract

A test scheme is designed to qualify MMC submodules based on 10 kV SiC MOSFETs comprehensively, including thermal design, insulation design, and operation under high *dv/dt*. In the test scheme, the essential step is the continuous test realized with the proposed ac-dc continuous test circuit with two MMC submodules in series. With the designed modulation scheme, two cascaded submodules are leveraged to generate high *dv/dt*. The submodule under test has to continuously withstand 2X normal *dv/dt* of 10 kV SiC MOSFETs, which could occur during the MMC converter operation. Higher *dv/dt* can also be generated to fully test the submodule. An open loop voltage balancing method is adopted to simplify the continuous test setup. Simulation and experimental results are provided to validate the proposed test scheme.

Introduction

Modular multilevel converter (MMC) has become increasingly more prevalent in various applications, thanks to its numerous benefits [1]-[3]. In medium voltage (MV) applications, especially, MMC has received growing attention, such as MVDC systems [1] and MV converters tied to the distribution grid [2]. The performance of MMC for MV applications can be further improved by the emerging 10 kV SiC MOSFETs. Compared to MMC submodules based on Si IGBTs, MMC submodules equipped with 10 kV SiC MOSFETs feature >10X switching frequency and higher submodule voltage, enabling a wide range of converter-level benefits such as simpler circuit, higher control bandwidth, power density, and efficiency [4]-[9].

The design and testing of MMC submodules are essential to the performance and operation of a MMC. The comprehensive testing and qualification of MMC submodules is necessary to ensure the robust operation of the MMC converter. Also, it is desirable to test submodules comprehensively so that problems can be found at the submodule level before assembling and testing the full converter,

which is much more complex than one submodule. The qualification of MMC submodules based on 10 kV SiC MOSFETs is more crucial, considering the higher submodule voltage and much higher *dv/dt* and hence challenges in both insulation and noise immunity design [10]-[14].

The test scheme for submodules based on 10 kV SiC MOSFETs should be able to provide a condition similar to the real condition in a MMC, such as device current, *dv/dt*, and so on. Specifically, the test scheme should fully validate its thermal performance, insulation design, and the capability to withstand high *dv/dt* when the submodule operates as part of a MMC converter. For example, high *dv/dt* can distort PWM signals and falsely trigger protections, and such issues should be found during submodule testing, instead of during converter testing. Qualification of the gate driver for high voltage SiC devices is studied under high *dv/dt* conditions, however, only the gate driver is tested with a dc-dc continuous test setup [15]. Nevertheless, the testing and qualification of MMC submodules and MV converters based on high voltage SiC MOSFETs or IGBTs has not been covered in detail in previous literature, although experimental results are demonstrated in [5], [8].

This paper focuses on a simple test method to fully qualify a MMC submodule based on 10 kV SiC MOSFETs with half bridge topology. First, the proposed test scheme is introduced in detail, whose essential step is the ac-dc continuous test in which two MMC submodules are connected in series to resemble MMC operation with high *dv/dt*. MMC submodules which pass the qualification testing are able to operate as a robust building block of a MMC. Secondly, an open loop voltage balancing scheme is introduced to balance the voltage of two cascaded submodules. Detailed simulation and experimental results are provided to validate the test method for MMC submodules based on 10 kV SiC MOSFETs, followed by the conclusions of this paper.

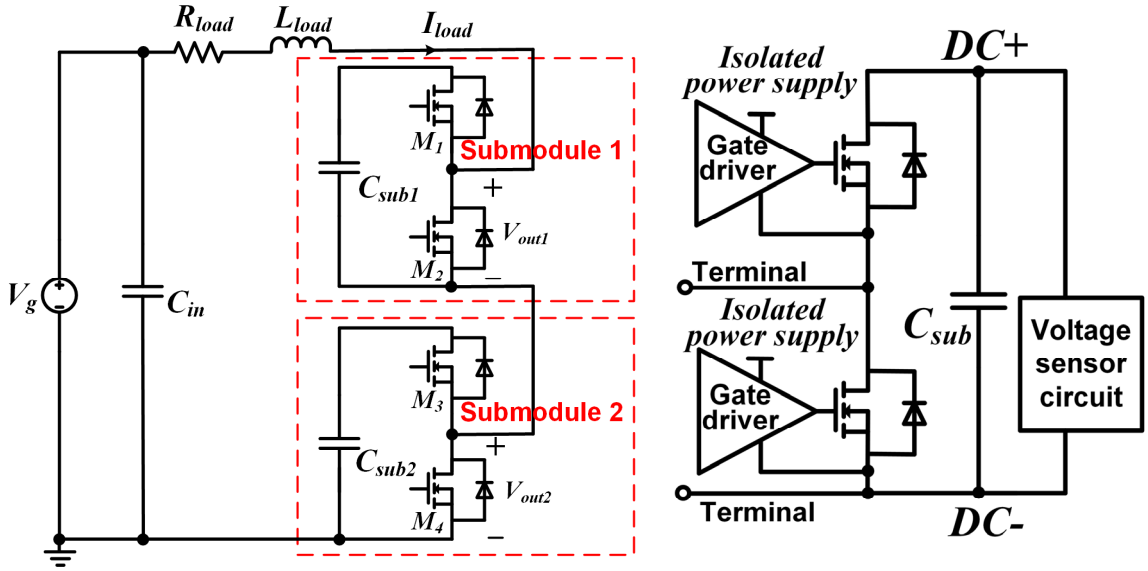
Overview of proposed test scheme

The proposed test scheme for MMC submodules is a simple three-step scheme with the focus on the ac-dc continuous test. The first step is the component qualification and submodule assembly. Then, initial tests are conducted to check the gate loop and gate driver functions. In the first step, components should be tested and qualified individually before the submodule assembly, including gate driver, voltage sensor, MOSFETs, and busbar. After the submodule is assembled, the vital functions of the gate driver are examined, including rising/falling edge of gate-to-source voltage V_{gs}, feedback signal, short circuit protection as well as soft turn-off. The last step is the ac-dc continuous test which should be conducted carefully by starting from low dc-link voltage operation. Compared to the test scheme in [13], the proposed test scheme does not require double pulse test (DPT) and short circuit test for each MOSFET, and hence is much simpler, less time-consuming, and more efficient, which is important when many submodules and converters need to be tested. It is acceptable to skip DPT and short circuit test since the 10 kV/20 A SiC MOSFET and its package in the submodule have become more mature. Meanwhile, more comprehensive tests of the gate driver functions are required in the second step.

Overview of ac-dc continuous test

A proposed ac-dc continuous test circuit with two cascaded submodules is the core of the test scheme, as shown in Fig. 1(a). The proposed ac-dc continuous test circuit has a simple configuration, including a high voltage dc power supply, which is commercially available from various manufacturers, an input capacitor, two MMC submodules, and the load. Two MMC submodules should be connected in the same way as submodules are connected in the MMC. During the normal operation with balanced submodule voltage, the dc component of the submodule voltage is approximately equal to the input voltage V_g. Thereby, the high voltage dc power supply should be able to output the rated dc bus voltage of the MMC submodule. The load can be easily realized with arm inductors of the MMC and a resistive load. R_{load} can be adjusted to obtain the desired active power. Typically, the active power and the value of R_{load} are limited by the output current capability of the dc power supply. MMC submodules with different topologies can be tested with the proposed test circuit. This paper focuses on the testing of MMC submodules with a half bridge topology.

During the ac-dc continuous test, Submodule 1 in Fig. 1(a) is the submodule under test, with high *dv/dt* in its DC- terminal resulting from the switching actions in Submodule 2. Submodule 2 can be regarded as part of the ac-dc continuous test setup. The gate resistance of Submodule 2 can be reduced to further increase *dv/dt* in order to fully test the *dv/dt* immunity of the submodule under test. A fiber optic voltage probe which is able to withstand high common mode voltage can be used to monitor the gate signal, the output signal of the short circuit protection, and other signals, to evaluate the noise immunity under high *dv/dt*. In parallel with the ac-dc continuous test, the thermal design can be evaluated online by measuring device temperature with a fiber optic temperature sensor. Acoustic partial discharge detection method is effective in the online validation of the insulation design of a submodule under PWM voltage with high *dv/dt* [16].



(a) (b)

Fig. 1: (a) Circuit diagram of the proposed ac-dc continuous test circuit for the qualification of MMC submodules. (b) Overview of the MMC submodule with half bridge topology.

Modulation scheme

In the ac-dc continuous test, a modulation scheme is implemented to force the MMC submodule under test to undergo high *dv/dt* that may occur during the MMC converter operation. Cascaded submodules are leveraged to generate high *dv/dt* that is likely to occur in the converter. Bipolar SPWM modulation with the same modulation index is implemented in both Submodule 1 and 2. With zero phase shift between the PWM signals for Submodule 1 and 2, M_1 shares the same gate signal with M_3, and M_2 and M_4 receive the same gate signal.

If Submodule 2 and the submodule under test have the same switching speed and switching frequency, the source of M_1 in Submodule 1 will undergo the voltage rise from 0 to $2V_g$ with 2X normal turn-on *dv/dt* of M_1 as M_1 and M_3 turn on simultaneously. The source potential of M_1 drops from $2V_g$ to 0 with 2X normal turn-off *dv/dt* of M_1, as M_1 shuts off. Such switching actions with 2X normal *dv/dt* could occur in the MMC converter when two submodules in the same arm switch simultaneously. The voltage step change between 0 and $2V_g$ with 2X normal *dv/dt* results in 2X common mode (CM) current flowing through the gate driver and its isolated power supply. Also, the insulation capability of the isolated power supply for the gate driver can be fully tested in this case.

Reducing the gate resistance for MOSFETs in Submodule 2 will further increase the *dv/dt* for the submodule under test, >2X normal *dv/dt* and CM current can be realized. Meanwhile, the DC- terminal of the submodule under test undergoes *dv/dt* higher than the normal *dv/dt* of 10 kV SiC MOSFETs in a MMC. The *dv/dt* that the submodule under test normally experiences in operation can be controlled to be much higher for the purpose of evaluating the noise immunity margin. The noise immunity of the gate driver, especially the short circuit protection and the isolated power supply, can

hence be fully tested. In fact, the high *dv/dt* can influence the normal circuit operation via CM current, radiation noise, and other mechanisms. The submodule under test can be tested and debugged to achieve the capability to handle high *dv/dt*. With such modulation scheme, the ac-dc continuous test setup is a suitable platform to test the submodule's capability to withstand high *dv/dt* during the MMC operation.

The ac-dc continuous test setup has the capability to validate the thermal and insulation design of the MMC submodule under test at the rated dc bus voltage and current. The rated dc bus voltage of the submodule can be realized by increasing V_g. The load voltage is a PWM-type voltage with step changes between V_g and -V_g. Normally the load current has a sinusoidal shape due to the high impedance of the load inductor at high frequency. The magnitude of the load current can be adjusted by changing the modulation index and the fundamental frequency. The peak value of the fundamental component of the load current $I_{fund,pk}$ can be estimated with the equation below.

$$I_{fund,pk} = \frac{mV_g}{2\pi f_{line} L_{load} + R_{load}} \quad (1)$$

In the equation, f_{line} is the fundamental frequency, and m is the modulation index, both of which are determined by the modulation signal. The dc component of the load current $I_{load,DC}$ is determined by the active power consumed in the continuous test setup, which can be calculated with the following equation.

$$I_{load,DC} = \frac{P_{loss} + R_{load} I_{RMS}^2}{V_g} \quad (2)$$

I_{RMS} is the RMS value of the load current, and P_{loss} is the power loss in the ac-dc continuous test setup. If the resistive load is not installed, the load current is almost pure AC current.

Voltage balancing of submodules

Submodule voltage balancing is essential to the ac-dc continuous test circuit with two cascaded MMC submodules. Closed loop submodule voltage balancing control is commonly used in the MMC converter [3], which can also be implemented in the ac-dc continuous test circuit. In order to further simplify the test setup and control, however, an open loop voltage balancing scheme is adopted.

The two cascaded submodules ideally have balanced submodule capacitor voltage, since the two capacitors always have the same current with the designed modulation scheme. In ideal conditions, M_1 and M_3 always conduct at the same time to achieve the natural submodule voltage balancing. In reality, the two submodules could have different dead times due to nonideal factors in the controller and the gate driver board. Also, there could be slight phase shift between V_{gs} of M_1 and M_3, or V_{gs} of M_2 and M_4. For example, the fiber optic transmitter or receiver with the same part number could have different propagation delay. Especially, longer dead time contributes to higher submodule capacitor voltage no matter what the direction of the load current is. Without any voltage balancing method, the voltage of the two submodules would diverge from each other, and the capacitor voltage of the MMC submodule with shorter dead time finally drops to zero. This can be explained by the difference between the average submodule capacitor current of the two submodules, which is named the offset current, I_{offset}. In the dc circuit model in Fig. 2(a), the voltage of the two submodules is marked as ΔV_{sub1} and ΔV_{sub2}, because the initial dc voltage is neglected. The dc voltage difference V_{offset}, defined as $\Delta V_{sub1} - \Delta V_{sub2}$, will continue to increase in magnitude as long as I_{offset} exists due to the different dead time, and the voltage of one submodule will eventually drop to zero.

The magnitude and polarity of I_{offest} is determined by the load current as well as the dead time difference and phase shift between V_{gs} for the MOSFETs of the two submodules. In fact, the magnitude and polarity of I_{offest} can be time-varying. For instance, assuming 20 ns phase shift between V_{gs} for M_1 and M_3 (V_{gs} for M_1 leading) and zero phase shift between V_{gs} for M_2 and M_4, the instantaneous I_{offset} is almost zero when the load current is positive, because M_1 and M_3 are synchronous devices whose body diodes conduct current during the dead time. If the load current is

negative, the phase shift between V_{gs} for M_1 and M_3 will play a part, and the instantaneous $I_{offset}(t)$ can be described with the following equation.

$$I_{offset}(t) = \frac{1}{T_s}\left(\int_{t}^{t+DT_s} I_{load}(t)dt - \int_{t+\Delta t}^{t+\Delta t+DT_s} I_{load}(t)dt\right) \quad (3)$$

In the equation, T_s is the switching period, D is the duty cycle, and Δt is the phase shift. The equation shows that the magnitude and polarity of I_{offset} depend on the instantaneous phase angle of the load current. In fact, it is likely that different dead time and slight phase shift between V_{gs} for M_1 and M_3 as well as between V_{gs} for M_1 and M_3 influence I_{offset} simultaneously. Asa result, the average I_{offset} over a line cycle is not zero in steady state, and hence the voltage balancing cannot be achieved.

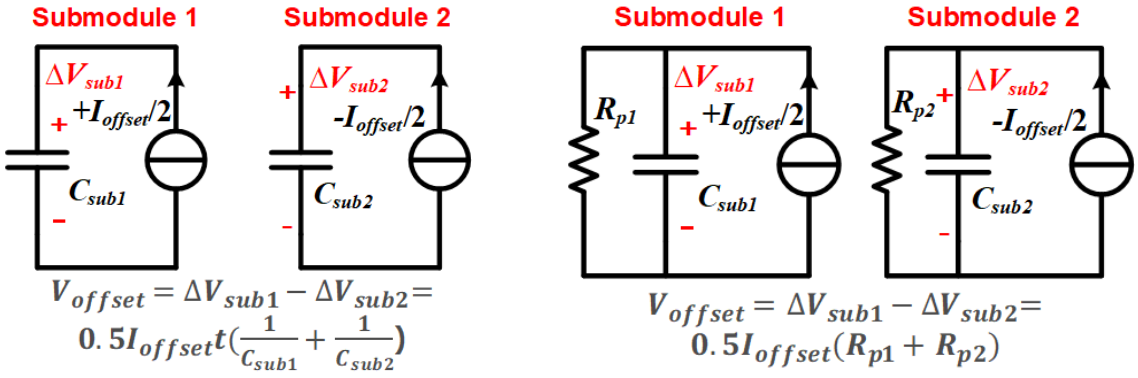


Fig. 2: (a) DC circuit model of the two MMC submodules used to study the submodule voltage difference V_{offset}. (b) DC circuit model of the two MMC submodules after adding a resistor in parallel with the capacitor.

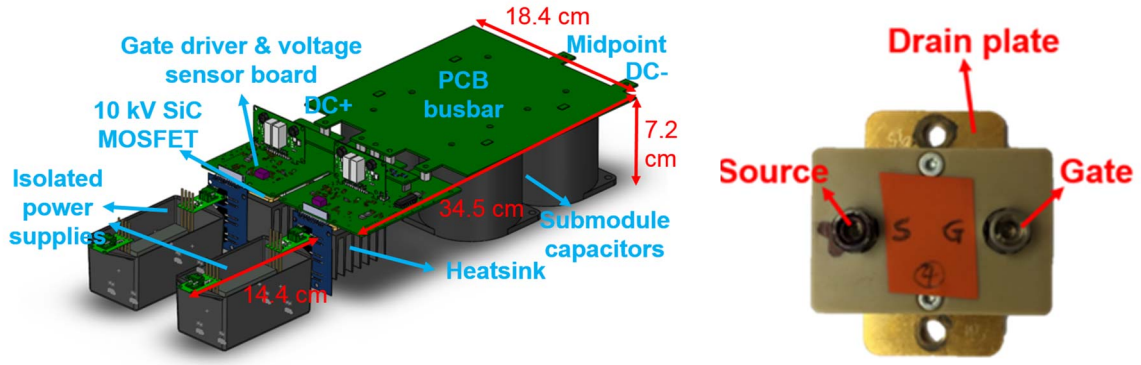
An open loop method with an external parallel resistor is developed to suppress the impact of I_{offset} and achieve voltage balancing. As can be seen in Fig. 2(a), I_{offset} caused by numerous nonideal factors can only flow through the submodule capacitor, and hence keeps charging or discharging the submodule capacitor. After adding a resistor in parallel with the submodule capacitor, as shown in Fig. 2(b), all of the offset current will be absorbed by the resistor, and the submodule capacitor voltage will reach steady state. The dc voltage of the two submodules in steady state still has some difference V_{offest}, whose equation is shown in Fig. 2(b). V_{offest} is only determined by the added parallel resistor and the magnitude of I_{offset} and is independent of the capacitance and parasitics of the submodule capacitor.

It is difficult to calculate the average I_{offset} in a line cycle in an analytical way. However, the average I_{offset} can be obtained easily based on simulation results. The parallel resistor should be selected based on the trade-off between the V_{offest} and the power loss of the resistor. A small parallel resistance is attractive due to better voltage balancing results, yet bulky power resistors must be selected which may also require additional heatsinks or fans and lead to complicated experimental setup. A large parallel resistance results in simple test setup, but the large V_{offset} makes it difficult to control the voltage of the submodule under test in a convenient way, and increases the risk of device damage due to overvoltage.

Simulation results

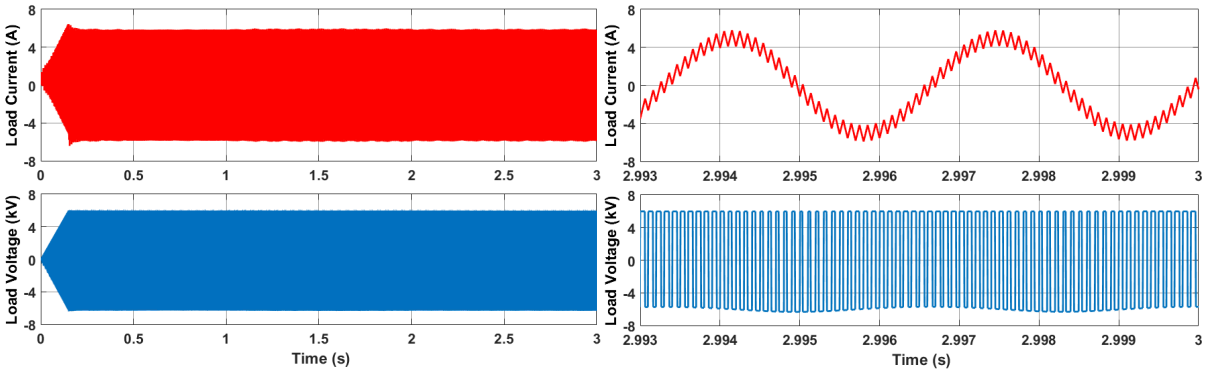
The proposed ac-dc continuous test circuit with the open loop voltage balancing method is simulated in Matlab/Simulink. Parameters in the simulation are obtained from the built MMC submodules based on discrete 10 kV/20 A SiC MOSFETs from Wolfspeed [17] and the test setup which will be introduced in detail in next section. A 3D model of the half bridge submodule is displayed in Fig. 3, together with the 10 kV/20 A SiC MOSFET.

Fig. 4 shows simulation results of the case with zero phase shift between gate signals for the two submodules and 500 ns dead time for both submodules. The submodule voltage is hence perfectly balanced, and the PWM-type load voltage and the load current with sinusoidal shape can be seen in the simulation waveforms. The load current is regulated at ~6 A peak with almost zero DC component, since R_{load} is 1 Ω. In addition, Fig. 5 displays the simulated submodule voltage waveforms without and with the open loop voltage balancing method to prove its effectiveness. The case where two submodules have significantly different dead time is simulated since it provides a large I_{offset}. Without the added parallel resistor, the voltage of Submodule 2 with 100 ns shorter dead time keeps decreasing, and V_{offset} increases rapidly to ~800 V within 3 s. The calculated I_{offset} based on simulation results is 2.4 mA, and the calculated V_{offset} at t=3 s is 782 V based on the equation in Fig. 2(a). Then a relatively small parallel resistor is added in both submodules in order to achieve voltage balancing even faster and reduce computational burden in the simulation. After adding a 100 kΩ resistor, the voltage of two submodules is balanced, and reaches steady state with a constant V_{offset} of ~200 V, close to the calculated 240 V V_{offset}, based on the equation in Fig. 2(b). Like the real MMC operation, the submodule voltage has the line frequency ripple with a peak-to-peak value of ~300 V.



(a) (b)

Fig. 3: (a) 3D model of the built MMC submodule based on 10 kV/20 A SiC MOSFETs. (b) Picture of the 10 kV/20 A SiC MOSFET from Wolfspeed.



(a) (b)

Fig. 4: Simulated waveforms of load voltage and load current at 6 kV dc-link voltage (modulation index m=0.25, R_{load} =1 Ω, L_{load} =175 mH): (a) Overview (V_g ramps up from 0 to 6 kV within 0.15 s); (b) Zoom-in waveforms.

Experimental setup and results

Experimental setup

The proposed ac-dc continuous test circuit is realized with the experimental setup shown in Fig. 6. The high voltage dc power supply from Spellman (Part Number: ST15P12) can output the dc voltage up to 15 kV with the maximum power of 12 kW. The input capacitor C_{in} is implemented with a capacitor bank whose equivalent capacitance is 46.7 μF. The load inductor is implemented with two high

voltage inductors in series with a total inductance of 175 mH, which are also the arm inductors of the MMC. The resistive load is not installed due to the 0.8 A output current limit of the power supply. In fact, in order to reduce the output current ripple of the DC power supply, a 470 Ω resistor is inserted between the DC+ terminal of the power supply and C_{in}, otherwise an overcurrent fault will be reported from the power supply.

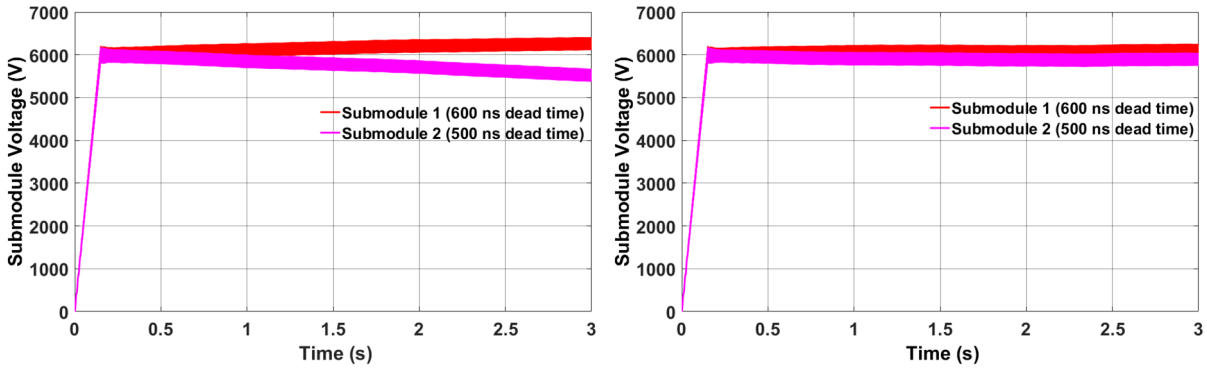


Fig. 5: Simulated submodule voltage waveforms (modulation index m=0.25, V_g= 6 kV, R_{load} =1 Ω, L_{load} =175 mH): (a) Without parallel resistor for voltage balancing; (b) With a 100 kΩ parallel resistor for voltage balancing.

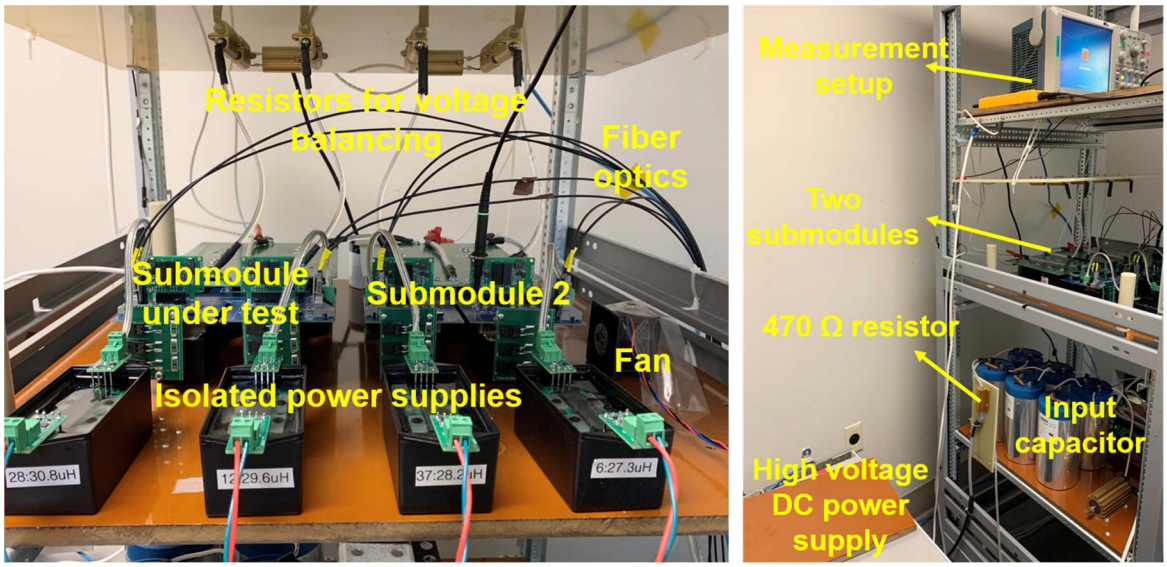


Fig. 6: Experimental setup of the ac-dc continuous test circuit: (a) Zoom-in view of the two cascaded MMC submodules; (b) Overview of the whole test setup (the load inductor is not visible).

Two cascaded MMC submodules are placed next to each other. Each MMC submodule has two 24 V isolated power supplies with 20 kV insulation capability to provide the auxiliary power [18], whose primary side is connected to a 110 V AC power adapter. Each submodule has a 500 kΩ resistor for voltage balancing which is composed of five 100 kΩ resistors (RH050100K0FE02 from Vishay) in series to support the continuous test up to 6 kV V_g. Without any additional heatsinks or fans, the 500 kΩ resistor has a power rating of 100 W, which is 39% higher than its expected power loss at 6 kV. The 500 kΩ resistor can support the test setup even when nonideal factors result in I_{offset} up to 4 mA and the voltage of one submodule up to 7 kV. As shown in Fig. 6, the resistors for voltage balancing are placed on a garolite board.

The cabinet is solidly grounded by connecting it with the grounded case of the high voltage dc power supply to achieve single-point grounding. The DSP controller and human-machine interface (HMI) are far away from the high voltage test setup and isolated via fiber optics. The selected fundamental

frequency is 300 Hz, which is higher than 60 Hz in order to limit the magnitude of the load current. The switching frequency of the 10 kV SiC MOSFETs is 10 kHz.

Experimental results

Experimental results of the ac-dc continuous test at 2.1 kV dc-link voltage are displayed in Fig. 7 and Fig. 8. Before the continuous test, both MMC submodules have passed the first two steps of the test scheme. Both submodules have the same gate resistance: 15 Ω for turn-on, and 3 Ω for turn-off. In terms of the measurement setup, a CWT Ultra Mini Rogowski coil from PEM is adopted for the load current measurement, and two differential voltage probes are used to measure the output voltage of the two submodules. V_{gs} of M_4 is monitored by a low voltage passive probe TPP1000 from Tektronix, whose source is solidly grounded. With a modulation index of 0.45, the sinusoidal load current with 10 kHz ripple has a peak value of ~3 A, which coincides with the estimation result and the simulation result. The low frequency ripple of the submodule voltage is also clearly indicated in Fig. 7.

The submodule voltage is well balanced with the help of the 500 kΩ parallel resistor. The voltage difference between the two submodules V_{offset} is less than 250 V with a dc-link voltage of 2.1 kV. In fact, only one pair of PWM signal is generated in the DSP controller, so the same gate signal is sent to the gate driver of M_1 and M_3 via fiber optics, as well as M_2 and M_4. The voltage difference is mainly attributed to the phase shift between the V_{gs} of M_1 and M_3, and M_2 and M_4, which is due to the propagation delay difference of the components in the gate driver board. According to the zoom-in waveforms in Fig. 8, the output voltage of the two submodules rises and drops almost simultaneously, with a phase shift of <20 ns. It is thereby proved that the designed modulation scheme forces the source of M_1 to undergo 2X *dv/dt* that M_2 and M_3 withstand. The *dv/dt* that M_1 and M_2 of the submodule under test experience continuously will be higher if Submodule 2 is modified to switch with higher *dv/dt*.

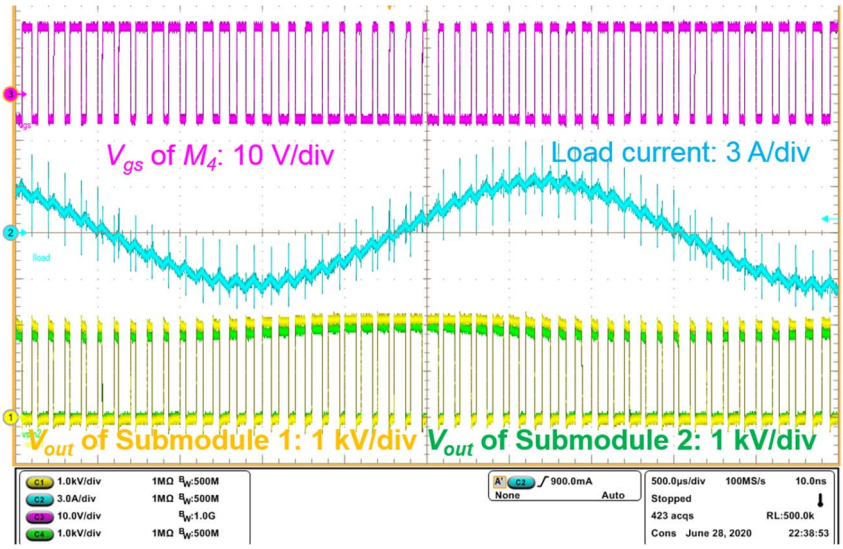
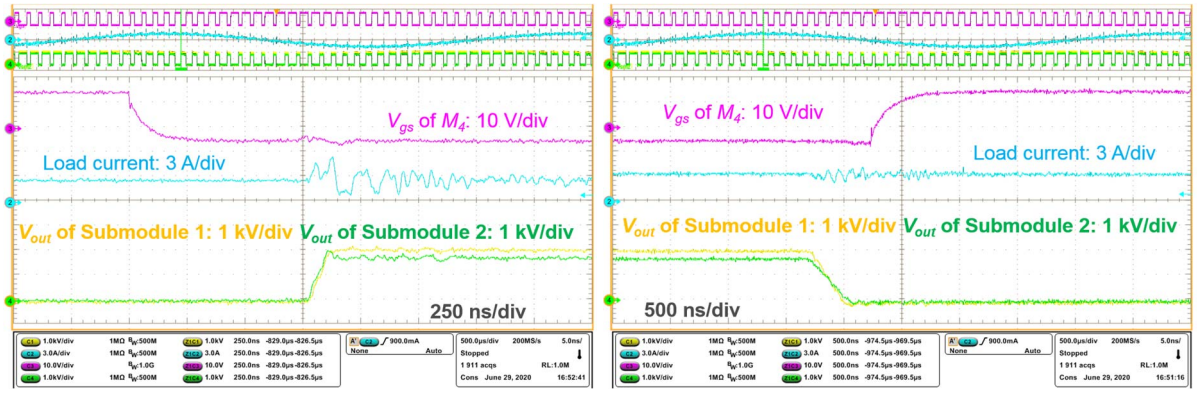


Fig. 7: Waveforms of the continuous test with the proposed ac-dc continuous test circuit at 2.1 kV.

The ac-dc continuous test is successfully conducted at 6 kV dc-link voltage, with the waveforms displayed in Fig. 9. Since the differential voltage probe is not capable of withstanding 6 kV common mode voltage with high *dv/dt*, the output voltage of the submodule under test (Submodule 1) cannot be measured any more. The output voltage of Submodule 2 is measured with a high voltage passive probe, P6015A from Tektronix. At 6 kV, the modulation index is reduced to 0.25 because the continuous operation of the load inductor only allows <9 A peak current. The maximum load current flowing through the inductor and MOSFETs is ~6 A. Because the source of M_1 experiences 2X normal *dv/dt* of the 10 kV SiC MOSFET, substantial displacement current flows through the effective parallel capacitance (EPC) of the load inductor, as clearly indicated in the measured load current waveform.

Measurement results of the output voltage of Submodule 2 show that the capacitor voltage of Submodule 2 varies from 5.1 kV to 5.4 kV. Therefore, it is estimated that the voltage of the submodule under test (Submodule 1) varies from 6.6 kV to 6.9 kV. The proposed open loop voltage balancing method effectively achieves voltage balancing in the ac-dc continuous test setup. With a larger I_{offset} due to the higher load current, the voltage difference V_{offset} is higher than 1 kV. In addition, more accurate submodule voltage measurement results and V_{offset} can be obtained with better high voltage differential voltage probes in the future.



(a) (b)

Fig. 8: Zoom-in waveforms of the continuous test with the proposed ac-dc continuous test circuit at 2.1 kV: (a) Submodule output voltage rises; (b) Submodule output voltage decreases.

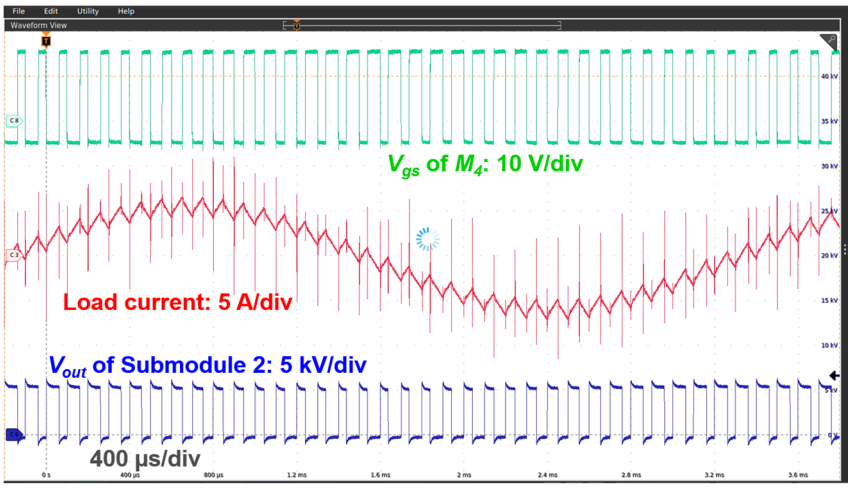


Fig. 9: Waveforms of the continuous test with the proposed ac-dc continuous test circuit at 6 kV.

Conclusions

This paper focuses on a simple test scheme to fully qualify MMC submodules based on 10 kV SiC MOSFETs. The test scheme provides a comprehensive and efficient qualification of the MMC submodule, including its thermal design, insulation design, and its capability to withstand high *dv/dt*. In the test scheme, an ac-dc continuous test circuit with two MMC submodules cascaded in series is developed to qualify the submodules as the final step. With the designed modulation scheme, the submodule under test needs to continuously withstand 2X normal *dv/dt* of 10 kV SiC MOSFETs, which could occur during the operation of a real MMC. In fact, the *dv/dt* that the submodule under test will undergo is controllable so that the capability of the submodule to operate normally under high *dv/dt* can be fully tested. An open loop voltage balancing method with the external parallel resistor is adopted to simplify the test setup. The developed continuous test circuit is fully validated with the built test setup and the ac-dc continuous test up to 6 kV.

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