Analysis and Gate Driver Design Considerations of 10 kV SiC MOSFETs under Flashover Fault due to Insulation Failure

Xingxuan Huang[1], Shiqi Ji[1], Dingrui Li[1], Cheng Nie[1], Leon M. Tolbert[1,2], Fred Wang[1,2], William Giewont[3]

[1]*Min H. Kao Department of Electrical Engineering and Computer Science, The University of Tennessee, Knoxville, TN, USA*

[2]*Oak Ridge National Laboratory, Oak Ridge, TN, USA*

[3]*EPC Power, San Diego, CA, USA*

xhuang36@vols.utk.edu

***Abstract*—The behavior of 10 kV SiC MOSFETs during a flashover fault condition is investigated comprehensively. A larger turn-off gate resistance $R_{g,off}$ is recommended for 10 kV SiC MOSFETs without Kelvin source to avoid very asymmetrical gate resistance, while a small $R_{g,off}$ is recommended for 10 kV SiC MOSFETs with Kelvin source. Guidelines regarding gate loop inductance and selecting an external capacitor across gate and source terminal are also provided. 10 kV SiC MOSFETs have much higher energy loss under flashover fault compared to typical short circuit faults. The required response time for short circuit protection to safely clear flashover fault should be at least 350 ns shorter than the response time designed to clear conventional short circuit faults.**

Keywords—10 kV SiC MOSFET, gate driver design, flashover fault, short circuit protection

I. INTRODUCTION

In recent years, tremendous progress has been made in device design, fabrication, and medium voltage (MV) applications of 10 kV SiC MOSFETs [1]-[8]. Research has demonstrated their superior performance, including low conduction loss, lower switching loss with higher blocking voltage, and hence can operate with >10X higher switching frequency compared to Si IGBTs for MV converters [1]-[7]. At the converter level, 10 kV SiC MOSFETs bring numerous benefits, such as the opportunity to use a simpler and hence more reliable topology and design as well as an overall system level size and weight reduction [7]-[9].

The short circuit performance of 10 kV SiC MOSFETs under hard switching fault (HSF) and fault under load (FUL) has been investigated [10]-[11]. Nonetheless, it is also essential to study the behavior of 10 kV SiC MOSFETs under the flashover fault, the most serious type of short circuit fault in MV converters [12]. In this paper, it is defined that flashover fault happens because protective insulation fails resulting in a shorted component, such as the MOSFET package, the isolated power supply, and the voltage sensor. In fact, flashover fault can be regarded as the most extreme case of FUL fault with exceptionally fast transients.

In MV converters based on 10 kV SiC MOSFETs and other high voltage SiC devices, flashover fault becomes a much more serious issue compared to traditional MV converters, due to high PWM voltage coupled with high switching frequency (>5 kHz) and *dv/dt* (>20 V/ns) [12]-[14]. If partial discharge (PD) is initiated inside the insulation material, the total PD charge and its detrimental impact on the insulation material increases as *dv/dt* and switching frequency become higher, leading to accelerated insulation failure [14] [15]. It is difficult to determine accurately the real partial discharge inception voltage (PDIV) of the insulation material exposed to PWM-type voltage, since a typical PD tester can only output 50/60 Hz sinusoidal voltage, resulting in higher measured PDIV. In practical applications, the real PDIV of the insulation material inside MV converters can be further reduced in harsh operating conditions. Moreover, high *dv/dt* and switching frequency exacerbate the overvoltage and dielectric loss inside insulation material, both of which can also cause the premature insulation breakdown [14] [16]. Therefore, insulation failure and flashover fault are more challenging to tackle in MV converters based on 10 kV SiC MOSFETs.

Flashover fault results in extremely high dv_{ds}/dt (>1 kV/ns) and *di/dt* (>30 A/ns), posing a great threat to the 10 kV SiC MOSFET already in ON state [12]. When flashover fault happens, the 10 kV SiC MOSFET that is already in ON state should be protected from damage, unless the insulation inside its own package fails. However, there is still no detailed analysis of 10 kV SiC MOSFETs and other high voltage SiC devices under the flashover fault, which is necessary for protection design and survival of 10 kV SiC MOSFETs from the flashover fault.

This paper focuses on the analysis of 10 kV SiC MOSFETs under flashover fault to provide guidelines for gate driver design from the perspective of flashover fault. A simplified model of a 10 kV SiC MOSFET is established in Section II, with the focus on its behavior in the active region. Both 10 kV SiC MOSFETs

with and without Kelvin source are analyzed in Section III, in terms of their behavior under the flashover fault, and gate driver design considerations are discussed accordingly in Section IV. Section V compares the energy loss generated by flashover fault and HSF as well as FUL fault and discusses the protection design. Section VI concludes this paper and discusses the future work.

II. Model of 10 kV SiC MOSFET

The 10 kV SiC MOSFET analyzed in this paper is the 3rd generation 10 kV/350 mΩ SiC MOSFET from Wolfspeed [4]. The 10 kV/20 A SiC MOSFET with only one die is studied in this paper as an example. Power modules with higher current rating are realized by paralleling multiple dies with 20 A current rating. The body diode serves as the antiparallel diode [17]. In order to study the behavior of 10 kV SiC MOSFETs under flashover fault, a simplified model of the 10 kV/20 A SiC MOSFET is established. Fig. 1(a) shows the 10 kV/20 A SiC MOSFET and its cross section view, and Fig. 1(b) displays the equivalent circuit of the MOSFET model.

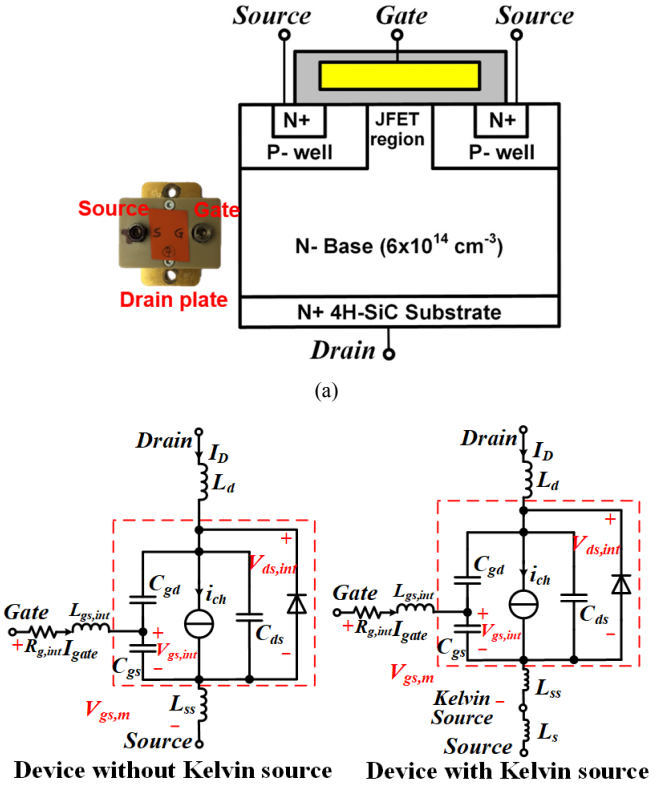


Fig. 1. (a) 3rd gen 10 kV SiC MOSFET from Wolfspeed and its cross section view. (b) Equivalent circuit of the established 10 kV SiC MOSFET model.

The established model of a 10 kV SiC MOSFET is based on the classic quadratic model of MOSFET [18] and the model in [6]. The 10 kV SiC MOSFET model is composed of two parts, which model the bare die and the package, respectively. As shown in Fig. 1(b), components inside the red rectangle are used to model the bare die. The MOSFET channel is modeled with a controlled current source dependent on internal gate voltage $V_{gs,int}$, gate threshold voltage V_{th}, transconductance factor k_p, and internal drain-to-source voltage $V_{ds,int}$. The channel current is always zero when the MOSFET operates in cutoff mode.

$$i_{ch} = 0 \left(V_{gs,int} - V_{th} < 0\right) \tag{1}$$

In the ohmic region, where $V_{gs,int} - V_{th}$ is higher than $V_{ds,int}$, $V_{ds,int}$ increases as channel current rises, which can be described with the following equation.

$$i_{ch} = k_p \left[\left(V_{gs,int} - V_{th}\right) V_{ds,int} - \frac{V_{ds,int}^{\ 2}}{2} \right] \tag{2}$$

As $V_{ds,int}$ keeps increasing and exceeds $V_{gs,int} - V_{th}$, which is still higher than 0 V, the MOSFET operates in the active region, and the channel current will gradually saturate, as described in the equation below.

$$i_{ch} = \frac{k_p}{2} \left(V_{gs,int} - V_{th}\right)^2 \tag{3}$$

Gate threshold voltage V_{th} of the 10 kV SiC MOSFET is a function of junction temperature and $V_{ds,int}$, but it is dominated by $V_{ds,int}$ as $V_{ds,int}$ keeps increasing in the active region due to the short channel effect [19]. Higher $V_{ds,int}$ reduces V_{th} and hence leads to higher saturation current of the channel, based on (3). k_p can be extracted with a curve tracer, and it is almost independent of junction temperature.

In the established model of the MOSFET channel, k_p is 2.02 A/V^2. V_{th} is a function of junction temperature and the internal drain-to-source voltage $V_{ds,int}$. Considering the extremely fast transient during the flashover fault, the junction temperature indeed soars rapidly to eventually over 400 ˚C, so the impact of initial junction temperature before the flashover fault is negligible. The influence of initial junction temperature is hence neglected to simplify the model. As $V_{ds,int}$ increases, the depletion layer becomes thicker leading to decreased V_{th}. Once $V_{ds,int}$ exceeds 4 kV, the depletion layer starts to occupy the N+ substrate region, and its thickness saturates, so V_{th} remains the same as long as $V_{ds,int}$ is higher than 4 kV. According to [11], the saturation current increases with a coefficient of 0.111/kV as $V_{ds,int}$ rises from 500 V to 4000 V. When $V_{ds,int}$ is lower than 500 V, V_{th} is 2.85 V in the model, which is the extracted V_{th} at 125 ˚C. Based on (3) and the saturation current at different $V_{ds,int}$, the gate threshold voltage at different $V_{ds,int}$ from 500 V to 4 kV can be calculated accordingly.

Also, base resistance R_{base} due to the thick N- base region is not considered since it models the N- base resistance when the MOSFET operates in the ohmic region. When the MOSFET stays in the active region, the impact of N- base region is considered by the channel model with short channel effect and the nonlinear C_{ds} model. The body diode is modeled with a resistor in series with its forward voltage drop, based on the measured I-V characteristic.

Parasitic capacitors of the 10 kV SiC MOSFET are also modeled based on extracted data with the curve tracer. Gate-to-source capacitance C_{gs} is modeled with a linear capacitor of 5.4 nF. Both gate-to-drain capacitance C_{gd} and drain-to-source

capacitance C_{ds} are a nonlinear function of the internal drain-to-source voltage $V_{ds,int}$. Both C_{ds} and C_{gd} are realized by a variable capacitor model, which is determined by a look-up table established with the curve tracer data. The look-up table should include as many data points as possible, especially in the highly nonlinear region where C_{gd} and C_{ds} decrease dramatically as $V_{ds,int}$ rises slightly. The parasitic capacitance in parallel with C_{ds} contributed by such external components as heatsinks is not considered in this paper [20].

Internal module parasitics of the MOSFET package should also be carefully modeled. So, the model for the MOSFET with and without Kelvin source is slightly different in Fig. 1. Common source inductance L_{ss} is 1 nH for discrete 10 kV SiC MOSFETs without Kelvin source [6]. With a Kelvin source, L_{ss} can be reduced drastically, and L_s represents the parasitic inductance in the source terminal that is exclusively in the power loop. L_d is the parasitic inductance in the drain terminal. Internal gate resistance $R_{g,int}$ (2 Ω) and internal gate loop inductance $L_{gs,int}$ (1 nH) model the parasitic resistance and inductance in the gate loop inside the device package, which are caused by mechanical connectors, the bond wire, etc. L_d and L_s typically have negligible impact on the short circuit performance of the 10 kV SiC MOSFET, since it only increases the power loop inductance slightly. Nonetheless, L_d, L_s, and L_{ss} result in the difference between the internal drain-to-source voltage $V_{ds,int}$ and the measured drain-to-source voltage $V_{ds,m}$. In fact, L_{ss}, together with $R_{g,int}$ and $L_{gs,int}$ also makes the measured gate-to-source voltage $V_{gs,m}$ different from the internal gate-to-source voltage $V_{gs,int}$.

III. 10 kV SiC MOSFET under Flashover Fault

In this section, the 10 kV SiC MOSFET under flashover fault is analyzed with the circuit model in Fig. 2, which models a typical flashover fault case. The flashover fault happens in a half bridge phase leg, and the low-side MOSFET under investigation is already turned on. In order to model the insulation breakdown, the ideal switch, high-side switch in the phase leg, is shorted and generates the flashover fault. Due to the extremely high *di/dt* in the power loop, common source inductance L_{ss} plays an essential role in the behavior of the 10 kV SiC MOSFET under flashover fault. Therefore, both the 10 kV SiC MOSFET with Kelvin source and without Kelvin source are evaluated in this section.

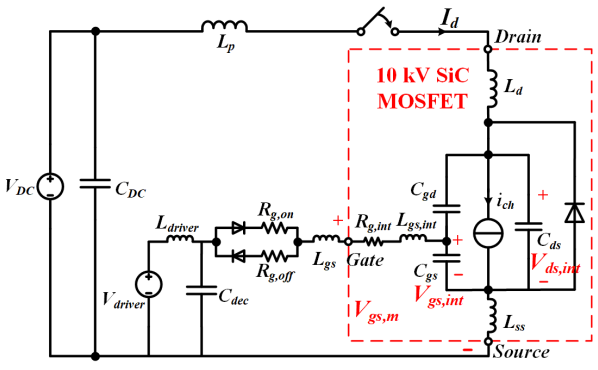


Fig. 2. Circuit model of the 10 kV SiC MOSFET in ON state under flashover fault modeled by closing an ideal switch (device model of the 10 kV SiC MOSFET without Kelvin source used as an example) .

A. Flashover Fault and Simulation Model

The flashover fault is studied using a half bridge phase leg in this paper, because the half bridge phase leg is one of the most common building blocks in MV converters. Flashover fault due to insulation failure in MV voltage converters is devastating because of its extremely fast dynamics. So, the fault is generated by closing an ideal switch in the phase leg, as shown in Fig. 2. Before the fault happens, the ideal switch withstands all of the dc-link voltage, and the 10 kV SiC MOSFET is fully ON with 15 V $V_{gs,int}$. In summary, the circuit in Fig. 2 can effectively model the flashover fault in a real half bridge phase leg based on 10 kV SiC MOFETs.

The simulation model in Fig. 2 is established in PLECS. The phase leg has a power loop inductance L_p of 80 nH and a dc-link capacitance of 8.75 µF. The 10 kV SiC MOSFET gate driver has a gate loop inductance L_{gs} of 5 nH, and the decoupling capacitor C_{dec} is 2.18 µF. V_{driver} is always 15 V in the simulation.

B. 10 kV SiC MOSFET without Kelvin Source

In 10 kV SiC MOSFETs without Kelvin source, the gate loop is heavily influenced by extremely fast voltage and current transients due to flashover fault. High *di/dt* disturbs the gate loop by inducing a high voltage across L_{ss}. Meanwhile, high *dv/dt* and Miller capacitance C_{gd} introduce Miller current. The simulation waveforms at 7 kV are displayed in Fig. 3, in which turn-on gate resistance $R_{g,on}$ and turn-off gate resistance $R_{g,off}$ are 15 Ω and 2.5 Ω, respectively. The fault occurs at t=50 ns.

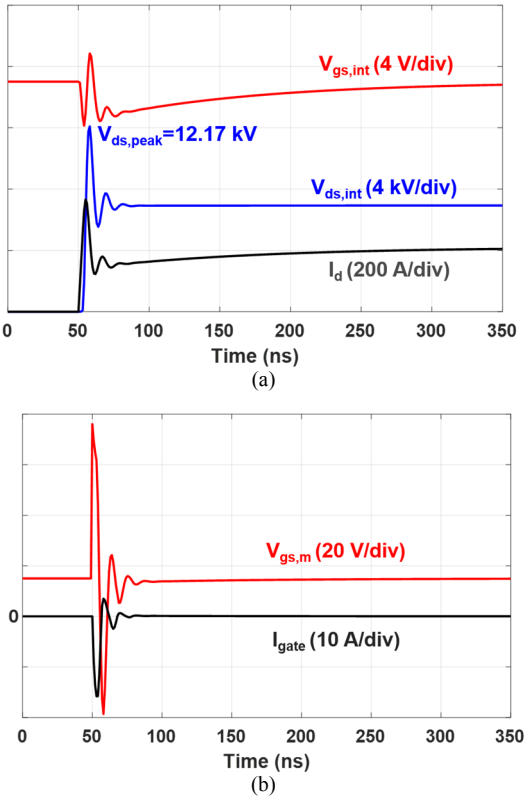


Fig. 3. Simulation waveforms of flashover fault at 7 kV with 1 nH common source inductance L_{ss}, 15 Ω $R_{g,on}$, and 2.5 Ω $R_{g,off}$: (a) Waveforms of $V_{ds,int}$, I_d, and $V_{gs,int}$; (b) Waveforms of $V_{gs,m}$ and gate current I_{gate}.

The high *di/dt* resulting from the flashover fault induces a high positive voltage across L_{ss}, leading to -16.2 A instantaneous gate current I_{gate} and reduced $V_{gs,int}$, as shown in Fig. 3(b). The channel current decreases accordingly. Meanwhile, the drain current is not allowed to change rapidly because of the power loop inductance, hence C_{ds} is effectively charged, leading to high *dv/dt* and a large overshoot in $V_{ds,int}$. $V_{gs,int}$ and drain current effectively decrease as the oscillation continues, since the gate current discharging C_{gs} is higher because the selected $R_{g,off}$ is 1/6 of $R_{g,on}$. After the oscillation ends, it takes around 300 ns for $V_{gs,int}$ to rise back to 15 V, and then the drain current reaches saturation current. In this case, the risk of device damage due to overvoltage is considerable.

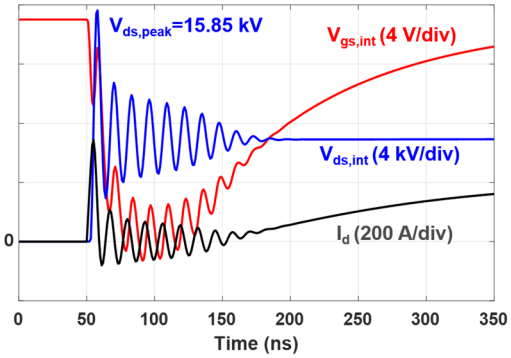
The Miller current from C_{gd} counteracts the effect of voltage across L_{ss} on $V_{gs,int}$ and channel current. With asymmetrical gate resistance, the negative spike of I_{gate} is more substantial than its positive spike, and $V_{gs,int}$ continues decreasing until the oscillation ends. This phenomenon is alleviated by the Miller current. When positive *di/dt* occurs, the voltage drop across L_{ss} generates current to discharge C_{gs}, and meanwhile the Miller current due to the positive *dv/dt* (>1 kV/ns) enters the gate loop and effectively increases $V_{gs,int}$.

In addition, if the asymmetry in gate resistance becomes worse with a smaller $R_{g,off}$, the effect of the voltage across L_{ss} completely dominates. If $R_{g,off}$ is 0 Ω, $V_{gs,int}$ drops rapidly to 0 V within 30 ns once the flashover fault happens, as displayed in Fig. 4(a). The tremendous decline in $V_{gs,int}$ is attributed to the gate current I_{gate} with high negative peaks shown in Fig. 4(b) due to asymmetrical gate resistance. Such "self turn-off" behavior results in smaller short circuit current and energy loss, but the disadvantage is the extremely high peak voltage (15.85 kV) in $V_{ds,int}$. The channel is effectively shut off for a short time, and severe ringing (77 MHz) occurs in $V_{ds,int}$ due to the resonance between the 80 nH L_p and 48 pF C_{ds} (when $V_{ds,int}$ > 3 kV).

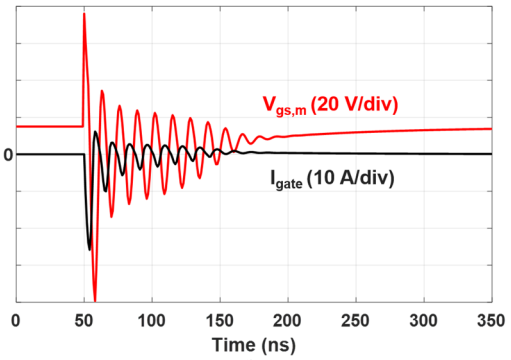
C. 10 kV SiC MOSFET with Kelvin Source

With a Kelvin source in the 10 kV SiC MOSFET, extremely fast transients under the flashover fault are mainly coupled to the gate loop via the Miller capacitance C_{gd}. If L_{ss} is negligible, flashover fault induces positive voltage spike in $V_{gs,int}$ and high device current and energy loss, according to simulation waveforms in Fig. 5. To simulate this case, it is assumed that L_{ss} is 0.15 nH with an 85% reduction compared to the MOSFET without Kelvin source.

With negligible L_{ss}, the significant oscillations in the gate loop and power loop are eliminated. In this case, the extremely high *dv/dt* and the nonlinear Miller capacitance result in the substantial spike in $V_{gs,int}$. $V_{gs,int}$ increases by 45% to 21.8 V with 15 Ω $R_{g,on}$, and 2.5 Ω $R_{g,off}$. The peak drain current is higher than 2X saturation current of the channel (211 A), leading to high short circuit energy loss. On the other hand, the overvoltage in $V_{ds,int}$ is reduced compared to the case without Kelvin source, thanks to increasing $V_{gs,int}$ and channel current in the early stage of flashover fault. The MOSFET damage due to overvoltage is not likely in this case, which is obviously a major concern for the MOSFET without Kelvin source. The device damage due to high energy loss and junction temperature is the concern that should be tackled in gate driver design.

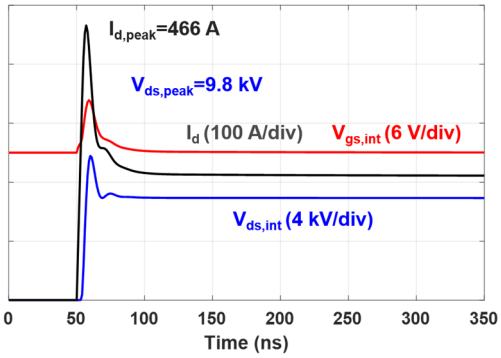


(a)

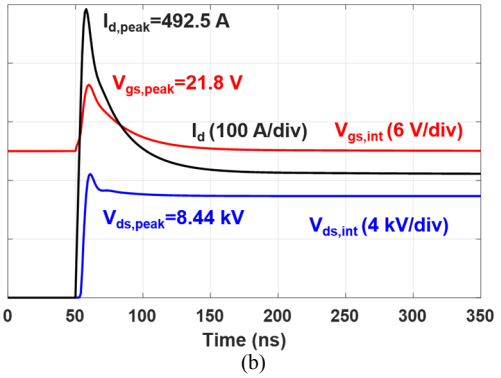


(b)

Fig. 4. Flashover fault simulation results at 7 kV with 1 nH L_{ss}, 15 Ω $R_{g,on}$, and 0 Ω $R_{g,off}$: (a) Waveforms of $V_{ds,int}$, I_d, and $V_{gs,int}$; (b) Waveforms of $V_{gs,m}$ and I_{gate}.



(a)



(b)

Fig. 5. Simulation waveforms of flashover fault at 7 kV with 0.15 nH L_{ss} and 15 Ω $R_{g,on}$: (a) 0 Ω $R_{g,off}$ (b) 2.5 Ω $R_{g,off}$.

IV. Gate Driver Design Considerations

This section discusses how to improve the performance of the 10 kV SiC MOSFET and reduce device damage risk under the flashover fault from the perspective of gate driver design. The design target is to lower peak $V_{ds,int}$ and $I_{d,peak}$ under flashover fault. Gate driver design guidelines are provided for gate resistance selection, gate loop inductance, and whether to add an external capacitor across gate and source terminal. The short circuit energy loss and the impact of flashover fault on short circuit protection design are not covered in this section, since both are investigated in detail in Section V.

A. 10 kV SiC MOSFET without Kelvin Source

Without a Kelvin source available in device package, a relatively high turn-off gate resistance should be selected. The small $R_{g,off}$ and significant asymmetry in gate loop result in reduced $V_{gs,int}$ and substantial voltage overshoot that could damage the MOSFET at the beginning of flashover fault. Such asymmetrical gate resistance should be avoided in the 10 kV SiC MOSFET gate driver. As shown in Fig. 3, Fig. 4, and Fig. 6, as $R_{g,off}$ keeps increasing from 0 Ω to 7.5 Ω (with a 15 Ω $R_{g,on}$), the peak value of $V_{ds,int}$ decreases from 15.85 kV to 9.42 kV. Hence, higher $R_{g,off}$ is preferred to reduce the voltage stress. In fact, increasing $R_{g,off}$ from 0 Ω to 7.5 Ω hardly impacts the turn-off transient of the 10 kV/20 A SiC MOSFET during the normal operation [6].

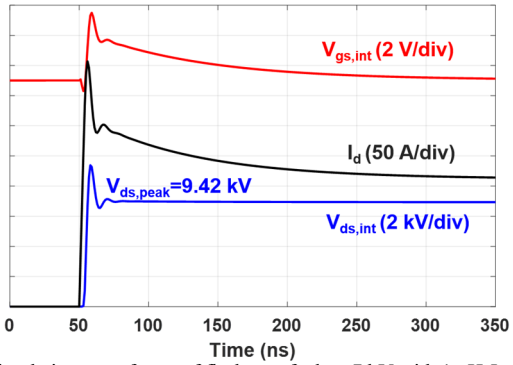


Fig. 6. Simulation waveforms of flashover fault at 7 kV with 1 nH L_{ss}, 15 Ω $R_{g,on}$ and 7.5 Ω $R_{g,off}$.

Adding an external capacitor across gate and source terminal suppresses oscillations in gate loop and reduces voltage overshoot in $V_{ds,int}$ during the flashover fault, as can be seen in Fig. 7. With 15 Ω $R_{g,on}$ and 2.5 Ω $R_{g,off}$, the peak $V_{ds,int}$ reduces from 12.17 kV to 9.46 kV after adding a 500 pF external capacitor between gate and source terminal of the MOSFET. Adding a larger external capacitor is not recommended since the capacitor will result in higher converter switching loss. A smaller capacitor only increases switching loss slightly, yet it will be less effective in reducing the overvoltage of $V_{ds,int}$. Generally, the best solution to suppressing overvoltage in $V_{ds,int}$ is a relatively large $R_{g,off}$ to achieve lower $R_{g,on}/R_{g,off}$, although a small external capacitor is also effective.

In addition, a small gate loop inductance L_{gs} is desirable from the perspective of flashover fault. A large gate loop inductance L_{gs} causes higher $V_{gs,int}$ and device current and energy loss during the flashover fault, since the large impedance of L_{gs} alleviates the asymmetric impedance in the gate loop and hence the effect of L_{ss}. On the other hand, larger L_{gs} strengthens the effect of Miller current, and a larger portion of Miller current flows to C_{gs}. Compared to the case in Fig. 3(a), the peak device current surges from 367 A to 435 A when L_{gs} rises from 5 nH to 30 nH. Hence a large gate loop inductance should be avoided in PCB layout.

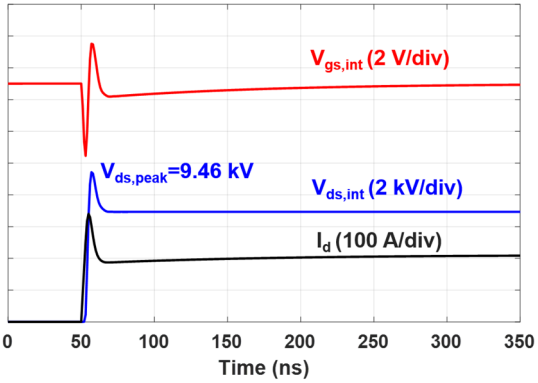


Fig. 7. Simulation waveforms of flashover fault at 7 kV with 1 nH L_{ss}, 15 Ω $R_{g,on}$ and 2.5 Ω $R_{g,off}$ as well as a 500 pF external capacitor.

B. 10 kV SiC MOSFET with Kelvin Source

If L_{ss} is negligible, a smaller turn-off gate resistance and gate loop inductance are preferable to reduce current and energy loss during a flashover fault. To suppress positive voltage spike in $V_{gs,int}$ due to Miller current, it is crucial to reduce the gate loop impedance when the gate current is negative. $R_{g,off}$ as well as L_{gs} thereby should be as small as possible, while $R_{g,on}$ should still be determined by the switching performance during the normal operation. As displayed in Fig. 8, a large $R_{g,off}$ (7.5 Ω) causes 7.9 V spike in $V_{gs,int}$ and 12.2% increase in peak current compared to the case with 0 Ω $R_{g,off}$, and the 523 A peak device current is 2.5X device saturation current, which will be increased further to 539 A with 30 nH L_{gs} due to poor PCB layout.

With negligible L_{ss}, adding an external capacitor across the gate and source terminal is not recommended, which only reduces the peak current slightly. Even with a 1 nF external capacitor, the peak current only drops by 2.9% compared to 492.5 A in Fig. 5(b). Because of 2 Ω $R_{g,int}$ and 1 nH $L_{gs,int}$ inside the device package, it is not likely that a small external capacitor can reduce device current under flashover fault substantially.

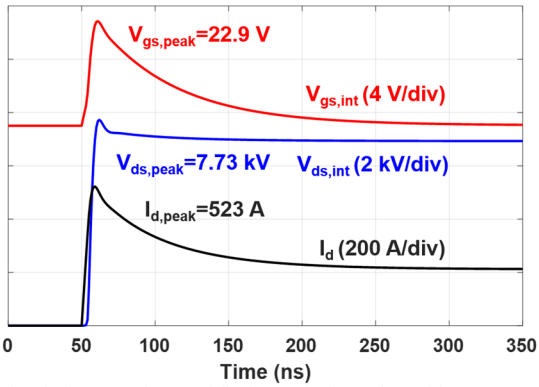


Fig. 8. Simulation waveforms of flashover fault at 7 kV with 0.15 nH L_{ss}, 15 Ω $R_{g,on}$, and 7.5 Ω $R_{g,off}$.

C. Summary

The 10 kV SiC MOSFET gate driver design guidelines are summarized in Table I, whose target is lower device damage risk and better performance under the flashover fault.

TABLE I. SUMMARY OF GATE DRIVER DESIGN GUIDELINES

10 kV SiC MOSFET	w/ Kelvin source	w/o Kelvin source
Gate loop inductance L_{gs}	Reduce L_{gs} in layout	Reduce L_{gs} in layout
Turn-off gate resistance $R_{g,off}$	Select a small $R_{g,off}$	Select a larger $R_{g,off}$ to avoid high $R_{g,on}/R_{g,off}$
External capacitor across gate and source	Adding an external capacitor is not effective	Adding an external capacitor is effective but not recommended

V. SHORT CIRCUIT ENERGY LOSS AND PROTECTION DESIGN

A flashover fault usually generates high energy loss, because $V_{ds,int}$ and I_d soar rapidly to reach dc-link voltage and saturation current, respectively. In this section, the energy loss of the 10 kV SiC MOSFET under flashover fault is investigated quantitatively, which is essential in short circuit protection design. Nonetheless, the response time of short circuit protection is typically determined based on short circuit performance under HSF and FUL fault, instead of flashover fault. As a result, the designed protection may not be fast enough to safely turn off the MOSFET under a flashover fault. A fair comparison between flashover fault and FUL fault as well as HSF fault is made to quantitatively show how much higher energy loss flashover fault produces. Response time required to safely clear flashover fault is provided to guide short circuit protection design.

A. Simulation of FUL Fault and HSF Fault

The same 10 kV SiC MOSFET model in the simulation of flashover fault is adopted in the simulation of FUL fault in order to make a fair comparison. To emulate FUL fault, the ideal switch in Fig. 2 should be replaced by a power semiconductor device with much higher saturation current so that the 10 kV SiC MOSFET eventually withstands complete dc-link voltage during the fault.

When simulating FUL fault, the ideal switch is replaced by a 10 kV SiC MOSFET module composed of three identical 10 kV/20 A dies in parallel. Such implementation ensures sufficiently high saturation current and makes full use of the established 10 kV SiC MOSFET model in Section II. The gate resistance of the 10 kV SiC MOSFET module is selected to ensure fast turn-on process to emulate the short circuit in the load side. The power loop inductance and dc-link capacitance are the same as those in flashover fault simulation.

In the simulation of HSF fault, the ideal switch in the half bridge phase leg in Fig. 2 is completely shorted. C_{DC} and L_p are not changed. The HSF fault occurs once the 10 kV SiC MOSFET is turned on. During the HSF fault, $V_{ds,int}$ remains close to the dc-link voltage, so gate threshold voltage V_{th} is not dominated by $V_{ds,int}$ any more. Instead, V_{th} decreases dramatically as device junction temperature T_j rises rapidly under the HSF fault. V_{th} in the model of the MOSFET channel should hence be modified for more accurate simulation result under the HSF fault. An empirical model of V_{th} as a function of T_j is derived based on the experimental data of the 10 kV/20 A SiC MOSFET under the HSF fault. The nonlinear model of V_{th} is realized with a look-up table in PLECS. The instantaneous T_j during the fault is estimated with the energy loss and thermal capacitance of the drift region of the device, which is 6.4 mJ/K [11]. Other parts of the MOSFET model in Section II remain unchanged to make a fair comparison.

B. Comparison between Flashover and FUL Fault

Common source inductance L_{ss} makes a difference in the behavior of the 10 kV SiC MOSFET under flashover fault. A large L_{ss} reduces $V_{gs,int}$ and device current in the early stage of a flashover fault. However, as displayed in Fig. 9, a large L_{ss} is only able to significantly reduce short circuit energy loss as $R_{g,off}$ approaches zero, inevitably giving rise to huge spike in $V_{ds,int}$ which can damage the MOSFET. Therefore, it is not realistic to take advantage of a large L_{ss} to reduce energy loss during a flashover fault. In summary, if gate resistance is correctly selected to prevent device damage from overvoltage under the flashover fault, common source inductance has little influence on the energy loss during the flashover fault.

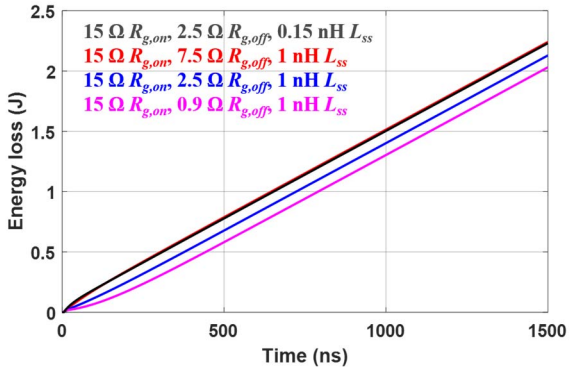


Fig. 9. Short circuit energy loss under flashover fault at 7 kV with different gate resistances and common source inductance.

Simulation waveforms of the 10 kV SiC MOSFET under both flashover and FUL fault at 7 kV are displayed in Fig. 10, both of which last for 1.5 µs. The gate driver for the 10 kV SiC MOSFET with Kelvin source has 15 Ω $R_{g,on,}$ and 2.5 Ω $R_{g,off.}$ Compared to a flashover fault, a FUL fault results in much slower transient. After the FUL fault occurs, it takes 760 ns for $V_{ds,int}$ and I_d to reach their saturation levels. $V_{ds,int}$ rises slowly with an average dv/dt of 13.6 V/ns. In fact, there is a 230 ns delay before $V_{ds,int}$ starts to increase with a high slew rate. The slow transient contributes to lower energy loss under the FUL fault than that under flashover fault, with details shown in Fig. 11. In the first 500 ns, the energy loss under the FUL fault is 0.1 J, while the flashover fault has a 0.77 J energy loss. After 1.5 µs, the flashover fault produces 49.5% higher energy loss than the FUL fault.

With 49.5% higher device energy loss under flashover fault than FUL fault, a shorter response time is required in the short circuit protection design to prevent device damage due to high

energy loss. In fact, after $V_{ds,int}$ and I_d reach steady state, the energy loss difference between FUL and flashover fault is ~0.74 J. The energy loss difference is mainly established in the first 500 ns of the fault. For instance, based on Fig. 11, the energy loss under the flashover fault reaches 1.5 J at t=1 µs, while the energy loss under the FUL fault reaches 1.5 J at t=1.5 µs. From the perspective of critical energy, in order to achieve the same margin, the short circuit response time under flashover fault should be ~500 ns shorter than that under FUL fault.

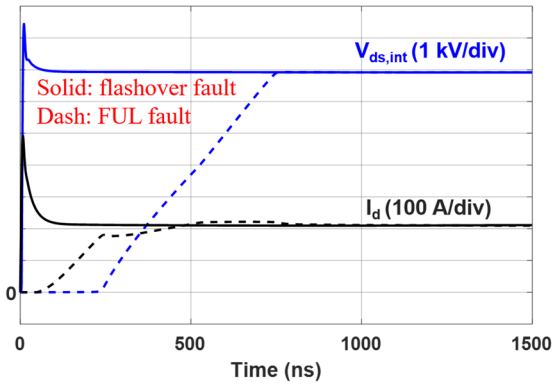


Fig. 10. Simulation waveforms of FUL and flashover fault at 7 kV with 0.15 nH L_{ss}, 15 Ω $R_{g,on,}$ and 2.5 Ω $R_{g,off.}$

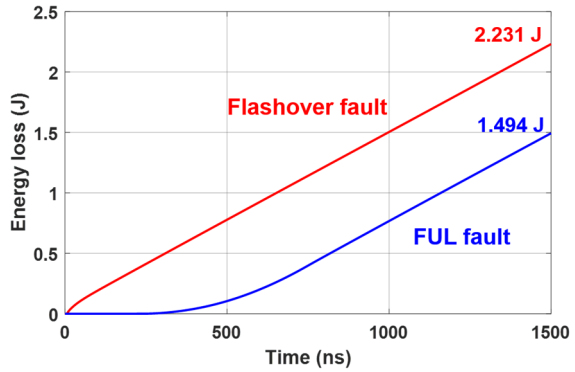


Fig. 11. Short circuit energy loss comparison between FUL and flashover fault at 7 kV with 0.15 nH L_{ss}, 15 Ω $R_{g,on,}$ and 2.5 Ω $R_{g,off.}$

C. Comparison between Flashover Fault and HSF Fault

Similar analysis can be conducted to compare the performance of the 10 kV SiC MOSFET under flashover fault and HSF fault, with details displayed in Fig. 12 and Fig. 13. Under both faults, L_{ss} is 0.15 nH, and the MOSFET is driven with 15 Ω $R_{g,on,}$ and 2.5 Ω $R_{g,off.}$ Fig. 12 displays the typical behavior of the 10 kV SiC MOSFET under HSF fault. $V_{ds,int}$ has a small dip and then climbs back to the dc-link voltage (7 kV) quickly, and the device always operates in the active region.

After 1.5 µs, flashover fault produces 29.5% higher energy loss than HSF fault. The 0.51 J energy loss difference between the two kinds of faults is mainly due to the short circuit current during the first 800 ns. The device current under flashover fault soars immediately with a huge overshoot, while the short circuit current under the HSF fault rises slowly with an average *di/dt* of 0.223 A/ns. After the device current saturates, the instantaneous power loss under the two faults is almost the same.

Based on the simulation result, in order to limit the energy loss to the same level, the short circuit response time under flashover fault should be ~350 ns shorter than that under HSF fault. For example, if 1.5 J critical energy is assumed, the flashover fault should be cleared within 997 ns, and the HSF fault should be cleared within 1.348 µs to guarantee the same margin in short circuit protection.

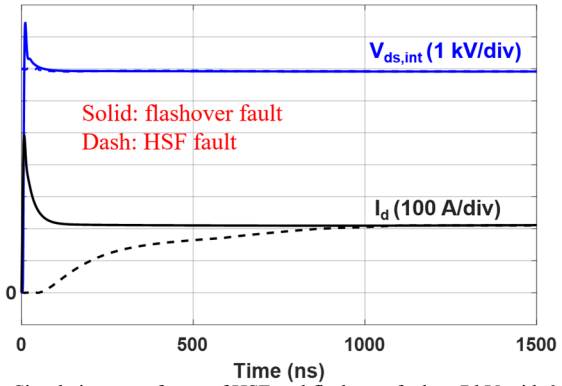


Fig. 12. Simulation waveforms of HSF and flashover fault at 7 kV with 0.15 nH L_{ss}, 15 Ω $R_{g,on,}$ and 2.5 Ω $R_{g,off.}$

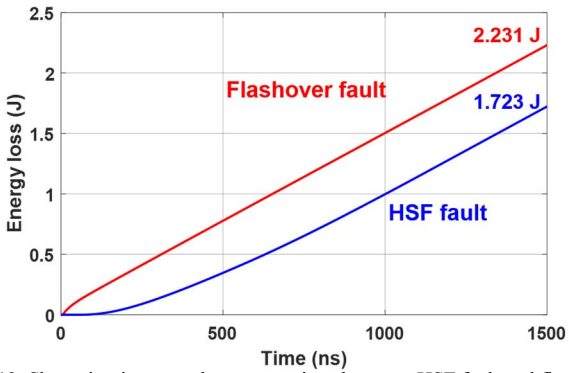


Fig. 13. Short circuit energy loss comparison between HSF fault and flashover fault at 7 kV with 0.15 nH L_{ss}, 15 Ω $R_{g,on,}$ and 2.5 Ω $R_{g,off.}$

VI. Conclusions and Future Work

The 10 kV SiC MOSFET under flashover fault due to insulation failure is analyzed comprehensively, where *dv/dt*, *di/dt*, and energy loss are higher than those under FUL and HSF short circuit fault. Extremely fast transients impact the gate loop via common source inductance and Miller capacitance. Higher $R_{g,off}$ is suggested for 10 kV SiC MOSFETs without Kelvin source to avoid a large $R_{g,on}/R_{g,off}$, while a small $R_{g,off}$ is recommended for the MOSFET with Kelvin source. Design guidelines for gate loop inductance or adding an external capacitor across gate and source terminal are also provided. Short circuit performance under a flashover fault, FUL, and HSF fault is compared, especially the energy loss. With 49.5% higher energy loss under flashover fault, the required response time to clear flashover fault should be ~500 ns shorter than that designed to clear FUL fault. The response time to clear a flashover fault should be ~350 ns shorter than the response time determined by

HSF fault. Future work will include discussion of methods to alleviate the impact of the flashover fault such as a fast V_{gs} clamping circuit, a high voltage test platform for the flashover fault, experimental validation of the analysis based on simulation results, and more discussions based on test results.

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