Noise Immunity of Desat Protection Circuitry for High Voltage SiC MOSFETs with High dv/dt

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***Abstract*—This paper provides an analysis of the desat protection for high voltage (>3.3 kV) SiC MOSFETs from the perspective of noise immunity. The high positive *dv/dt* with long voltage rise time generated by high voltage SiC MOSFETs is identified as a major threat to noise immunity of the desat protection circuitry. The impact of numerous influencing factors is analyzed, such as parasitic inductance, damping resistance, and clamping impedance. In some cases, small parasitic capacitances (<0.01 pF) between the drain terminal with high *dv/dt* and protection circuitry dominate the noise immunity of the desat protection circuitry with high-impedance voltage divider. The noise immunity margin is derived quantitatively to guide the noise immunity improvement. Different noise immunity enhancement methods are developed and validated with experimental results, including adding a shielding layer, reducing clamping impedance, and decreasing voltage divider impedance.**

Keywords—High voltage SiC MOSFETs, gate driver design, desat protection, noise immunity

I. Introduction

High voltage (> 3.3 kV) SiC MOSFETs are promising next-generation switching devices for medium voltage (MV) applications, thanks to their superior characteristics, including high blocking voltage and >10X higher switching frequency than Si IGBTs for MV applications [1]-[8]. However, they also have higher *dv/dt* and insulation voltage requirement, higher current density and lower thermal capacitance, and weaker short circuit withstand capability [6]-[8]. It is also anticipated that high voltage SiC MOSFETs for MV and high-power applications will be more costly. Therefore, the gate driver design for high voltage SiC MOSFETs is challenging and crucial, in which the overcurrent/short circuit protection is an indispensable function [8]-[12].

Among numerous methods developed to protect high voltage SiC MOSFETs from overcurrent/short circuit, desaturation (desat) protection scheme is widely adopted because of its relatively easy implementation to achieve a satisfactory response time for different cases [8]-[11]. When designing the desat protection for high voltage SiC MOSFETs, fast response and high noise immunity often contradict each other. To achieve a better trade-off between these two factors, noise immunity of the desat protection circuitry for high voltage SiC MOSFETs should be analyzed thoroughly, which will also guide the design for future high voltage SiC MOSFETs with higher voltage rating and higher *dv/dt*. Although how to suppress false triggering of desat protection for 1.2 kV SiC MOSFETs with high *dv/dt* has been previously investigated [13], the desat protection circuitry for high voltage SiC MOSFETs is still not clearly understood in terms of noise immunity. High voltage SiC MOSFETs generally experience high *dv/dt* for much longer time than their low voltage counterparts and hence must withstand a much stronger interference from high *dv/dt*.

This paper focuses on the noise immunity of the desat protection for high voltage SiC MOSFETs with high *dv/dt*. Section II introduces the common desat protection circuitry adopted for high voltage SiC MOSFETs. Comprehensive noise immunity analysis and enhancement methods are provided in Section III and IV, respectively, followed by conclusions of this paper.

II. Overview of Desat Protection Circuitry

Desat protection for high voltage SiC MOSFETs can be implemented with circuitry composed of discrete components or a gate driver IC with an integrated desat protection function, as illustrated in Fig. 1. The gate driver IC with desat protection function (MC33153 and FOD8318 from On Semiconductor, STGAP1AS from STMicroelectronics, etc) enables more compact layout, as shown in Fig. 1(b), yet leads to too low threshold current for some high voltage SiC MOSFETs due to its low threshold voltage (<10 V) for desat protection [10], [14], [15]. With a voltage divider and a discrete comparator, desat protection based on discrete components has better flexibility to realize desired performance for high voltage SiC MOSFETs, although the design is more complicated [8], [11]. Also, noise immunity investigation of desat protection based on discrete components will benefit the noise immunity analysis and enhancement of the desat protection realized with gate driver

ICs. Therefore, this paper focuses on desat protection based on discrete components.

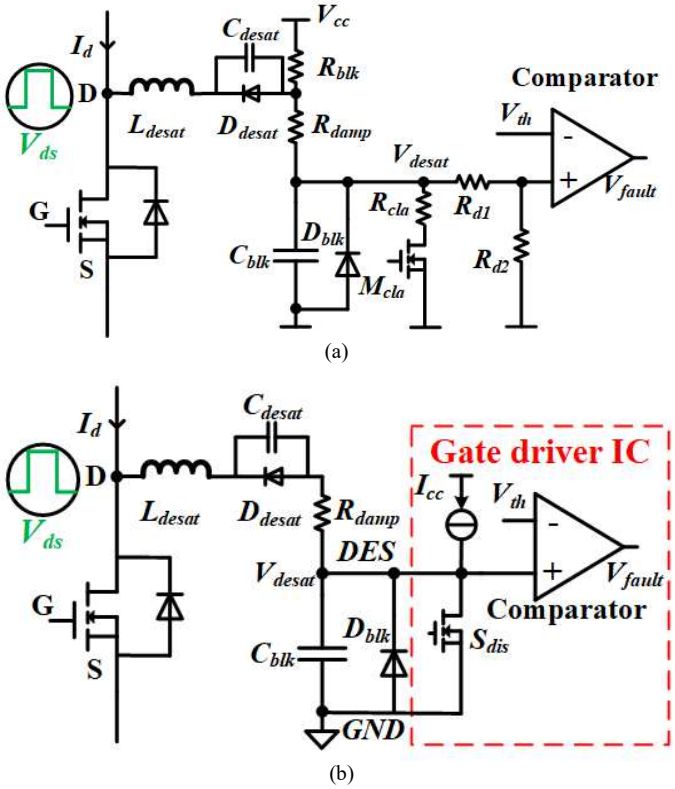


Fig. 1. Two implementations of desat protection for high voltage SiC MOSFETs: (a) Based on discrete components; (b) Realized with gate driver IC.

III. Noise Immunity Analysis

The noise issue and spurious triggering of desat protection are mainly caused by high *dv/dt*, particularly high positive dv_{ds}/dt. High *dv/dt* disturbs the operation of the desat protection circuitry via the parasitic capacitance C_{desat} of the desat diode D_{desat}, as illustrated in Fig. 2 and Fig. 3. The parasitic inductance L_{desat} in series with the desat diode should also be considered. A well-known mechanism of spurious triggering is that the blanking capacitor voltage V_{desat} rises substantially due to the interference of high dv_{ds}/dt [8], [13].

With negative dv_{ds}/dt generated by high voltage SiC MOSFETs, V_{desat} could experience a voltage dip if the displacement current of C_{desat} (100 mA if 2 pF C_{desat} and 50 V/ns *dv/dt* are assumed) is much higher than the current from V_{cc} in Fig. 1(a) and I_{cc} in Fig. 1(b). As shown in Fig. 2, C_{blk} will be discharged to contribute to the displacement current of C_{desat}, and V_{desat} will continue decreasing during the voltage fall time of V_{ds}. Therefore, the negative dv_{ds}/dt does not contribute to the voltage rise in V_{desat} and its impact will not be covered in detail in this paper.

The positive dv_{ds}/dt results in the voltage rise in V_{desat} and hence heavily influences the noise immunity of the protection circuitry. Traditionally, R_{damp} is added to dampen the oscillation, and R_{cla} and M_{cla} are installed to clamp V_{desat} [13]. As illustrated in Fig. 3, R_{cla} and M_{cla} are introduced with the purpose of absorbing the displacement current of C_{desat} due to high positive dv_{ds}/dt, without which V_{desat} will increase dramatically and could lead to spurious triggering. R_{cla} and M_{cla} are necessary if the output voltage of gate driver IC cannot serve as V_{cc} since the required magnitude of V_{cc} is higher than $V_{gs,on}$. This is often the case when designing desat protection for high voltage SiC MOSFETs requiring relatively high threshold voltage.

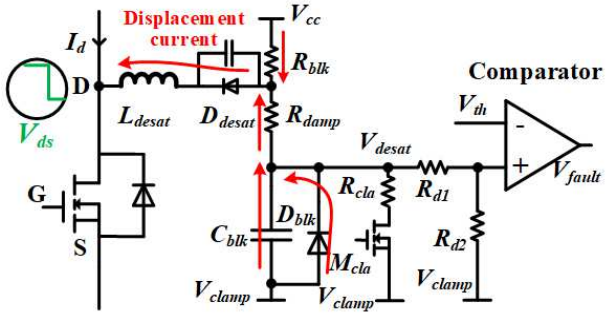


Fig. 2. Displacement current caused by C_{desat} and negative dv_{ds}/dt in desat protection circuitry.

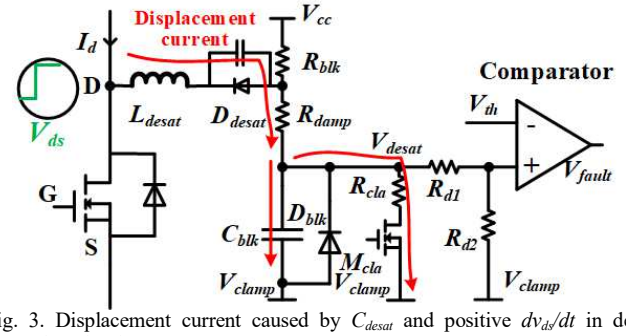


Fig. 3. Displacement current caused by C_{desat} and positive dv_{ds}/dt in desat protection circuitry.

Even with R_{damp}, R_{cla}, and M_{cla}, there will be spikes and oscillations in V_{desat} due to high dv_{ds}/dt, which should be studied when evaluating the noise immunity. As shown in Fig. 4, the desat protection designed for the 10 kV/20 A SiC MOSFET from Wolfspeed is studied as an example in this paper [11], whose simulation model is established in PLECS. Parameters and other details of the desat protection circuitry can be seen in Fig. 4. C_{desat} of the desat diode is nonlinear and decreases rapidly as V_{ds} increases. Meanwhile, the resulting displacement current does not change significantly since dv_{ds}/dt is low when the parasitic capacitance of the desat diode is large. The nonlinear C_{desat} of the diode (three 3.3 kV SiC Schottky diodes in series) is modeled with its equivalent capacitance in terms of charge (2.3 pF) in the simulation [16]. In the simulation, M_{cla} and R_{cla} clamp V_{desat} to V_{clamp} (-5 V) before V_{ds} rises from 0 to 7 kV with a *dv/dt* of 100 V/ns. V_{ds} starts to rise at t=20 ns, and the voltage rise time t_{rise} of V_{ds} is 70 ns.

A. Analysis of Blanking Capacitor Voltage V_{desat}

Simulation waveforms of both V_{desat} and V_{comp} (shown in Fig. 4) are displayed in Fig. 5. The analysis of V_{desat} during the voltage rise time of V_{ds} is presented first, which will benefit the noise immunity analysis of both desat protection based on

discrete components in Fig. 1(a) and desat protection realized with gate driver IC in Fig. 1(b).

V_{desat} goes through oscillations before reaching steady state during the 70 ns voltage rise time. At steady state, the spike of V_{desat} is proportional to R_{cla}, C_{desat}, and dv_{ds}/dt, all of which heavily influence the noise immunity of the desat protection. Thus, achieving a low R_{cla} and C_{desat} can effectively suppress the influence of the high positive dv_{ds}/dt on V_{desat}.

The peak value of V_{desat} is determined by the oscillations at the beginning of the voltage rise time of V_{ds}. According to simulation waveforms in Fig. 5, higher L_{desat} increases the peak value of V_{desat} slightly, which can be attributed to higher quality factor in the resonant circuit. If C_{blk} is reduced to 20 pF for shorter response time, the oscillations caused by high dv_{ds}/dt will become more serious, leading to higher peak in V_{desat}. A larger R_{damp} is effective in suppressing the oscillations and positive spike in V_{desat}, especially when the circuitry has a large L_{desat} and/or a small C_{blk}.

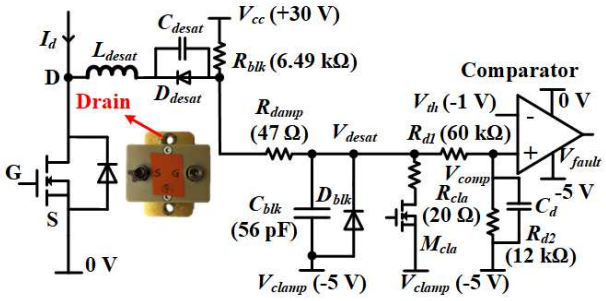


Fig. 4. Desat protection for 10 kV/20 A SiC MOSFET from Wolfspeed.

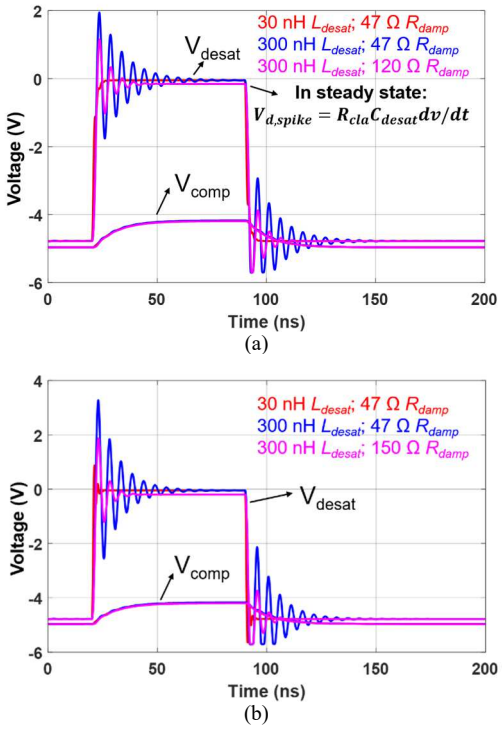


Fig. 5. Simulation waveforms of desat protection for 10 kV/20 A SiC MOSFETs: (a) C_{blk}=56 pF; (b) C_{blk}=20 pF.

The influence of different parameters on the spike of V_{desat} during the voltage rise time of V_{ds} is summarized in Table 1, in which the design recommendations are also provided to reduce the spike and enhance the noise immunity. The analysis of V_{desat} is also beneficial for the desat protection realized with gate driver IC in Fig. 1(b), where the discharge switch S_{dis} can be modeled by R_{cla} when S_{dis} is turned on as the high voltage SiC MOSFET is in OFF state.

TABLE I. SUMMARY OF DESIGN GUIDELINES TO REDUCE SPIKE IN VDESAT DUE TO HIGH POSITIVE DV/DT

Parameter	Recommendation to reduce spike in V_{desat}	Reduce steady-state value of V_{desat} during voltage rise time of V_{ds}?
L_{desat}	Reduce L_{desat}	No
C_{desat}	Reduce C_{desat}	Yes
R_{damp}	R_{damp} should be added	No
C_{blk}	Increase C_{blk}	No
R_{cla}	Reduce R_{cla}	Yes

B. Analysis of Comparator Input Voltage V_{comp}

In the desat protection based on discrete components, V_{comp} should be investigated when evaluating the noise immunity. According to Fig. 5, V_{comp} is hardly impacted by high frequency oscillations in V_{desat}, because the voltage divider and C_d (1 pF in simulation) due to the comparator and PCB layout form an effective low pass filter.

However, parasitic capacitances between the drain terminal and PCB traces or polygons of the protection circuitry should also be considered, which can be calculated with finite element analysis. As drawn in Fig. 6, these parasitic capacitances (< 0.1 pF) are critical due to the high dv/dt with considerable voltage rise time t_{rise} generated by high voltage SiC MOSFETs. C_{p1} and C_{p2} effectively increase the value of C_{desat}. C_{p3} coupled with the voltage divider results in a substantial voltage spike in V_{comp} due to the high impedance of the voltage divider.

To simplify the study, it is assumed that that V_{ds} rises with a constant dv/dt. The displacement current of C_{p3} can hence be modeled by a dc current source I_{p3}. With superposition theorem, V_{comp} in s domain can be calculated with the following equation.

$$V_{comp}(s) = V_{desat}\frac{R_{d2}}{sC_dR_{d1}R_{d2} + R_{d2} + R_{d1}} + I_{p3}\frac{R_{d1}R_{d2}}{sC_dR_{d1}R_{d2} + R_{d1} + R_{d2}} \quad (1)$$

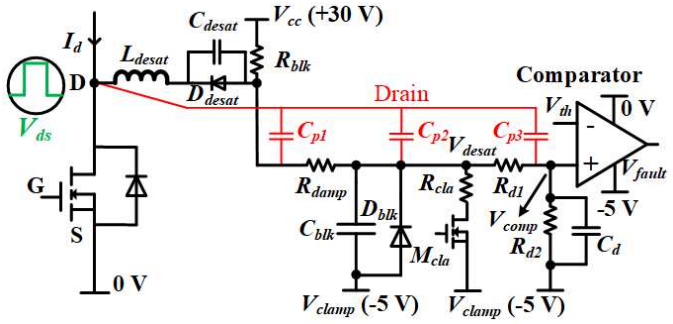


Fig. 6. Desat protection circuitry considering parasitic capacitances between drain and protection circuitry.

In equations in this paper, the reference point of V_{desat} and V_{comp} is V_{clamp} (-5 V), unless their reference point is explicitly noted.

During the voltage rise time t_{rise}, V_{desat} can be modeled as a dc voltage source after neglecting the voltage divider, $R_{blk,}$ and high frequency oscillations in V_{desat}. The peak voltage spike V_{spike} of V_{comp} can be derived with the following two equations, which is the value of $V_{comp}(t)$ at the end of the voltage rise time t_{rise}. The reference point of V_{spike} is also V_{clamp} (-5 V).

$$V_{spike} = V_{comp}(t_{rise}) = (R_{d1}C_{p3} + T)\frac{R_{d2}}{R_{d1}+R_{d2}}\frac{dv}{dt}[1 - e^{\frac{-t_{rise}}{C_d(R_{d1}//R_{d2})}}] \quad (2)$$

$$T = R_{cla}(C_{desat} + C_{p1} + C_{p2}) \quad (3)$$

High *dv/dt* with long voltage rise time generated by high voltage SiC MOSFETs can make the desat protection circuitry vulnerable to noise and spurious triggering. Fig. 7 shows that 0.004 pF C_{p3} induces a sufficiently high spike in V_{comp} to spuriously trigger the protection for 10 kV SiC MOSFETs in Fig. 4, which is 60% higher than that in 1.7 kV SiC MOSFETs with the same *dv/dt* and much shorter t_{rise}. In the simulation, C_{p1}, C_{p2}, and C_{p3} are 0 pF, 0 pF, and 0.004 pF, respectively, and C_{desat} is still modeled with a 2.3 pF capacitor. Fig. 7 also illustrates that the measured V_{spike} in simulation waveforms coincides well with the calculation result based on (2).

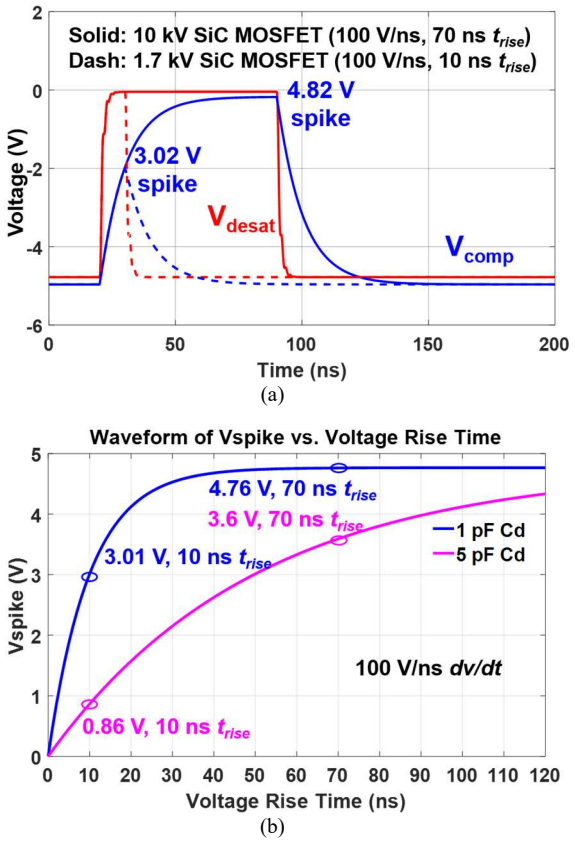


Fig. 7. (a) Simulation results of V_{desat} and V_{comp} with 0.004 pF C_{p3} and 1 pF C_d considered for 10 kV and 1.7 kV SiC MOSFETs with 100 V/ns *dv/dt*; (b) Calculation result of V_{spike} as a function of t_{rise}.

With the established model of V_{spike}, the impact of the voltage rise time t_{rise} can be analyzed quantitively, as plotted in Fig. 7(b). Longer t_{rise} results in higher spike in the comparator input voltage V_{comp}, making the protection more susceptible to spurious triggering. As t_{rise} becomes longer, V_{spike} starts to increase more slowly and eventually saturate. The maximum value of V_{spike} can be expressed as:

$$V_{spike,max} = (R_{d1}C_{p3} + T)\frac{R_{d2}}{R_{d1}+R_{d2}}\frac{dv}{dt} \quad (4)$$

In fact, if $R_{cla}C_{blk}$ is not considerably smaller than t_{rise}, V_{desat} cannot be modeled by a dc voltage source, and the expression of V_{spike} can be modified as follows.

$$V_{spike} = [R_{d1}C_{p3} + T(1 - e^{\frac{-t_{rise}}{C_{blk}R_{cla}}})]\frac{R_{d2}}{R_{d1}+R_{d2}}\frac{dv}{dt}[1 - e^{\frac{-t_{rise}}{C_d(R_{d1}//R_{d2})}}] \quad (5)$$

It should be noted that C_{blk} in the equation is the lumped capacitance between V_{desat} and V_{clamp} (-5 V), including the parasitic capacitance of D_{blk} and M_{cla}.

Based on (5), the magnitude of V_{spike} as a function of voltage rise time and *dv/dt* is evaluated in Fig. 8, in which C_{p1}, C_{p2}, C_{p3}, and C_d are still 0 pF, 0 pF, 0.004 pF, and 1 pF, respectively. In terms of generating high V_{spike} in desat protection circuitry, it is the worst case to have high *dv/dt* and long voltage rise time simultaneously. It is hence concluded that the desat protection of high voltage SiC MOSFETs is more vulnerable to noise caused by *dv/dt*, compared to other power semiconductor devices, including 1.2 and 1.7 kV SiC MOSFETs also with high *dv/dt* and 3.3 kV, 4.5 kV, and 6.5 kV Si IGBTs which are currently dominant in MV applications.

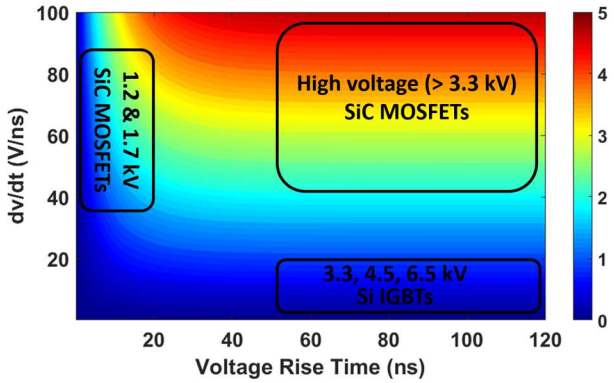


Fig. 8. Contour plot of V_{spike} as a function of *dv/dt* and voltage rise time t_{rise}.

IV. Noise Immunity Enhancement

High positive dv_{ds}/dt with a long t_{rise} leads to a voltage spike in V_{desat} and V_{comp}, although V_{desat} is clamped to V_{clamp} (-5 V in Fig. 4) by a clamping branch. The noise immunity margin V_{margin} in V_{comp} can be estimated as follows.

$$V_{margin} = V_{th} - V_{clamp} - V_{spike} \quad (6)$$

V_{th} is the threshold voltage of the comparator. V_{th}-V_{clamp} is closely coupled with the threshold voltage of desat protection $V_{desat,th}$ and the voltage divider design. The reference point of V_{th} and $V_{desat,th}$ is 0 V. The quantitative analysis is as follows.

$$V_{th} - V_{clamp} = (V_{desat,th} - V_{clamp})\frac{R_{d2}}{R_{d1}+R_{d2}} \quad (7)$$

V_{spike} can be calculated with (2), since high voltage SiC MOSFETs usually have long t_{rise}. Then, the expression of V_{margin} can be rewritten as:

$$V_{margin} = \frac{R_{d2}}{R_{d1}+R_{d2}}[V_{desat,th} - V_{clamp} - T_r\frac{dv}{dt}(1 - e^{\frac{-t_{rise}}{C_d(R_{d1}//R_{d2})}})] \quad (8)$$

$$T_r = R_{d1}C_{p3} + R_{cla}(C_{desat} + C_{p1} + C_{p2}) \quad (9)$$

A. Theoretical Analysis

Noise immunity of the desat protection circuitry can be enhanced by achieving a higher V_{th}-V_{clamp} and reducing V_{spike}. Since $V_{desat,th}$ is completely determined by the output characteristic and threshold current of the MOSFET, increasing $V_{th} - V_{clamp}$ will lead to a higher voltage divider ratio $\frac{R_{d2}}{R_{d1}+R_{d2}}$, and a higher V_{margin}. The selection of comparator should consider its capability of supporting a high V_{th}-V_{clamp}. Hence, comparators with higher power supply voltage V_{cc} can have larger noise immunity margin of desat protection. For example, 5 V comparators are preferable compared to 3.3 V comparators. Also, comparators with high input voltage range are suggested so that V_{th}-V_{clamp} can be as close to power supply voltage V_{cc} of the comparator as possible. By selecting comparators (ADCMP600, TLV3501, etc) which allow input voltage to reach V_{cc}, better noise immunity margin can be realized.

Also, comparators with longer propagation delay contributes to better noise immunity of the desat protection, which will not respond to those extremely short spikes in V_{comp}. Longer propagation delay of the comparator requires V_{comp} to maintain above comparator threshold voltage for a longer time before the comparator output is flipped. The voltage reference used as threshold voltage of the comparator should also be stable and immune from the impact of high *dv/dt*. The selection and design guidelines about the comparator are summarized in Table 2 to improve the noise immunity of the desat protection.

TABLE II. SUMMARY OF SELECTION AND DESIGN GUIDELINES OF COMPARATOR TO ENHANCE NOISE IMMUNITY OF DESAT PROTECTION

Parameter	Selection or design guideline
Power supply voltage	Higher power supply voltage is preferred
Input voltage range	Wider input voltage range is preferred
Propagation delay	Slightly longer propagation delay is preferred; Trade-off: longer delay leads to desat protection with slower response
Threshold voltage	Higher threshold voltage preferred; Filter capacitor added to stabilize threshold voltage

To improve the noise immunity, V_{spike} can be suppressed by reducing R_{cla}, the parasitic capacitances, the voltage divider impedance, and increasing C_d. If R_{cla} is reduced from 20 Ω to 2 Ω in the desat protection design in Fig. 4, V_{spike} is decreased to 4.1 V with 14% reduction. The reduction is not tremendous because the noise immunity margin in this case is dominated by the displacement current from C_{p3}, instead of the displacement current from the desat diode. Therefore, if the voltage divider impedance is reduced by 67%, as shown in Fig. 9, V_{spike} can be reduced from 4.76 V to 2.1 V. If C_{p3} is suppressed to 0.001 pF, V_{spike} will be reduced to 1.8 V. Increasing C_d can also lower V_{spike} and improve the noise immunity. Fig. 7(b) demonstrates that V_{spike} is brought down to 3.6 V with 24% reduction by increasing C_d from 1 pF to 5 pF. Increasing C_d is more effective in noise immunity enhancement when t_{rise} is shorter. When increasing C_d, the trade-off between response time and noise immunity must be considered.

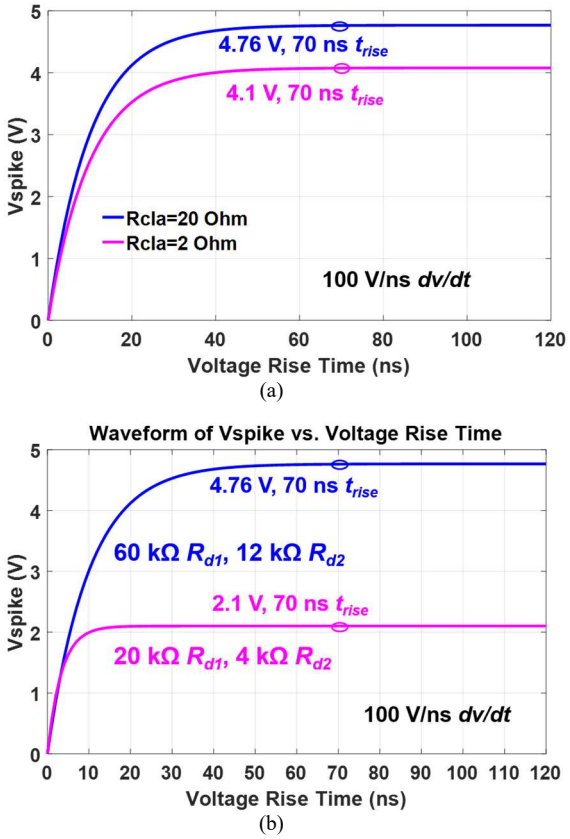


Fig. 9. Calculation result of V_{spike} as a function of t_{rise}: (a) Impact of R_{cla}; (b) Impact of voltage divider impedance.

B. Experimental Validation

Ac-dc continuous test of the half bridge phase leg based on 10 kV SiC MOSFETs is utilized to validate noise immunity enhancement methods of the desat protection designed for the 10 kV SiC MOSFET [17]. Parameters of the desat protection implemented in the phase leg are displayed in Fig. 4. Voltage signals of the desat protection for the lower MOSFET are measured with a 1 GHz TPP1000 probe (3.9 pF input capacitance). 6 kV ac-dc continuous test results in Fig. 10 show that the peak positive spike in V_{comp} is 2.56 V with 1.44 V noise immunity margin. Selecting higher R_{cla} will reduce the noise immunity margin significantly. As shown in Fig. 11, the desat protection for the lower MOSFET is falsely triggered by the positive *dv/dt* (~65 V/ns) during the 6 kV ac-dc continuous test, with R_{cla} increased from 20 Ω to 90 Ω. The measured spike V_{spike} in V_{comp} which falsely triggers the protection is 3.8 V. The equivalent C_d is 5.3 pF with the input capacitance of the passive probe considered. Meanwhile, the measured peak voltage spike in V_{desat} is 11.2 V, which generates a voltage spike of 1.55 V in V_{comp}. The additional 2.25 V voltage spike in V_{comp} is due to the displacement current from C_{p3}.

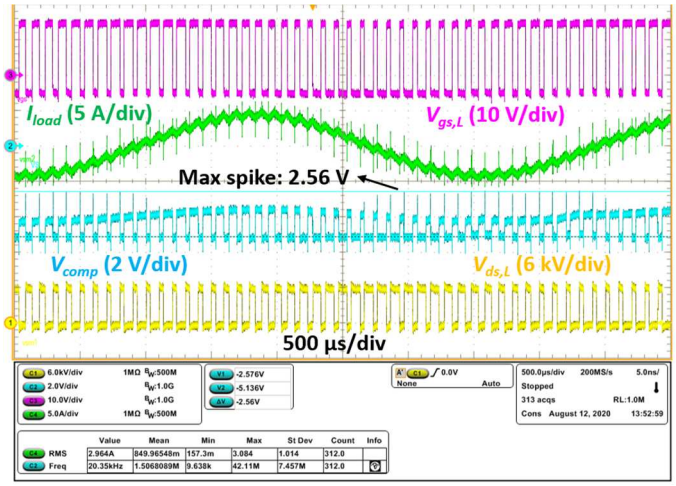
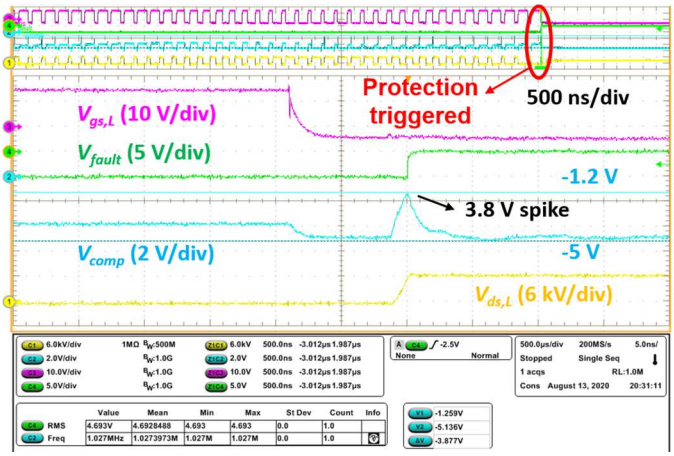


Fig. 10. Waveforms of 6 kV continuous ac-dc test of a phase leg based on 10 kV SiC MOSFETs with desat protection in Fig. 4.

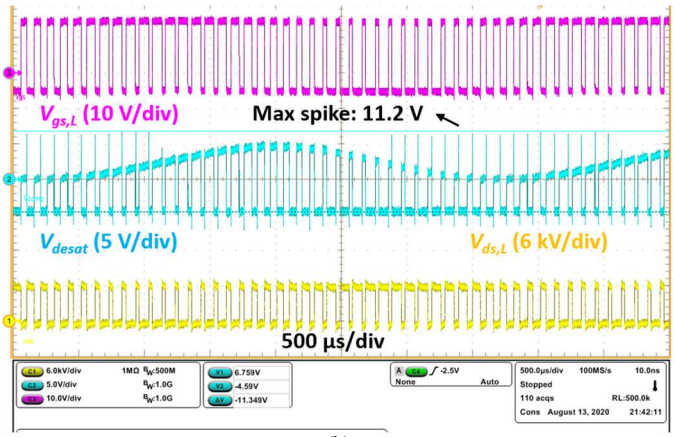
In fact, R_{d1} in the desat protection circuitry shown in Fig. 4 is implemented with two 30 kΩ resistors in series, as illustrated in Fig. 12. Therefore, the drain terminal is coupled with the voltage divider via two parasitic capacitances, $C_{p3,a}$ and $C_{p3,b}$. $C_{p3,a}$ and $C_{p3,b}$ are mainly caused by the large drain plate of the 10 kV SiC MOSFET and the heatsink with the same potential as the drain plate [2], [17], [18], which are included in the simulation model in Ansys Q3D. The finite element analysis in Ansys Q3D reveals that $C_{p3,a}$ and $C_{p3,b}$ are 0.0031 pF and 0.00131 pF, respectively. Based on the analysis in Section III, the additional spike in V_{comp} due to $C_{p3,a}$ and $C_{p3,b}$ can be calculated as 1.54 V, which is slightly lower than the measured result, 2.25 V. The discrepancy is mainly a result of the Ansys Q3D model that does not include all objects in the phase leg which have the same potential as the drain terminal of the 10 kV SiC MOSFET. In other words, the finite element analysis results still underestimate the capacitive coupling between the voltage divider and the drain terminal of the MOSFET.

To suppress the capacitive coupling between the protection circuitry and the drain terminal, an external copper shielding layer connected with the source of the MOSET is installed beneath the desat protection circuitry, since the drain plate of the MOSFET and the heatsink are under the gate driver PCB. Still with 90 Ω R_{cla}, the peak voltage spike in V_{comp} declines from 3.8 V to 2.2 V, and spurious triggering of desat protection is eliminated, as shown in Fig. 13. The role played by $C_{p3,a}$ and $C_{p3,b}$ in the generation of positive voltage spike in V_{comp} is hence proved. It is also proved that shielding is an effective method to suppress the noise propagated to desat protection circuitry via extremely small parasitic capacitances.

Based on the analysis and experimental results, a new iteration of desat protection circuitry is designed to further boost its noise immunity under high *dv/dt*. Several methods are adopted simultaneously in PCB layout and component selection. Compared to the design in Fig. 4, R_{d1} and R_{d2} are reduced by 66.7%. R_{cla} is reduced from 20 Ω to 10 Ω. All components of the desat protection circuitry are placed on top layer of the PCB, and thereby completely shielded by large grounding planes in the inner layers of the PCB. Such PCB design not only tremendously suppresses the influence from parasitic capacitances C_{p1}, C_{p2}, and C_{p3}, but also leads to parasitic capacitance which effectively increases C_d. Further decreasing R_{cla} will benefit the noise immunity margin, but R_{cla} and M_{cla} could be damaged due to high instantaneous current if they are not properly selected.



(a)



(b)

Fig. 11. Waveforms of 6 kV continuous ac-dc test of a phase leg based on 10 kV SiC MOSFETs with 90 Ω R_{cla}. (a) Waveform of V_{comp} when desat protection is falsely triggered. (b) Waveform of V_{desat}.

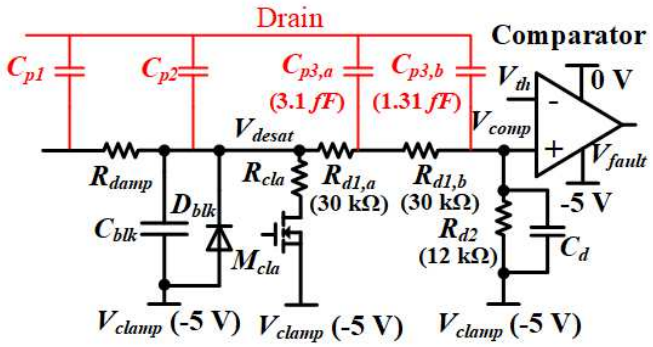


Fig. 12. Details of capacitive coupling between the voltage divider in the desat protection circuitry and the drain terminal of the 10 kV SiC MOSFET.

Ac-dc continuous test results of the new desat protection design in Fig. 14 show that the spike in V_{comp} is almost eliminated. Waveforms captured during a 6 kV ac-dc continuous test prove that spikes in V_{comp} have an amplitude of 0.5 V, with 80% reduction compared to the previous design. The noise immunity margin V_{margin} increases from 1.44 V to 3.5 V. The voltage spike in V_{comp} is mainly caused by the displacement current from the desat diode.

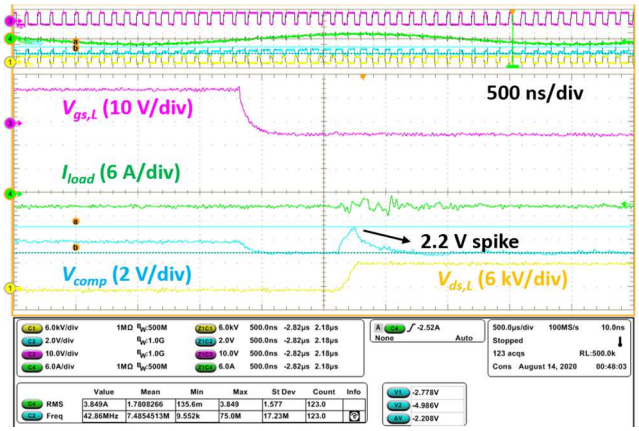


Fig. 13. Waveforms of 6 kV continuous ac-dc test of a phase leg with 90 Ω R_{cla} and an external shielding layer installed.

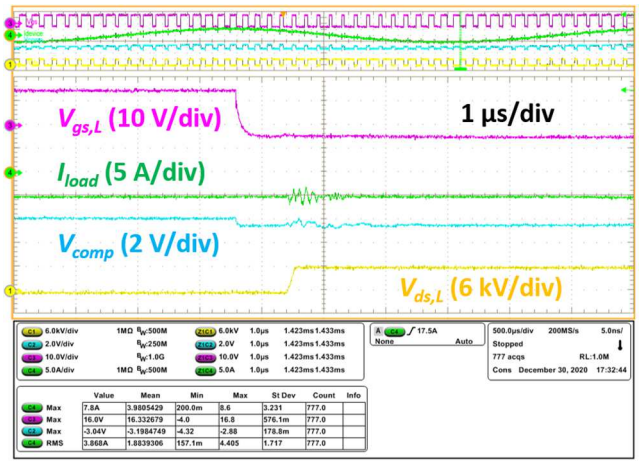


Fig. 14. Waveforms of V_{comp} of new desat protection board with improved noise immunity under 6 kV continuous ac-dc test.

Based on the theoretical analysis and experimental results, design guidelines can be summarized to realize better noise immunity of the desat protection for high voltage SiC MOSFETs. Circuit design guidelines are presented in Table 3, including the design trade-off that should be considered when implementing the guidelines. Some design guidelines in Table 3 can be used to strengthen the noise immunity of both the desat protection based on discrete components and the desat protection realized with gate driver IC.

TABLE III. SUMMARY OF DESIGN GUIDELINES TO ENHANCE NOISE IMMUNITY OF DESAT PROTECTION FOR HIGH VOLTAGE SIC MOSFETS

Design guideline	Detailed guideline	Design trade-off
Reduce C_{desat}	Select or implement desat diode with as low parasitic capacitance as possible	Increasing cost and perhaps size
Reduce L_{desat}	Achieve lower parasitic inductance in PCB layout and connection	Case by case
Add R_{damp}	Use slightly higher R_{damp} if L_{desat} is higher	No considerable trade-off if $R_{damp} << R_{blk}$
Reduce R_{d1}	Reduce voltage divider impedance	Slightly higher loss and slower response
Reduce C_{p1}, C_{p2}, and C_{p3}	Design shielding layer and/or box when doing PCB layout	Slightly slower response due to slightly higher C_d
Increase C_d	Add an external capacitor to increase C_d	Slower response
Reduce R_{cla}	Select a low R_{cla}	R_{cla} and M_{cla} need to handle higher pulse current

V. CONCLUSIONS

Noise immunity of the desat protection for high voltage (>3.3 kV) SiC MOSFETs is comprehensively analyzed in this paper. The main issue is the high positive dv_{ds}/dt, which lasts for a much longer time than that generated by 1.2 kV and 1.7 kV SiC MOSFETs. In addition to the parasitic capacitance of the desat diode, the parasitic capacitance (< 10 fF) coupled with the voltage divider significantly influences the noise immunity of the desat protection circuitry based on discrete components. Other factors' effect on noise immunity is also studied, such as parasitic inductance, voltage divider impedance, damping resistance, and duration of high dv/dt.

The mathematical model of the noise immunity margin is established to support the noise immunity improvement. The noise immunity analysis and improvements are supported by simulation and experimental results, as well as finite element analysis results. Different methods and their experimental validation based on the derived noise immunity margin are presented to enhance the noise immunity. Comprehensive circuit design guidelines to boost noise immunity are summarized, including component selection and PCB layout.

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REFERENCES

[1] J. B. Casady, V. Pala, D. J. Lichtenwalner, E. V. Brunt, B. Hull, G. Wang, J. Richmond, S. T. Allen, D. Grider and J. Palmour, "New generation 10 kV SiC power MOSFET and diodes for industrial applications," in *Proc. of PCIM Europe*, Nuremberg, Germany, 2015, pp. 1-8.

[2] D. Rothmund, T. Guillod, D. Bortis and J. W. Kolar, "99.1 % efficient 10 kV SiC-Based medium voltage ZVS bidirectional single-phase PFC AC/DC stage," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 7, no. 2, pp. 779-797, June 2019.

[3] M. K. Das, C. Capell, D. Grider, S. Leslie, J. Ostop, R. Raju, M. Schutten, J. Nasadoski and A. Hefner, "10 kV, 120 A SiC half H-bridge power MOSFET modules suitable for high frequency, medium voltage applications," in *Proc. of IEEE Energy Conversion Congress and Exposition (ECCE)*, Phoenix, AZ, 2011, pp. 2689-2692.

[4] D. Johannesson, M. Nawaz and K. Ilves, "Assessment of 10 kV, 100 A silicon carbide MOSFET power modules," *IEEE Trans. Power Electron.*, vol. 33, no. 6, pp. 5215-5225, June 2018.

[5] D. Kranzer, J. Thoma, B. Volzer, D. Derix and A. Hensel, "Development of a 10 kV three-phase transformerless inverter with 15 kV silicon carbide MOSFETs for grid stabilization and active filtering of harmonics," in *Proc. of 19th European Conference on Power Electronics and Applications (EPE'17 ECCE Europe)*, Warsaw, 2017, pp. P.1-P.8

[6] S. Ji, Z. Zhang and F. Wang, "Overview of high voltage SiC power semiconductor devices: development and application," *CES Transactions on Electrical Machines and Systems*, vol. 1, no. 3, pp. 254-264, September 2017.

[7] K. Vechalapu, S. Bhattacharya, E. Van Brunt, S. Ryu, D. Grider and J. W. Palmour, "Comparative evaluation of 15-kV SiC MOSFET and 15-kV SiC IGBT for medium voltage converter under the same dv/dt conditions," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 5, no. 1, pp. 469-489, March 2017.

[8] S. Ji, M. Laitinen, X. Huang, J. Sun, W. Giewont, F. Wang and L. M. Tolbert, "Short circuit characterization and protection of 10 kV SiC MOSFET," *IEEE Trans. Power Electron.*, vol. 34, no. 2, pp. 1755-1764, Feb. 2019.

[9] D. N. Dalal et al., "Gate driver with high common mode rejection and self turn-on mitigation for a 10 kV SiC MOSFET enabled MV converter," in *Proc. of 19th European Conference on Power Electronics and Applications (ECCE Europe)*, Warsaw, 2017, pp. P.1-P.10.

[10] Anurag, S. Acharya, Y. Prabowo, G. Gohil and S. Bhattacharya, "Design considerations and development of an innovative gate driver for medium voltage power devices with high dv/dt," *IEEE Trans. Power Electron.*, vol. 34, no. 6, pp. 5256-5267, June 2019.

[11] X. Huang, S. Ji, J. Palmer, L. Zhang, D. Li, F. Wang, L. M. Tolbert, and W. Giewont, "A robust 10 kV SiC MOSFET gate driver with fast overcurrent protection demonstrated in a MMC submodule," in *Proc. of IEEE Applied Power Electronics Conference and Exposition (APEC),* New Orleans, LA, USA, 2020, pp. 1813-1820.

[12] J. Wang, S. Mocevic, Y. Xu, C. DiMarino, R. Burgos and D. Boroyevich, "A high-speed gate driver with PCB-embedded Rogowski switch-current sensor for a 10 kV, 240 A, SiC MOSFET module," in *Proc. of IEEE Energy Conversion Congress and Exposition (ECCE),* Portland, OR, 2018, pp. 5489-5494.

[13] Z. Wang, X. Shi, Y. Xue, L. M. Tolbert, F. Wang and B. J. Blalock, "Design and performance evaluation of overcurrent protection schemes for silicon carbide (SiC) power MOSFETs," *IEEE Trans. Industrial Electron.*, vol. 61, no. 10, pp. 5570-5581, Oct. 2014.

[14] STMicroelectronics, "gapDRIVE: Galvanically isolated single gate driver," STGAP1AS, Datasheet, pp. 1-67, Rev. 3, 2015.

[15] C. DiMarino, J. Wang, R. Burgos and D. Boroyevich, "A high-power-density, high-speed gate driver for a 10 kV SiC MOSFET module," in *Proc. of IEEE Electric Ship Technologies Symposium (ESTS)*, Arlington, VA, 2017, pp. 629-634.

[16] D. Costinett, D. Maksimovic and R. Zane, "Circuit-oriented treatment of nonlinear capacitances in switched-mode power supplies," *IEEE Trans. Power Electron.*, vol. 30, no. 2, pp. 985-995, Feb. 2015.

[17] Xingxuan Huang, "Design and switching performance evaluation of a 10 kV SiC MOSFET based phase leg for medium voltage applications." Master's Thesis, University of Tennessee, 2019.

[18] X. Huang, J. Palmer, S. Ji, L. Zhang, F. Wang, L. M. Tolbert, and W. Giewont, "Design and testing of a modular multilevel converter submodule based on 10 kV SiC MOSFETs," in *Proc. of IEEE Energy Conversion Congress and Exposition (ECCE),* Baltimore, MD, 2019, pp. 1926-1933.