A Novel SPWM-based Common-mode Voltage elimination Modulation Method for Dual Three-phase Motors

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***Abstract*—Common-mode voltage (CMV) is one of the major concerns in modern motor drive techniques. To alleviate the CMV issue, a series of different pulse width modulation (PWM) methods have been proposed, which are particularly effective when the motor phases have even numbers, such as six phases. This paper proposes a new modulation method based on the traditional sinusoidal PWM (SPWM) to fully eliminate the CMV in a dual-three-phase motor drive system, thereby helps the sizing shrinking of the CM choke. Both mathematical models and experiments indicate its effectiveness in the full linearity range of the modulation index. Such a method has been implemented in the field-programmable gate array (FPGA) to widen its control bandwidth.**

Keywords—Modulation technique, common-mode voltage, motor drive)

I. Introduction

Conventional modulation schemes, such as space vector PWM(SVPWM), discontinuous (DPWM), active zero state PWM (AZSPWM) [1] are widely adopted in the three-phase motor drive system. One of the most concerning issues is the common-mode voltage (CMV). These PWMs yield CMV varies between $\pm V_{dc}/6$ or $\pm V_{dc}/2$. Due to the physical limitation of the three-phase two-level inverter, it can never eliminate the CMV. Eqn (1) gives the mathematical expression of CMV in a three-phase system, where V_{an}, V_{bn}, V_{cn} denote the voltage between the phase leg output and the DC-link middle point, and the value can only vary from $\pm V_{dc}/2$. It is impossible to maintain Eqn (1) always zero. Such CMV results in a large CM choke as the must pass CM standards, such as CISPR 25 in electric vehicles, which however adds the weight for the inverter system. As multi-phase motors become popular in the automotive industry [2]-[3], especially for six-phase motors [4]-[5], CMV elimination becomes possible. There's one type of six-phase motors that the neutral points for two sets of three-phase windings are separated with the winding angle difference of 30°. As shown in Fig. 2, such a motor is termed a dual three-phase motor (DTM). DTM shows outstanding advantages over the conventional three-phase motors in terms of reliability, fault tolerance, torque pulsations, and current stress, thereby becoming popular in safety-critical and high-power applications [6]-[11].

Comparing with single neutral point six-phase motor that counts on the classical vector space decomposition [12]-[13] to realize field-oriented control (FOC). A neutral-separated DTM provides more flexibility on the control for each set, therefore simplifying the control complexity on CMV reduction. In addition, Eqn (2) formulates the CMV for a six-phase inverter. As the phases are an even number, there exists the possibility to reduce CMV to zero by imposing $V_{dc}/2$ to half of the pole voltage and $-V_{dc}/2$ to the other half [14]-[15].

$$V_{CM} = (V_{ao} + V_{bo} + V_{co})/3 \quad (1)$$

$$V_{CM} = (V_{ao} + V_{bo} + V_{co} + V_{do} + V_{eo} + V_{fo})/6 \quad (2)$$

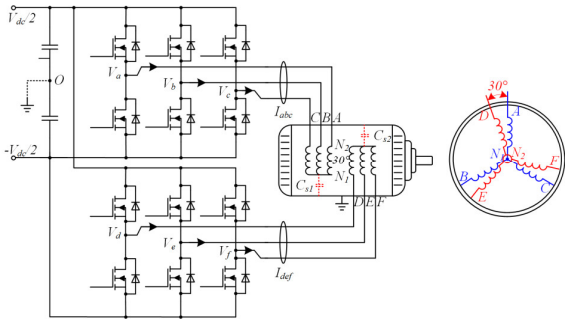

Fig. 1. The winding configuration of the dual-three-phase motor drive system

Taking conventional SPWM (CSPWM) as an example, the PWMs for each phase are center-aligned. As shown in Fig. 2 on the left, the corresponding CMV exhibits a 7-level profile with the peak value equal to $\pm V_{dc}/2$. Every switching action results in a step change of the CMV. A switch-on action

results in $V_{dc}/2$ at the corresponding phase leg output, and a switch-off action generates $-V_{dc}/2$. Most of the time during one switching period, the switch-on and -off actions of two phases cannot happen simultaneously due to the center-aligned modulation. However, when eliminating such constrain, we can shift or split the PWM for all six phases to align each switch-on/off pair while keeping the same duty cycle, which has the chance to eliminate the CMV as the

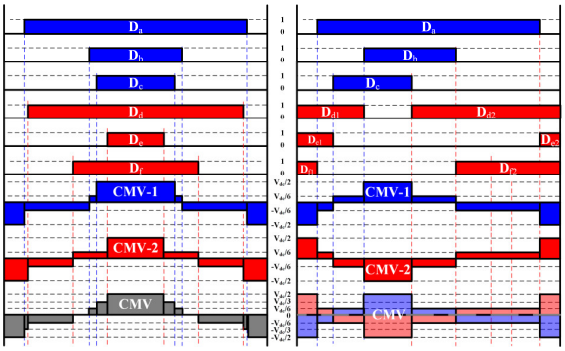

Fig. 2. PWM pattern and CMV for Conventional SPWM (left) and ZCMVM (right system)

$\pm V_{dc}/2$ step-changes neutralize each other. This approach is named zero CMV modulation (ZCMVM), as illustrated in the right plot of Fig.2. Such a pulse shifting mechanism does not change the total number of switching actions in one switching period. Therefore, the switching loss remains the same with SPWM and conventional space vector modulation (CSVM).

This paper focuses on deriving a new modulation method to fully eliminate the CMV for a dual-three-phase motor drive system. Chapter II gives the detailed mathematical model derivation, and Chapter III uses the Simulink model to study the theoretical modulation behavior. In Chapter IV, the experimental result is presented to indicate its effectiveness of CMV elimination. Chapter V is the conclusion and future work.

II. Mathematical Model of ZCMVM

Aligning the switch-on/off edges to cancel the CMV is easy to comprehend. The crucial point is whether this alignment can be applied in the whole switching period and extended to the whole modulation range. Therefore a mathematical model is important. For CSPWM, the duty cycle for each phase can be express as (3), where M is the modulation index, x represents the phase index and θ=0, 2π/3, 4π/3, π/6, 5π/6, 3π/2, for phase A-F, respectively. Note the two winding sets, ABC and DEF have a 30° phase difference.

$$D_x = \frac{1}{2} + \frac{2M}{\pi} cos(\omega t + \theta) \tag{3}$$

To clarify the PWM shift and split rule, we can take Fig. 2 as the reference. Assume the PWM of phase-A follows CSPWM without any shift or split. Angle shifting happens to phase-B/C and pulse splitting happens to phase-D/E/F. After the splitting, the pulses at the beginning of the switching period denote as d1/e1/f1, the pulse at the end of the switching period denotes as d2/e2/f2. Following this, based on Fig. 2, Eqns. (4)-(9) could be derived. The corresponding waveform is then plotted in Fig. 3. If all the switch-on/off pairs can be aligned, De2 must be equal to Df1.

$$D_{f1} = \frac{1-D_a}{2} \tag{4}$$

$$D_{f2} = D_f - D_{f1} \tag{5}$$

$$D_{d1} = 1 - D_b - D_{f2} \tag{6}$$

$$D_{d2} = D_d - D_{d1} \tag{7}$$

$$D_{e1} = 1 - D_c - D_{d2} \tag{8}$$

$$D_{e2} = D_e - D_{e1} \tag{9}$$

By substituting (3) to (4)-(9), the expression of De2 and Df1 could be found as (10).

$$D_{e2} = D_{f1} = \frac{1}{4} - \frac{M}{\pi} cos(\omega t) \tag{10}$$

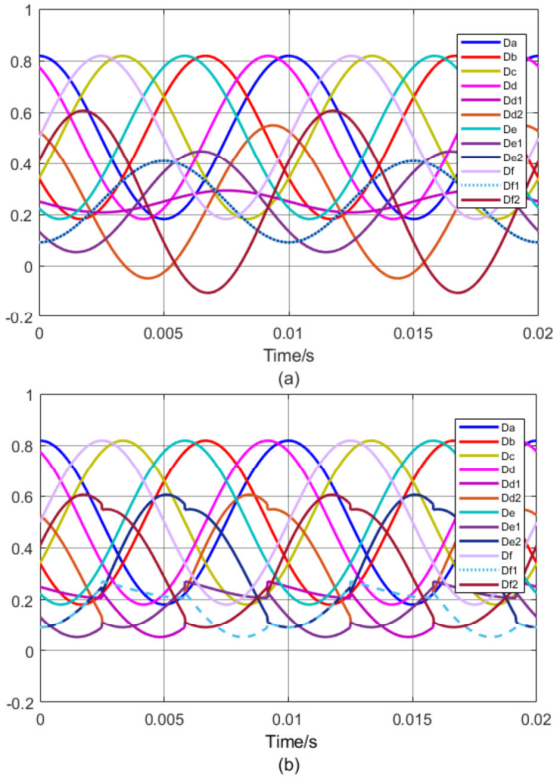

Fig. 3. PWM pattern and CMV for Conventional SPWM (left) and ZCMVM (right system)

This validates that shifting/splitting the PWMs to align all switch-on/off pairs is theoretically feasible regardless of the modulation index M. The challenge is, however, overmodulation happens when the modulation index is too large if such rule still applies. For instance, in Fig.3, the modulation index is 0.5, which is less than the maximum undistorted linearity limit of SPWM (0.785), nevertheless, the overmodulation still happens and cause phase current distortion because some of the modulation waves have negative part (the carrier signal varies from 0 to 1). The root cause is, in some cases, the ZCMV rule will cut the original duty cycle length to force the edges to align. If always fixing Phase-A as the reference phase, as the duty cycle of Phase-B/C becomes too large, the PWM shift will be hard to realize

as there is very limited room to move. Therefore, when the duty cycle of a certain phase is too high or low, the related phase shall not be shifted but fixed at the center of the period, which is termed as the stationary phase. To pick a stationary phase properly, specifying the zone as the indicator is necessary. Fig. 4 then introduces the zone division rule. By solving (11), a fundamental period could be divided into 6 zones by every 60°. The zone and corresponding stationary phase are given in Fig. 4 as well.

$$D_{max} = 1 - D_{min} \tag{11}$$

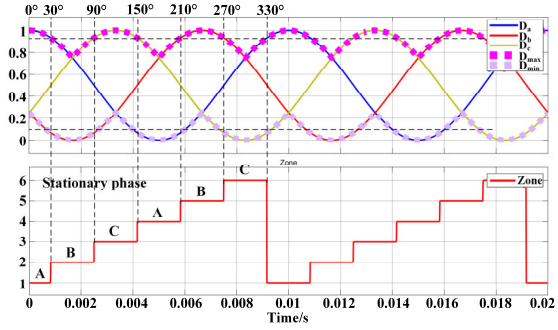

Fig. 4. Zone division.

As the stationary phase varies from zone to zone, the ZCMV requirement also changes. The rule is given in Table. I. Fig. 5 illustrates the PWM manipulation rule in each zone. With such constraints, the negative pulse width could be prevented.

TABLE I. ZCMV RULE

Zone	Stationary phase	ZCMV requirement
1, 4	A	De2 = Df1
2, 5	B	Dd1 = Df2
3, 6	C	De1 = Dd2

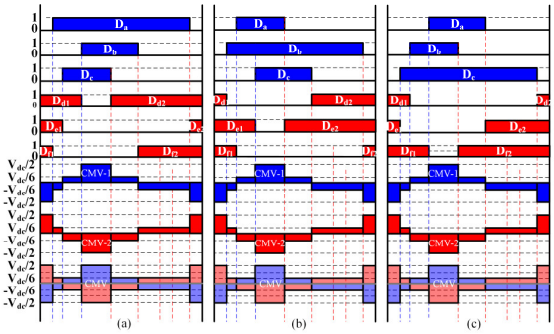

Fig. 5. ZCMVM pulse manipulation rules in different zones: (a) zone-1,4 (b) zone-2, 5 (c) zone-3, 6.

III. SIMULATION RESULT

Generally, to realize the PWM shift and split, changing the carrier wave is the direct method. However, for ZCMVM, the PWM shift/split changes rapidly, causing significant difficulty in carrier wave modification. In this paper, another efficient PWM manipulation method is proposed. As shown in Fig. 6. by calculating the ON/OFF duty cycle for each phase, we can compare it with the carrier and calculate the intermediate part with "AND" logic to obtain the duty cycle. To be specific, when the ON-time value is smaller than the carrier, the output logic-1 is high. When the OFF-time value is lower than the carrier, the output logic-2 is high. Calculate logic-1 AND logic-2, the pulse with desired duty cycle could be obtained. Therefore, by simply moving and splitting the ON/OFF duty-cycle, the PWM manipulation can be realized. The ON/OFF duty cycle equations are given through (12)-(14).

$$D_{on\_x} = \frac{1}{2} - \frac{1}{2}\left(\frac{2M}{\pi} cos(\omega t + \theta) + \frac{1}{2}\right) \tag{12}$$

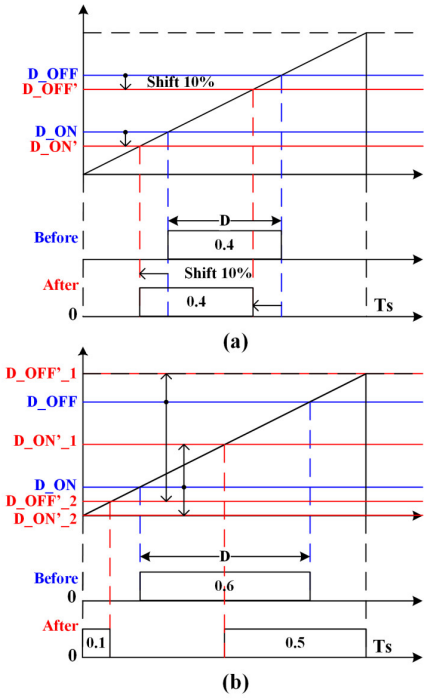

Fig. 6. Pulse manipulation (a) Pulse shifting (b) Pulse splitting.

$$D_{off\_x} = \frac{1}{2} + \frac{1}{2}\left(\frac{2M}{\pi} cos(\omega t + \theta) + \frac{1}{2}\right) \tag{13}$$

$$D_x = D_{off\_x} - D_{on\_x} \tag{14}$$

Such a method is very easy to implement in FPGA as Xilinx provides model-based coding tools for MATLAB Simulink. In the EV domain, the high-resolution microcontrollers, such as FPGAs draw more attention. With their unique parallel computation capability, FPGAs can update the duty cycle in every switching period. Therefore, in this paper, all the control logic is realized through Xilinx System Generator blocks and fixed-point arithmetic with high precision (32-bit) multiplications. As the simulation is finished, the control code is ready as well. Fig. 7 shows the simulation result of CMV at different zones, where the modulation index is 0.3, DC bus voltage is set to 30 V to fit the 48 V motor drive application, switching frequency is 10 kHz, the fundamental frequency is 100 Hz. The CSPWM is also depicted as green dashed line. Note that the dead time is not considered in this simulation. It can be seen that the PWMs for each phase are moved properly and the CMV is eliminated by ZCMVM.

The conventional reduced-CMV PWM method might bring negative impact on the system differential-mode

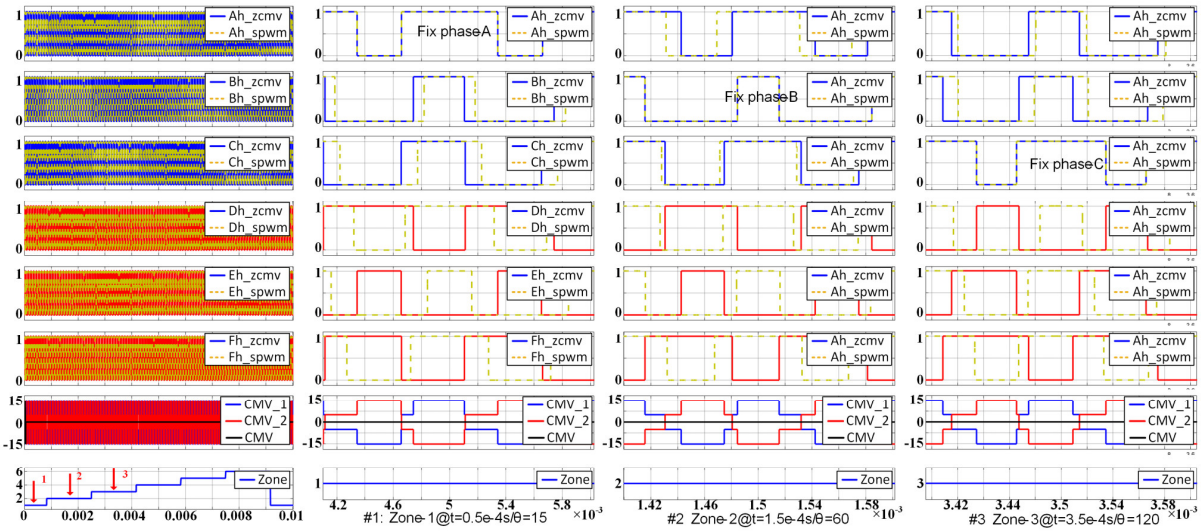

Fig. 7. Simulated CMV with ZRCMVM @M=0.3.

performance. Such as higher output current ripple and THD [16]. To investigate the side effect that ZCMVM brings to the

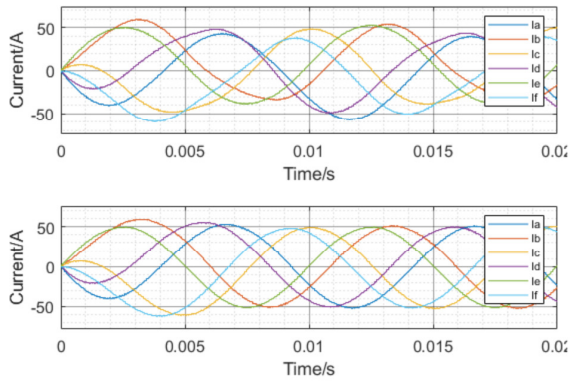

Fig. 8. Phase current waveform simulation result:
without zone division Bottom (top) with zone division (bottom)

system, the differential-mode performance is simulated. Fig. 7 shows the simulation result of CMV at different zones, where the modulation index is 0.3, DC bus voltage is set to 30 V for 48 V motor drive application, switching frequency is 10 kHz, the fundamental frequency is 100 Hz. The PWMs for each phase are moved properly and the CMV is eliminated by ZRCMVM. In the CMV elimination process, the stationary phase changes every 60° to avoid overmodulation happens in the present stage. As a result, the load current distortion is controlled as shown in Fig. 8.

The phase current ripple and THD, which are closely related to the PWM pattern, are also important to be investigated. If the differential-mode performance is strongly sacrificed, not only the harmonic performance will worsen, but also acoustic noise will be caused during the operation. The simulation result on the input/output differential-mode performance is shown in Fig. 9, performed with 30 V DC bus voltage to fit 48V six-phase motor application, 10 kHz switching frequency, and 100 Hz fundamental frequency. Based on the simulation result shown in Fig. 9(a)-(b), the ZCMVM always has a higher ripple in the linearity

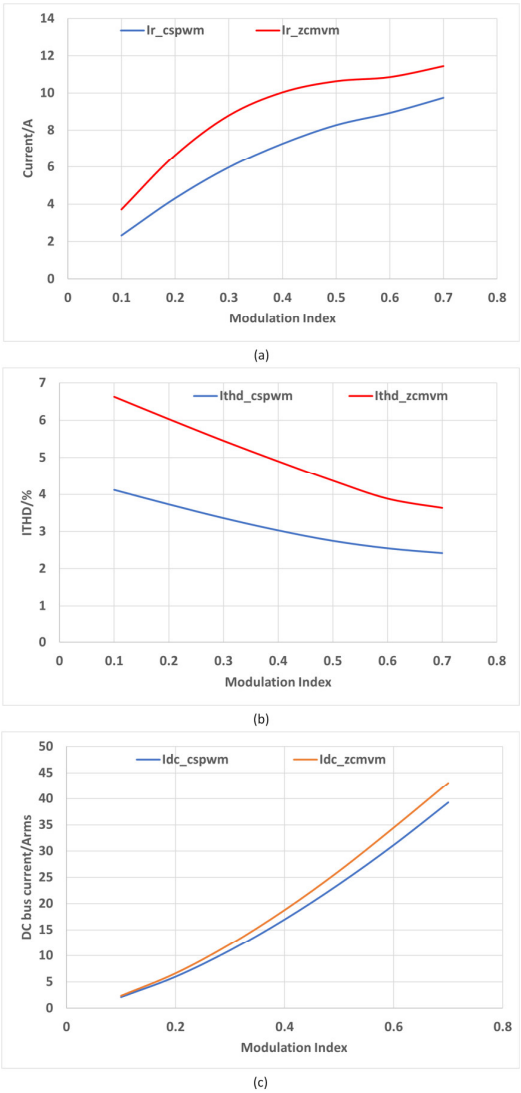

Fig. 9. Differential performance comparison:
(a) Phase current ripple (b) Phase current THD (c) DC-cap current

modulation range than CSPWM. As the modulation index increases, the ripple difference between ZCMVM and CSPWM decreases. In the overmodulation range, the difference is negligible. From the THD perspective, the current THD of ZRCMVM continuously drops as the modulation index increases. The overall gap is narrow and acceptable. On the other hand, the DC-link capacitor current is crucial to DC-link capacitor selection, which strongly affects the system size. Fig. 9(c) shows the simulation result of the DC-link capacitor current for CSPWM and ZCMVM. The DC-link capacitor current of ZCMVM, though always larger than CSPWM, still show a similar curve to CSPWM with a maximum difference of around 3.5 A. Such a small difference has very few impacts on the capacitor selection

IV. Experimental Result

As shown in Fig. 10, two FPGA-controlled SiC inverters are designed to set up a six-phase motor drive test bench. The motor is 48 V/10 kW rated with two separated neutral points. The detailed test bench parameters are listed in Table. II. The whole system sits on a grounded copper plate based on EMI measurement criteria.

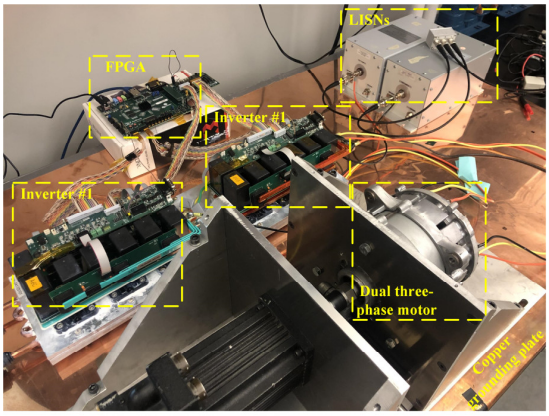

Fig. 10. Test bench with CM EMI measurement equipments.

TABLE II. Test Bench Parameters

Item	Value	Unit
DC bus voltage	30	V
Phase current (RMS)	25	A
Switching frequency (fs)	10	kHz
Fundamental frequency (f0)	100	Hz

The CMV waveform is measured and shown in Fig. 11. The CMV1 and CMV2 represent the CMV on each set of three-phase systems. According to the proposed CMV reduction strategy, for MI<0.785, the waveform of CMV1 and CMV2 is mirror-symmetrical along the time axis to cancel each other thereby eliminating the overall CMV. The experimental result shows good execution of the ZCMVM method, despite the CMV spikes caused by the 300 ns dead time.

The proposed modulation aims to eliminate the CMV profile through modulation, however, the same dv/dt components still exist because of the switching actions and dead-time effect. Therefore, the high-frequency EMI noise dominated by the high-speed transient processes will not be effectively reduced compared to CSPWM. Considering the CM filter is typically designed with respect to low-frequency

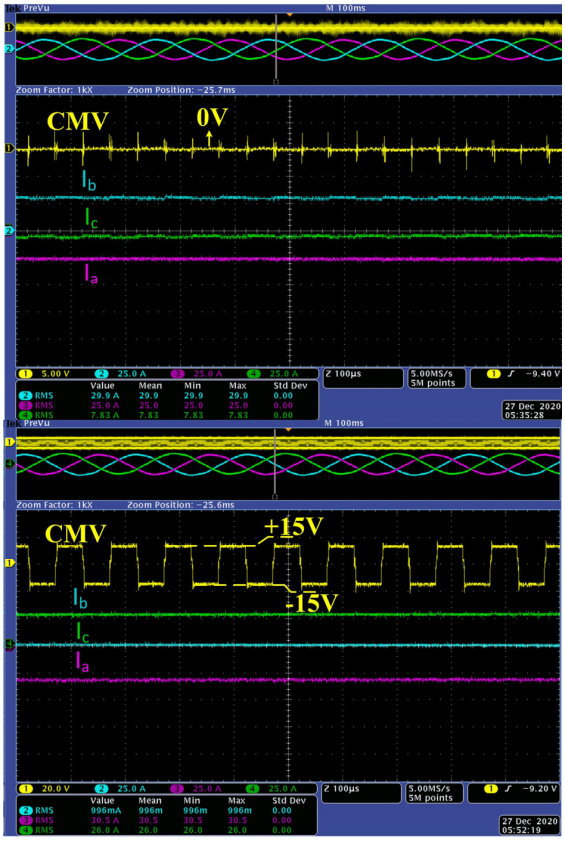

Fig. 11. CMV waveform for ZCMVM (top) and CSPWM (bottom).

range as the high-frequency components are relatively easier to damp, the CM EMI spectrum on the low-frequency conductive range is measured and shown in Fig. 12, given the modulation index equals 0.6. The frequency range (150kHz-300kHz) is defined in CISPR-25 as the longwave (LW) broadcast band, which is strongly affected by the modulation-based CMV reduction. With ZCMVM, the CMC reduction is significant. The maximum reduction is around 23 dBuV.

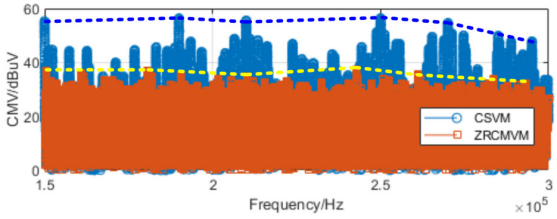

Fig. 12. CMC spectrum comparison @MI=0.6.

As for the differential-mode performance, the phase current waveform is captured and shown in Fig. 13. Even though close to the modulation limit. The current still keeps an undistorted sinusoidal profile. By measuring the current ripple through an RF current probe, the tested phase current ripple is captured. As shown in Fig. 14, the phase current ripple of ZCMVM is not significantly larger than CSPWM. The total ripple to phase current RMS ratio increment is less than 1.7%. Such performance not only prevents worsening phase current THD but also avoids louder acoustic noise when the switching frequency is below 20 kHz.

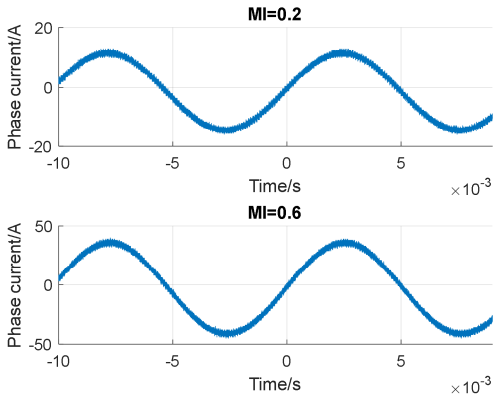

Fig. 13. Phase current waveforms for ZCMVM.

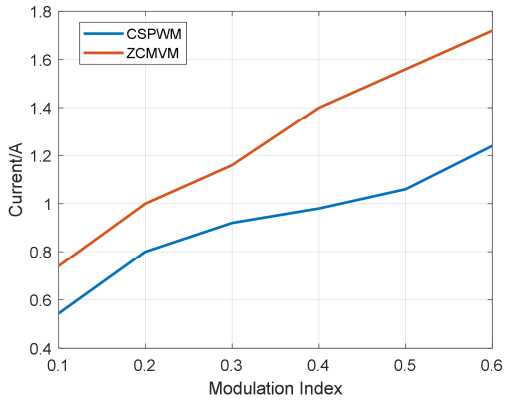

Fig. 14. Phase current ripple measurement.

V. Conclusions and Future Work

This paper proposed an SPWM based CMV elimination modulation method. A comprehensive mathematical derivation is performed to validate its feasibility. An efficient implementation approach in FPGA for PWM manipulation is also introduced. Some preliminary experimental results are presented to show the performance of ZCMVM compared with CSPWM. CMV reduction is significant. The complete modeling details and the effectiveness of ZCMVM and the corresponding differential-mode impact are investigated. According to the simulation and experimental results, a general summary of ZCMVM could be made:

1) The modulation is CSPWM-based, the overall implementation difficulty is low.

2) The CM EMI of the motor drive system is significantly reduced without degrading the differential-mode performance.

3) The total switching loss of ZCMVM is the same as CSPVM as no extra switching action is introduced. Therefore, system efficiency is not sacrificed.

4) Due to the CSPWM-based mechanism, the maximum linearity range is restricted to 0.785, which is 15% less than CSVM.

The future work is to extend this method to full modulation range for higher modulation linearity and DC-bus utilization and to analytically model its impact on the phase-current ripple and DC-link ripple. Quantifying the benefit in reducing the CM choke size is also the interest.

Acknowledgment

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References

[1] Hava, Ahmet M., and Emre Ün. "Performance analysis of reduced common-mode voltage PWM methods and comparison with standard PWM methods for three-phase voltage-source inverters." *IEEE Transactions on Power Electronics* 24.1 (2009): 241-252.

[2] Jiang, Dong, Fei Wang, and Jing Xue. "PWM impact on CM noise and AC CM choke for variable-speed motor drives." *IEEE Transactions on Industry Applications* 49.2 (2013): 963-972

[3] Levi, Emil. "Multiphase electric machines for variable-speed applications." *IEEE Transactions on industrial electronics* 55.5 (2008): 1893-1909.

[4] Wang, Lu, Yanjun Shi, and Hui Li. "Anti-EMI noise digital filter design for a 60-kW five-level SiC inverter without fiber isolation." *IEEE Transactions on Power Electronics* 33.1 (2017): 13-17.

[5] Levi, E., et al. "Multiphase induction motor drives–a technology status review." *IET Electric Power Applications* 1.4 (2007): 489-516.

[6] Shen, Zewei, et al. "Common-Mode Voltage Elimination for Dual Two-Level Inverter-Fed Asymmetrical Six-Phase PMSM." *IEEE Transactions on Power Electronics* 35.4 (2019): 3828-3840.

[7] Bojoi, Radu, et al. "INDUSTRIAL POWER CONVERSION SYSTEMS DEPARTMENT-Industrial Drives Committee-Digital Field-Oriented Control for Dual Three-Phase Induction Motor Drives." *IEEE Transactions on Industry Applications* 39.3 (2003): 752-760.

[8] Singh, Girish Kumar, K. Nam, and S. K. Lim. "A simple indirect field-oriented control scheme for multiphase induction machine." *IEEE Transactions on Industrial Electronics* 52.4 (2005): 1177-1184.

[9] Hu, Sideng, et al. "Research on the integration of hybrid energy storage system and dual three-phase PMSM drive in EV." *IEEE Transactions on Industrial Electronics* 65.8 (2017): 6602-6611.

[10] Bhattacharya, Subhadeep, et al. "A dual three-level T-NPC inverter for high-power traction applications." *IEEE Journal of Emerging and Selected Topics in Power Electronics* 4.2 (2016): 668-678.

[11] Jiang, Xuefeng, et al. "Electric drive system of dual-winding fault-tolerant permanent-magnet motor for aerospace applications." *IEEE Transactions on Industrial Electronics* 62.12 (2015): 7322-7330.

[12] Zhao, Yifan, and Thomas A. Lipo. "Space vector PWM control of dual three-phase induction machine using vector space decomposition." *IEEE Transactions on industry applications* 31.5 (1995): 1100-1109.

[13] Chinmaya, K. A., and Girish Kumar Singh. "Experimental analysis of various space vector pulse width modulation (SVPWM) techniques for dual three-phase induction motor drive." *International Transactions on Electrical Energy Systems* 29.1 (2019): e2678.

[14] López, Óscar, et al. "Space-vector PWM with common-mode voltage elimination for multiphase drives." *IEEE Transactions on Power Electronics* 31.12 (2016): 8151-8161.

[15] Julian, Alexander L. Active common mode voltage reduction in voltage source inverters. University of Wisconsin--Madison, 1997.

[16] Huang, Yang, et al. "Analytical Characterization of CM and DM Performance of Three-Phase Voltage-Source Inverters Under Various PWM Patterns." *IEEE Transactions on Power Electronics* 36.4 (2020): 4091-4104.