Development of a Two-Level VSC Based DC Impedance Measurement Unit

Le Kong [1], Nattapat Praisuwanna[1], Liang Qiao[1], and Fred Wang[1,2]

[1] Min H. Kao Department of Electrical Engineering & Computer Science,
The University of Tennessee, Knoxville, TN, USA
[2]Oak Ridge National Laboratory, Oak Ridge, TN, USA
lkong4@vols.utk.edu

***Abstract*—To analyze the small-signal stability of a power-electronics-based dc distribution system, it is important to know the converter input and output impedances. In a physical system, the converter impedances are measured for stability analysis in different ways. Many impedance measurement methods require dedicated frequency analysis equipment and/or are not suitable for high-power applications. This paper proposes one practical and easy-to-use solution for dc impedance measurement, which does not need any dedicated equipment or any extra power supply. Instead, it uses a two-level voltage source converter, which is usually available in a hybrid dc grid, to inject small perturbations into the system under test. Then the dc terminal voltage and current waveforms are measured by oscilloscopes and imported to MATLAB for further handling. Fast Fourier transform and system identification techniques are conducted to get the non-parametric impedance transfer functions. Simulation and experimental results are also given to validate the effectiveness of this approach.**

***Keywords— dc* impedance measurement, two-level VSC, small-signal stability**

I. INTRODUCTION

The dc impedance of a three-phase ac/dc converter is one of the most important parameters for small-signal stability analysis in hybrid dc grids. It has been shown that by analyzing the relationships between the output impedance of source-side converter Z_S and the input impedance of load-side converter Z_L, system stability can be determined [1-4]. In addition, the converter impedance characteristics can be used as one of the stability indicators for system power stage and controller design. Fig. 1 shows an example of stability analysis in a multi-converter dc system. In this scenario, it is of great importance to find a way to fully characterize the converter impedances Z_s and Z_L so that system stability can be further analyzed.

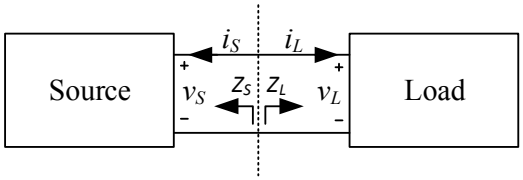


Fig. 1. Impedance-based stability analysis of a dc system.

For low voltage and low power applications, a commercial frequency response analyzer (FRA) is usually available. However, for high voltage high power applications, it requires more dedicated equipment, except for a FRA, a power amplifier and an isolation transformer are also needed, which are not easy to set up in most cases [5, 6]. Therefore, to measure the impedances without using any dedicated equipment, it would be good to use converters existing in the system under test (SUT).

To measure dc impedance using converters already existing in the system, a dc/dc converter is usually used. As shown in [7, 8], a small perturbation is injected into the control loop of the dc/dc converter in the system. The terminal voltages and currents are then monitored. Thereof, converter impedances can be identified. But in a dc grid with only ac/dc or dc/ac converter, there is no existing dc/dc converter. If adding one dc/dc converter as the impedance measurement unit, an extra dc power supply will be needed. In [9], an impedance measurement unit (IMU) based on power electronics building block (PEBB) is introduced. But this method also requires extra hardware and control blocks.

To minimize the efforts on building a new circuit to measure the impedance, an easy measurement setup is proposed in this paper. In hybrid dc grids (paralleled structure or multi-terminal structure) as shown in Fig. 2, a two-level voltage source converter (2L-VSC) is usually available, therefore, the proposed impedance measurement unit can be developed based on it. As shown in [10], a 2L-VSC is also used for impedance measurement but it is for ac impedance measurement, which is different on the controller and power stage requirements from dc impedance measurement.

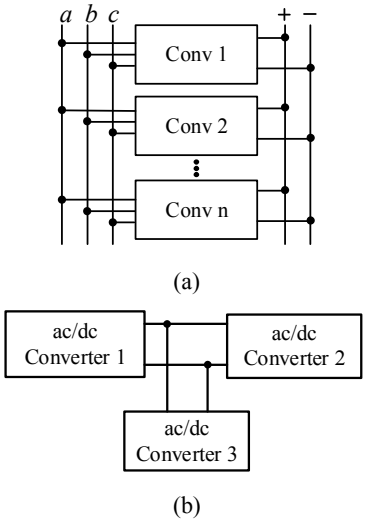


Fig. 2. Scenarios for the proposed IMU: (a) a paralleled converter structure and (b) a multi-terminal dc grid.

Compared with the existing impedance measurement methods, the contributions of this paper can be summarized as follows:

(1) There is no need for dedicated equipment, such as a frequency response analyzer or a power amplifier.

(2) There is no extra dc power supply or ac source required.

(3) It is suitable for a power system with a paralleled converter structure or a multi-terminal dc grid.

In this paper, the structure and control diagram of the proposed 2L-VSC based impedance measurement unit are presented first in section II. An impedance transfer function identification method will also be introduced. In section III and section IV, simulations and experimental results are given to validate the usefulness of the proposed method. Several practical issues about the measurement setup are discussed too. Section V concludes the paper.

II. Proposed 2L-VSC Based DC Impedance Measurement Unit

A. Concept, Structure, and Flowchart of the Proposed Impedance Measurement Method

In order to measure the small-signal dc impedance of an ac/dc converter, small sinusoidal disturbances are usually injected into the system, such as a shunt current perturbation injection as shown in Fig. 3(a) or a series voltage perturbation injection as shown in Fig. 3(b). Then by analyzing the response waveforms under the perturbations, small-signal models can be obtained. Usually, the current or voltage perturbation signals are generated by a FRA with a power amplifier. And the amplitude of the injection signal should be small enough to avoid affecting the system steady-state operation. The injected low-frequency perturbation magnitude is usually selected to be smaller than 10% of the normal operating points. For high-frequency injections, the amplitude can be around 20%-30% of the steady-state operating point to compensate for the low-pass filter impacts and increase the high-frequency noise immunity [10].

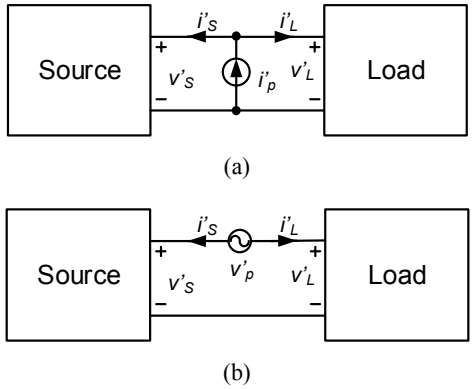


Fig. 3. Small-signal injections: (a) shunt current perturbation injection and (b) series voltage perturbation injection.

In this paper, to avoid using any dedicated equipment like a FRA or a power amplifier, an impedance measurement method is proposed based on a 2L-VSC, since a 2L-VSC can be easily obtained in most hybrid dc systems. The schematic of the impedance measurement setup is shown in Fig. 4. There are three types of converters in the system: one is a source side converter, one is a load side converter and another is an IMU converter. A three-phase voltage source is connected in the system to provide power for both source converter and IMU converter. And the IMU generates the perturbation signals to the dc link in the system under test which will be discussed in detail in section II-part B. In the IMU setup, probes and oscilloscopes are required for waveform measurement and data acquisition. The MATLAB environment is also needed for data processing to obtain the small-signal model as will be further introduced in section II-part C.

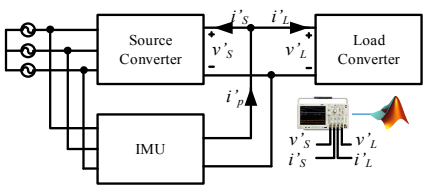


Fig. 4. Structure of the proposed IMU.

Fig. 5 shows the flowchart of the impedance measurement process. First, the test frequency range and the test points should be defined. The identifiable perturbation frequency can be up to half of the switching frequency of SUT which is f_{max}. The lowest frequency f_{min} can start from 1 Hz. Since the terminal voltage (v'_S, v'_L) and current (i'_S, i'_L) at the source side and load side at each frequency are measured by probes and the data are acquired through an oscilloscope, if the lower-frequency (<1 Hz) perturbation is injected, the oscilloscope may not have enough memory to store all data. The sampling rate of the oscilloscope is set to be 1MS/s. In addition, the number of testing point N is selected by the user. The larger N is, the more impedance data can be obtained. With the predefined frequency range and number of test times, the perturbation frequency test points can be selected. For example, the N test points can be equally scattered within the identifiable frequency range in the logarithmic scale.

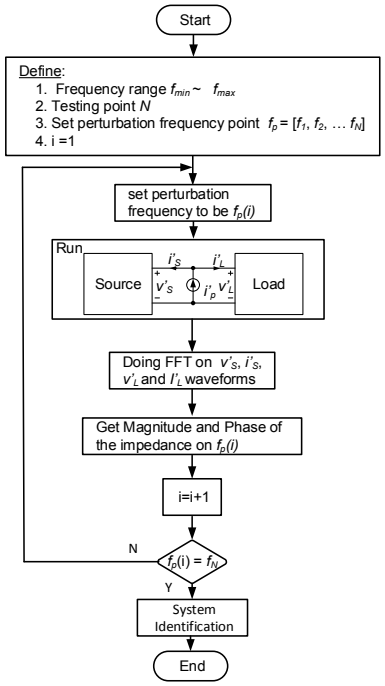


Fig. 5. Flowchart of the proposed impedance measurement method.

Then, we can start to test from the first testing point and continue the test until we finish the last testing point. Considering the accuracy of data measurement and FFT calculation, multiple periods of the injected sinusoidal perturbations should be guaranteed. The lower the injection frequency is, the longer the injection time it should be. For example, 4 seconds of perturbation injection is used for 1 Hz disturbance and 0.2 seconds of perturbation injection is used for 50 Hz disturbance.

After finishing frequency sweeping at all the test points, the measured waveforms are imported into MATLAB for

further analysis. By doing FFT and system identification using toolbox in MATLAB, Z_S and Z_L can be achieved with $Z_S(s) = v'_S(s)/i'_S(s)$ and $Z_L(s) = v'_L(s)/i'_L(s)$.

B. Circuit Diagram and Control Structure of the Proposed IMU

One of the most important steps of the proposed impedance measurement method is the generation of perturbation signals using a 2L-VSC. Fig. 6 shows the circuit diagram of the proposed current perturbation injection circuit. Compared with the conventional 2L-VSC structure, a resistor R_{dc} with a paralleled switch *S2* is connected on the dc link and a switch *S1* is connected in series with the large dc-link capacitor C_{dc2}. This proposed IMU structure can have two working modes: one is a conventional rectifier and the other is an impedance measurement unit. If working as a conventional 2L-VSC rectifier, the switch *S1* and *S2* are both "on" to obtain a large dc-link capacitor ($C_{dc1} + C_{dc2}$) and to bypass the resistor R_{dc} on the dc link. But when working as the perturbation current injection circuit, the switch *S1* is "off" to have a smaller dc-link capacitor C_{dc1} which can filter out the high-frequency noise but keep the perturbation component. And the switch *S2* is also "off" to decouple the dc bus of SUT v_{bus} and dc output of IMU v_t. The decoupling resistor R_{dc} is designed based on the perturbation amplitude. For example, if i_p is designed to be 10% of i_{nom} and v_t is designed to be $1.1v_{bus}$, then R_{dc} would be selected as v_{bus}/i_{nom}. The losses introduced by this resistor is very small due to the small-magnitude current perturbation injection.

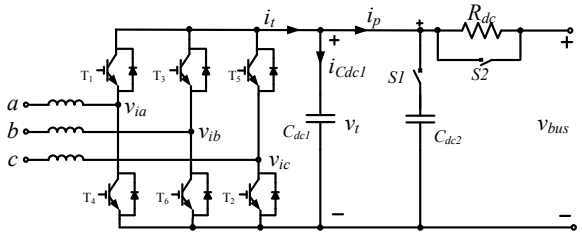


Fig. 6. Circuit diagram of the proposed IMU.

Based on the circuit diagram in Fig. 6, the relationships between the dc bus voltage v_{bus} and the IMU dc terminal voltage v_t are determined by the perturbation current i_p and decoupling resistor R_{dc}, which can be expressed as in (1). And the current flowing out of the dc terminal of the IMU i_t can be determined as shown in (2), which is the sum of the dc capacitor current i_{Cdc1} and perturbation current i_p. Then, according to the ac and dc power balance concept, the *d*-axis reference current i_{dref} can then be estimated as in (3) in the synchronous control frame. This calculated reference value i_{dref} can be used to generate the control signals of the IMU through an open-loop control block to avoid the limitations of the closed-loop control bandwidth. Also, reactive power is controlled to be 0 through a closed-loop PI controller for better accuracy because reactive power will only have slight impacts on dc side current so that *q* axis control bandwidth limitations can be ignored. Besides, the desired current perturbation i_p is a sinusoidal signal, where the perturbation frequency f_p and perturbation amplitude A_p are given by the user to the controller through a LabVIEW interface. Therefore, this open-loop active power and closed-loop reactive power control diagram can be obtained as shown in Fig. 7. With the duty cycle generator, the corresponding three-phase duty cycles D_a, D_b, and D_c can be obtained for the gate control signals for the switches in the proposed IMU. In addition, the sinusoidal pulse width modulation technique is adopted in this paper.

$$v_t = v_{bus} + i_p R_{dc} \tag{1}$$

$$i_t = C_{dc1}\frac{dv_t}{dt} + i_p \tag{2}$$

$$i_{dref} \approx \frac{v_t i_t}{v_d} \tag{3}$$

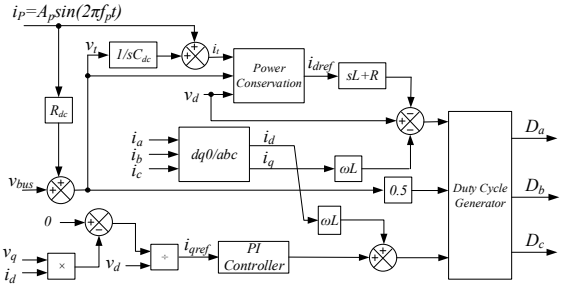


Fig. 7. Control block of the proposed IMU.

C. Identification of Impedance Transfer Functions

With different perturbations, a group of terminal voltage and current data can be obtained by oscilloscopes. By importing these data to MATLAB and doing Fast Fourier transform (FFT), a set of discrete impedance data (frequency, magnitude, and phase) can be calculated. However, these discrete data cannot be directly used to analyze system stability. To further use these data, they need to be transferred to continuous transfer functions. To do so, *System Identification Toolbox* in MATLAB [11] can be adopted.

The system identification process requires a model structure first and estimation methods will then be applied to determine the numerical values of the model parameters. We know that any transfer function can be expressed by an l^{th}-order ($l = \max\{m, n\}$) expression as shown in (4), which can also be used as the model structure in our case. By increasing the order number until an accurate model is found through this iterative process, the corresponding impedance transfer functions can finally be achieved. Then with the estimated impedance models, system stability can be analyzed using either Nyquist stability criterion [12] or passivity-based stability criterion [4].

$$Z(s) = \frac{b_m s^m + b_{m-1}s^{m-1} + \cdots + b_o}{a_n s^n + a_{n-1}s^{n-1} + \cdots + a_o} \tag{4}$$

Though this non-parametric model cannot tell the direct impact of the converter hardware and controller design on its terminal characteristics, it can still be used to analyze system stability and be used to check the accuracy of the derived mathematical model.

III. Simulation Results and Analysis

To verify the proposed IMU, a dc test system consisting of a modular multilevel converter (MMC) which is working as the source converter and a 2L-VSC which is working as the load converter is built. Also, the 2L-VSC based IMU is connected in parallel with the MMC for the source converter output impedance measurement and load converter input impedance measurement.

Fig. 8 shows the simulation schematic of the test system. There are two sets of simulations conducted for comparison: one is perturbation injection with the proposed IMU and the other is perturbation injection with an ideal current source which can be regarded as the benchmark. The comparisons are designed to see the effectiveness of the perturbation signals generated by the proposed IMU.

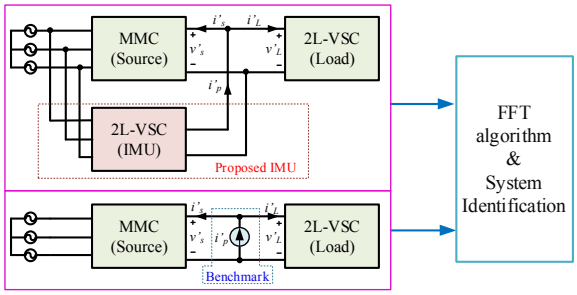


Fig. 8. Simulation circuit diagram in MATLAB/Simulink.

The simulation results of the source converter output impedance and load converter input impedance are shown in Fig. 9 separately. The results are in the frequency range of [1 Hz, 1 kHz]. The blue squares are the benchmark simulation results, the red stars are the discrete simulation data with the proposed IMU and the black line is a continuous model identified from the simulated discrete data. The source output impedance can be modeled as a 10^{th}-order transfer function and the load input impedance is estimated as a second-order transfer function. Take the load converter input impedance $Z_{L\_SI\_SIMU}(s)$ as an example, the system identification result can be obtained as shown in (5). From the Bode diagrams in Fig. 9, it can be seen that, for both source converter impedance and load converter impedance, the measured discrete data and the system identification results both match well with the benchmark simulations. It indicates that the results of perturbation injection generated by the proposed IMU are the same as the injection by the ideal current source and the system identification technique can estimate the impedance model correctly. We can also tell that the more simulation points are, the more accurate the system identification model would be.

$$Z_{L\_SI\_SIMU}(s) = \frac{0.005017s^2 + 182.1s - 2309}{s^2 - 17.86s + 64.46} \qquad (5)$$

IV. Experimental Platform and Results

To further demonstrate the effectiveness of the proposed IMU, an experimental platform is constructed with the same dc system structure as in the simulation. Fig. 10 shows the hardware setup in the lab. A three-phase MMC with 10 submodules in each arm is working as the source converter [13] and 2L-VSC converts dc to ac which can be regarded as a constant power load (CPL). By connecting another 2L-VSC (similar design and power rating as CPL in SUT) in parallel with the MMC and controlling it to work as an IMU, small current perturbations can be injected into the dc-link of the SUT. The three-phase ac voltage input of MMC and IMU is connected to the wall power. Tektronix oscilloscopes are used to measure and store the response waveforms under perturbations. Then the data are transmitted to personal computers (PCs) for monitoring and handling. By doing data processing offline, the MMC output

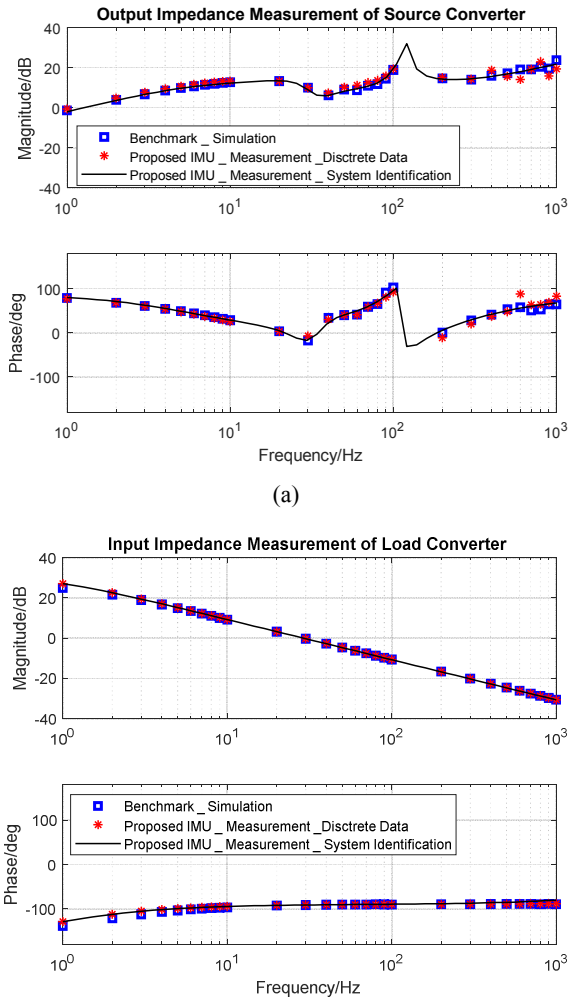


Fig. 9. Simulation results of impedance measurement: (a) source output impedance and (b) load input impedance.

impedance and CPL input impedance models can then be estimated.

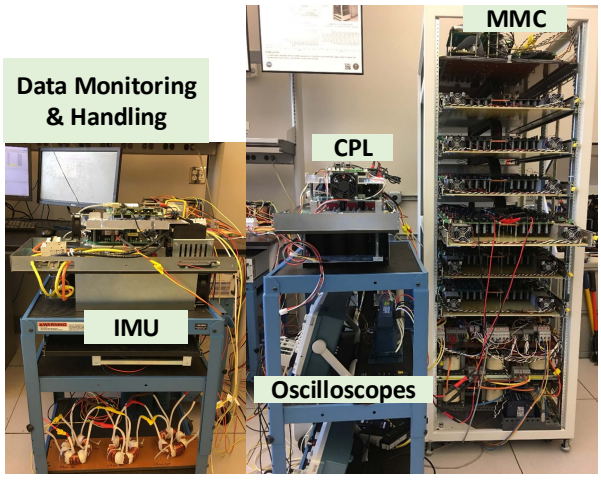


Fig. 10. Hardware setup of converter impedance measurement using the proposed IMU.

A. Practical Considerations

Unlike the conceptual design, there will be some practical issues when doing hardware tests, such as

circulating current, control delay effects, and operation sequence. These practical considerations will be discussed as follows.

1) Elimination of circulating currents

There are different types of circulating currents in the common-ac and common-dc parallel structure which will affect the impedance measurement results. And there are also some solutions by adding extra control blocks or some hardware to suppress these circulating currents as introduced in [14-16]. In this test platform, circulating current among the paralleled structure is suppressed by adding a three-phase transformer at the ac input side of the IMU for simplicity.

2) Minimization of control delay effects

There will be time delays in digital signal processing controllers (DSP). To eliminate the control delay effects, the controller structure needs to be designed efficiently to minimize the time delay. Except for that, some delay compensation methods (e.g., linear predictor, first-order-filter compensation, or shifting sampling instant) can also be implemented in the control loop as introduced in [17]. In this paper, a first-order-filter (FOF) compensation is adopted in the control loop.

3) Design of operation sequence

For such a three-converter system, an appropriate operation sequence is also important. If not starting up or shutting down properly, there may be huge inrush current which may cause a trip or even damage the whole system, especially under high voltage and high power conditions. The key to the start-up and shutdown process is to minimize the voltage difference. Therefore, the recommended start-up and shut-down sequences are shown below.

a. Start-up sequence:

(1) Pre-charge source side MMC submodules capacitors and dc bus capacitor (If the source converter is also a 2L-VSC, only the dc bus capacitor needs to be pre-charged).

(2) Turn on the ac voltage source.

(3) Enable source side converter control to regulate dc bus voltage with no load condition.

(4) Enable load converter control.

(5) Enable IMU control to start to inject perturbation signals.

b. Shut-down sequence:

(1) Disable IMU control.

(2) Disable load converter control.

(3) Disable source side control.

(4) Shutdown ac voltage source.

B. Experimental Results

Considering all the practical issues in the hardware platform, the experimental results can then be examined. First, the perturbation signals generated by the proposed IMU is monitored. Following the instructions given through the LabVIEW interface with the frequency range defined from f_{min} to f_{max}, the perturbation current waveforms can be measured. For example, a 1 Hz small perturbation current i_p is injected into the dc-link of the SUT which is shown as the green waveforms in Fig. 11. The blue waveform shows the line-to-line voltage v_{ab} of the IMU and the magenta waveform is the IMU dc terminal voltage v_t. It can be seen from the waveforms that 4 seconds of perturbations are injected into the SUT to have 4 periods of response data so that FFT calculation accuracy can be guaranteed.

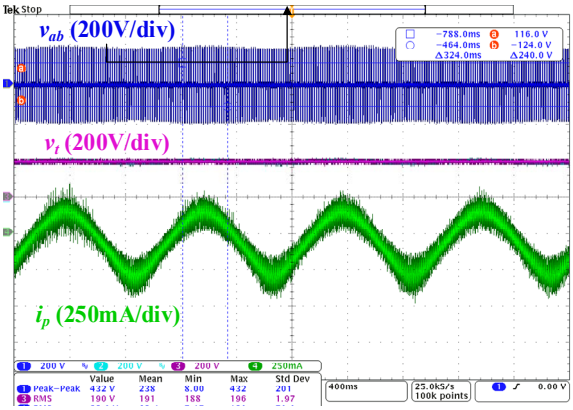
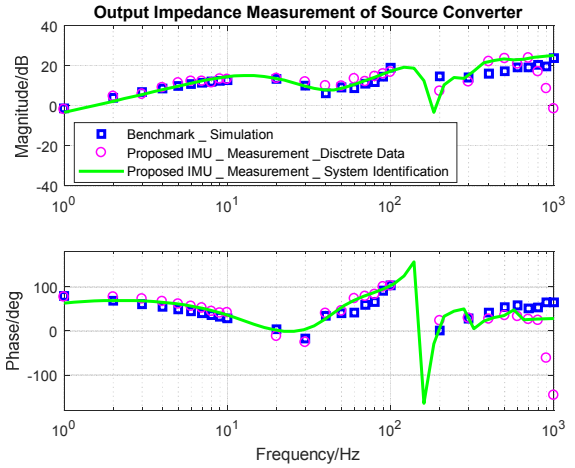
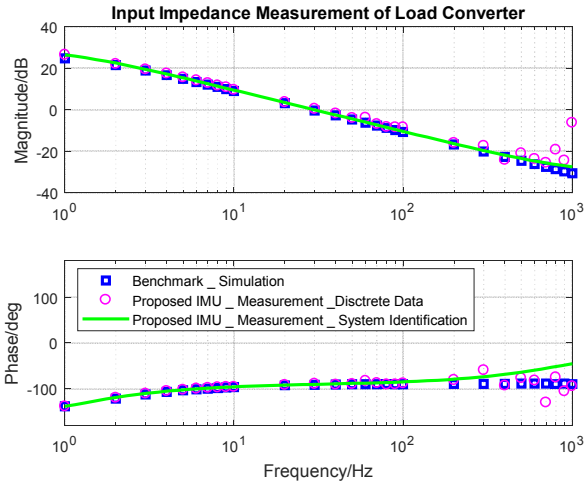


Fig. 11. Measurement of current perturbation injection at f_p = 1 Hz.



(a)



(b)

Fig. 12. Experimental results of impedance measurement: (a) source output impedance and (b) load input impedance.

With the proper perturbation signals over the desired frequency range ($f_1, f_2, \ldots, f_N$), the waveforms under different perturbations can be obtained. Then with data processing technology, the source and load impedances can be acquired. Fig. 12 shows the Bode diagram of the measured

results, where Fig. 12 (a) is for the source converter output impedance and Fig. 12 (b) is for the load converter input impedance. The blue squares are the benchmark simulation results as introduced in section III, the magenta circles are the discrete measured data with the proposed IMU and the light green line is a continuous model identified from the measured discrete data. The estimated results from the measured data of the source impedance is also a 10th-order non-parametric model and the load converter impedance from the measurement data is also a 2nd-order model which is shown in (6) as an example. From the Bode diagrams, it can be seen that the measured results (both the measured discrete data and estimated transfer functions by system identification) by the proposed IMU agree well with the simulation results with the benchmark simulation. Therefore, we can conclude that the proposed IMU can be used to measure converter dc impedance correctly.

$$Z_{L\_SI\_MEAS}(s) = \frac{0.02989s^2 + 189.1s + 838}{s^2 - 2.565s - 27.6} \qquad (6)$$

V. Conclusions

In this paper, a practical and easy-to-use dc impedance measurement unit based on a 2L-VSC for a hybrid dc grid is proposed. The impedance measurement unit is controlled to generate small current perturbations on the dc bus of the system under test. The terminal voltage and current response waveforms under the perturbations are measured and stored by oscilloscopes. Data processing, including Fast Fourier transform and System Identification, is then conducted in MATLAB with the measured data to obtain non-parametric models of converter dc impedances for system stability analysis.

Acknowledgment

This work was supported primarily by the Engineering Research Center Program of the National Science Foundation and the Department of Energy under NSF Award Number EEC-1041877 and the CURENT Industry Partnership Program.

References

[1] X. Feng, J. Liu, and F. C. Lee, "Impedance specifications for stable dc distributed power systems," *IEEE Transactions on Power Electronics,* vol. 17, pp. 157-162, 2002.

[2] J. Sun, "Impedance-based stability criterion for grid-connected inverters," *IEEE Transactions on Power Electronics,* vol. 26, pp. 3075-3078, 2011.

[3] A. Riccobono and E. Santi, "Comprehensive review of stability criteria for dc power distribution systems," *IEEE Transactions on Industry Applications,* vol. 50, pp. 3525-3535, 2014.

[4] L. Harnefors, X. Wang, A. G. Yepes, and F. Blaabjerg, "Passivity-based stability assessment of grid-connected VSCs—an overview," *IEEE Journal of Emerging and Selected Topics in Power Electronics,* vol. 4, pp. 116-125, 2016.

[5] Y. Panov and M. Jovanovic, "Practical issues of input/output impedance measurements in switching power supplies and application of measured data to stability analysis," in *Twentieth Annual IEEE Applied Power Electronics Conference and Exposition*, 2005, pp. 1339-1345.

[6] M. Liu, H. Yuan, Y. Sun, and C. Yang, "Research on measurement of Dc power supply impedance," in *9th International Conference on Electronic Measurement & Instruments*, 2009, pp. 2703-2706.

[7] M. Shirazi, J. Morroni, A. Dolgov, R. Zane, and D. Maksimovic, "Integration of frequency response measurement capabilities in digital controllers for dc-dc converters," *IEEE Transactions on Power Electronics,* vol. 23, pp. 2524-2535, 2008.

[8] T. Roinila, H. Abdollahi, S. Arrua, and E. Santi, "Online measurement of bus impedance of interconnected power electronics systems: applying orthogonal sequences," in *IEEE Energy Conversion Congress and Exposition (ECCE)*, 2017, pp. 5783-5788.

[9] Z. Shen, M. Jaksic, I. Cvetkovic, R. Burgos, and D. Boroyevich, "Small-signal impedance measurement in medium-voltage dc power systems," in *International Conference on Electrical Systems for Aircraft, Railway, Ship Propulsion and Road Vehicles (ESARS)*, 2015, pp. 1-5.

[10] W. Cao, Y. Ma, X. Zhang, and F. Wang, "Sequence impedance measurement of three-phase inverters using a parallel structure," in *IEEE Applied Power Electronics Conference and Exposition (APEC)*, 2015, pp. 3031-3038.

[11] *System identification overview*. Available [Online]: https://www.mathworks.com/help/ident/gs/about-system-identification.html

[12] L. Kong, S. Wang, N. Praisuwanna, S. Zhang, L. Qiao, F. Wang, *et al.*, "DC impedance model of MMC considering capacitor voltage and circulating current dynamics," in *IEEE Energy Conversion Congress and Exposition (ECCE)*, 2019, pp. 646-653.

[13] S. Zhang, S. Wang, N. Praisuwanna, L. Kong, Y. Li, R. B. Martin, *et al.*, "Development of a flexible modular multilevel converter test-bed," in *IEEE Energy Conversion Congress and Exposition (ECCE)*, 2018, pp. 5250-5257.

[14] Y. Zhihong, D. Boroyevich, C. Jae-Young, and F. C. Lee, "Control of circulating current in two parallel three-phase boost rectifiers," *IEEE Transactions on Power Electronics,* vol. 17, pp. 609-615, 2002.

[15] B. Wei, J. M. Guerrero, J. C. Vásquez, and X. Guo, "A circulating current suppression method for parallel connected voltage-source-inverters (VSI) with common DC and AC buses," in *IEEE Energy Conversion Congress and Exposition (ECCE)*, 2016, pp. 1-6.

[16] Y. Ma, L. Yang, J. Wang, X. Shi, F. Wang, and L. M. Tolbert, "Circulating current control and reduction in a paralleled converter test-bed system," in *IEEE Energy Conversion Congress and Exposition*, 2013, pp. 5426-5432.

[17] M. Lu, X. Wang, P. C. Loh, F. Blaabjerg, and T. Dragicevic, "Graphical evaluation of time-delay compensation techniques for digitally controlled converters," *IEEE Transactions on Power Electronics,* vol. 33, pp. 2601-2614, 2018.