Grid Stability Enhancement by a High Voltage SiC MOSFET-Based Asynchronous Microgrid Power Conditioning System

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***Abstract*—Asynchronous microgrid (ASMG) is a microgrid concept where the ac microgrid is connected to a utility grid through a power conditioning system (PCS). The development of high voltage (HV, >3.3 kV) silicon carbide (SiC) MOSFET technology promotes the implementation of ASMG PCS converters. However, the system-level benefits from SiC MOSFETs have not been well studied for this application. This paper discusses ASMG system stability enhancement resulting from HV SiC MOSFET-based PCS converters. HV SiC MOSFET-based PCS converters can achieve high control frequency, which can benefit the potential harmonic instability caused by the digital control delay. A detailed theoretical analysis is provided, and experimental results for the stability enhancement capability are demonstrated on a converter-based hardware testbed (HTB).**

Keywords—Asynchronous microgrid, power conditioning system, medium voltage converter, high voltage SiC MOSFET, harmonic stability enhancement.

I. INTRODUCTION

Asynchronous microgrids with PCS converters are one of the key application scenarios for future medium voltage (MV) converters [1-2]. In an ASMG, a back-to-back connected ac/dc, dc/ac PCS converter works as the interface of the microgrid to the utility grid. Previous study of ASMG focuses on the system operation benefits resulting from the ASMG structure, including isolation of faults [3], better mode transition performance [4], etc. The recent development of HV SiC devices are starting to facilitate the ASMG PCS implementation. Reference [5] proposed a 10 kV SiC MOSFET-based 3-level neutral point clamped (3L-NPC) converter-based PCS converter. References [6-7] designed and implemented a 10 kV SiC MOSFET-based modular multi-level converter (MMC) for the ASMG PCS.

However, existing research of PCS converters has mainly focused on the converter design [6] and converter-level benefits (size, efficiency, etc.) provided by HV SiC MOSFETs. System-level grid benefits that are driven by the HV SiC MOSFETs still need to be evaluated. Compared with silicon (Si) devices, HV SiC MOSFETs have several advantages such as lower switching loss and faster switching speed [8], which result in higher control frequency and bandwidth. Higher control frequency and bandwidth can lead to shorter digital control delay [9] and better transient performance, which may benefit the ASMG operation.

This paper demonstrates one of the benefits, the grid stabilizer capability provided by the HV SiC MOSFET-based PCS converter. The microgrid is usually supported by multiple distributed energy resources (DERs) with inverter interfaces, which may lead to interaction instability [10]. In the ASMG case, since the main grid and microgrid are decoupled by the PCS, the interactions and disturbances caused by the microgrid are isolated by the PCS. The interaction stability is then determined by the grid side PCS and grid conditions. The digital control delay in the grid side PCS will introduce negative conductance to the PCS output admittance, which reduces the system damping capability and causes instability over a certain frequency range called the non-passive region [11].

The SiC-based PCS may mitigate the instability caused by the control delay as higher control frequency and shorter control delay can be realized. In this paper, the theoretical analysis results show that SiC-based PCS can move the non-passive region to higher frequencies to reduce its impacts on lower-order grid harmonics which are usually difficult to deal with [12]. Moreover, besides PCS control loop stability requirements, the grid interaction stability issue will further limit the control bandwidth of the PCS. By using the SiC-based PCS, higher control bandwidth can be realized considering interaction stability. The experimental verifications are demonstrated on the converter based HTB [13].

The rest of the paper is organized as follows: Section II introduces the ASMG system structure and PCS decoupling capability. Section III provides the output admittance model of grid side PCS. Section IV provides a theoretical analysis of grid stability enhancement capability from HV SiC MOSFET based PCS. HTB test results are demonstrated in Section V, and conclusions are drawn in Section VI.

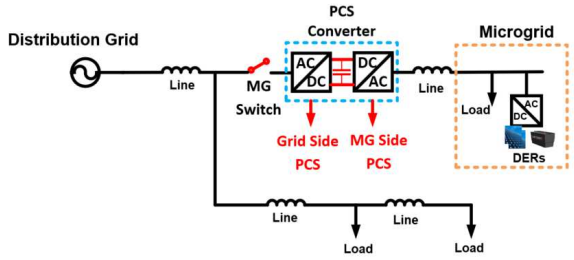


Fig. 1. Asynchronous microgrid (ASMG) concept using two back-to-back connected converters,

II. ASMG Structure and PCS Decoupling

A. ASMG Structure

In an ASMG, the main distribution grid and the microgrid are connected through the PCS converter. As shown in Fig. 1, a PCS converter contains two parts: grid side PCS and microgrid side PCS. There are two operation modes for an ASMG: (1) grid-connected mode and (2) islanded mode. The PCS converter operation in these two modes are different [2].

In the grid-connected mode, the ASMG is part of the main grid. The grid side PCS works as the rectifier to regulate the dc-link voltage and provide the main grid with reactive power support; the microgrid side PCS is controlled as a voltage source to regulate the voltage and frequency of the microgrid. The main grid and microgrid share the active power while the reactive power is decoupled by the PCS, meaning that the reactive power of the microgrid is provided locally.

In the islanded mode, the microgrid is disconnected from the main grid and the microgrid side PCS works as a rectifier to regulate the dc-link voltage. In this case, the microgrid voltage and frequency are provided by DERs within the microgrid.

B. PCS Decoupling

In an ASMG, since the PCS works as the interface of the microgrid, the grid and microgrid are decoupled by the PCS from multiple perspectives, including frequency decoupling, reactive power decoupling, and impedance decoupling. The frequency decoupling can result in potential asynchronous operation of grid and microgrid, which offers more flexibility for the microgrid frequency regulation. The reactive power decoupling can increase the dispatchable power of the local sources in the microgrid as the reactive power required by the grid is provided by the grid side PCS. The impedance decoupling can potentially benefit the grid stability.

In an interconnected system, the interactions among different subsystems may lead to stability issues. The interaction stability issue can be studied by analyzing the impedance/admittance interactions among subsystems as the impedance/admittance is a representative indicator of the system stability [11].

The impedance-based model for the synchronous microgrid (SMG) and ASMG are shown in Fig. 2. In the SMG shown in

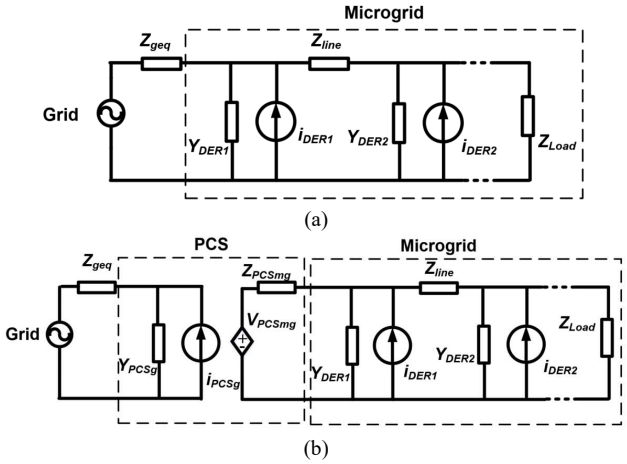


Fig. 2. Impedance-based model: (a) SMG case; (b) ASMG case.

Fig. 2(a), the microgrid is directly connected to the main grid, where the DERs and loads in the microgrid will directly interact with the main grid. The DERs are usually connected to the grid with power electronics-based interfaces, and loads' conditions can also vary from time to time. Therefore, the impedance or admittance characteristics of the microgrid are complicated, and the interaction stability is difficult to be guaranteed at all times.

However, for the ASMG shown in Fig. 2(b), the grid and microgrid are decoupled. From the grid side, the equivalent microgrid side admittance is the admittance of the grid side PCS. The stability impacts of the microgrid are mostly determined by the grid side PCS. Although the dc voltage perturbation may also impact the grid side PCS impedance, the impacts are limited and at a relatively low frequency range [14]. Therefore, in this paper, the dc voltage perturbation impacts will not be considered.

III. PCS Admittance Modelling and Stability Analysis

As shown in Fig. 2(b), the output admittance of the grid side PCS can be used to study the microgrid interaction stability with the main grid. In the grid-connected mode, the grid side PCS serves as a rectifier to regulate the dc-link voltage of the PCS and provides the grid with reactive power. The control diagram is shown in Fig. 3, where the dc voltage and reactive power are controlled in *dq* coordinates. The phase lock loop (PLL) is also realized in *dq* coordinates to synchronize the PCS with the main grid. Therefore, the admittance of grid side PCS is modelled in *dq* coordinates, which is an admittance matrix due to the coupling of *d* and *q* axis [15]. In this paper, the dc voltage and reactive power loop impacts on the output admittance are not considered as these loops are very slow.

A. PCS Admittance Model

The ac output admittance of the grid side PCS is determined by the inverter output passive filter as well as the control loop. As part of the control loop, the PLL will have impacts on the

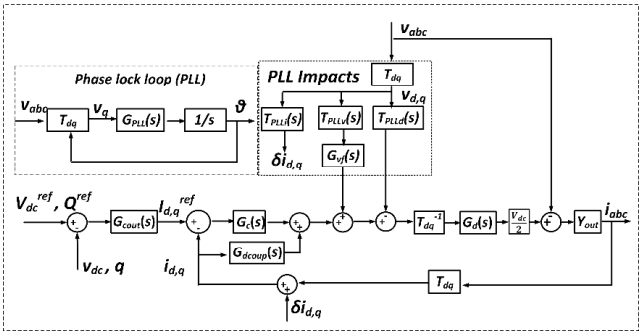


Fig. 3. Control diagram for grid side PCS.

PCS output admittance characteristics. The PLL introduces a disturbance to the sensed voltage and current during *dq* transformation and impacts the duty cycle generation during inverse *dq* transformation. The PLL impact matrices are defined as $\boldsymbol{T_{PLLv}}$, $\boldsymbol{T_{PLLi}}$, $\boldsymbol{T_{PLLd}}$ in (1)-(3):

$$\boldsymbol{T_{PLLi}} = \begin{bmatrix} 0 & T_{PLL} I_q^c \\ 0 & -T_{PLL} I_d^c \end{bmatrix} \tag{1}$$

$$\boldsymbol{T_{PLLv}} = \begin{bmatrix} 1 & T_{PLL} V_q^c \\ 0 & 1 - T_{PLL} V_d^c \end{bmatrix} \tag{2}$$

$$\boldsymbol{T_{PLLd}} = \begin{bmatrix} 0 & -T_{PLL} D_q^c \\ 0 & T_{PLL} V_d^c \end{bmatrix} \tag{3}$$

where $T_{PLL} = \frac{G_{PLL}}{s + V_d^c G_{PLL}}$ and G_{PLL} is the proportional-integral (*PI*) controller in the PLL. Subscript *c* represents *dq* value in the controller. The $\boldsymbol{G_{vf}}$ in the PLL impact loop is a first order filter matrix for the voltage feedforward control, and $\boldsymbol{T_{dq}}$ is the *dq* transformation matrix. The detailed derivations of the PLL impacts are in [15-16].

Besides PLL, main control loops and passive filter impedance also contribute to the PCS output admittance. In *dq* coordinates, the admittance matrix $\boldsymbol{Y_{out}}$ of the PCS inductor filter is in (4):

$$\boldsymbol{Y_{out}} = \begin{bmatrix} sL + R & -\omega L \\ \omega L & sL + R \end{bmatrix}^{-1} \tag{4}$$

where L and R are filter inductance and resistance. The decoupling term for *dq* axis is represented by $\boldsymbol{G_{dcoup}}$ in (5); the *PI* controller matrix is $\boldsymbol{G_c}$ in (6).

$$\boldsymbol{G_{decoup}} = \begin{bmatrix} 0 & -\omega L \\ \omega L & 0 \end{bmatrix} \tag{5}$$

$$\boldsymbol{G_c} = \begin{bmatrix} k_p + \dfrac{K_i}{s} & 0 \\ 0 & k_p + \dfrac{K_i}{s} \end{bmatrix} \tag{6}$$

Moreover, the PCS output admittance should consider the impacts from digital control delay $\boldsymbol{G_d}$ in (7):

$$\boldsymbol{G_d} = \begin{bmatrix} e^{-kT_c s} & 0 \\ 0 & e^{-kT_c s} \end{bmatrix} \tag{7}$$

where T_c is the control time, k is the delay cycle, which is usually assumed to be 1.5 in grid-connected inverter cases [16]. Based on (1)-(7), the output admittance is given in (8):

$$\boldsymbol{Y_{PCSg}} = \boldsymbol{Y_{main}}\left(\boldsymbol{I} - \boldsymbol{G_d T_{dq}^{-1} Y_{PLL} T_{dq}^{-1}}\right) \tag{8}$$

where $\boldsymbol{Y_{PCSg}}$ is the ac output impedance of PCS in *dq* coordinates; $\boldsymbol{Y_{main}}$ in (9) is the output impedance contributed by the main control loop, and $\boldsymbol{Y_{PLL}}$ in (10) is the PLL impact on the output impedance.

$$\boldsymbol{Y_{main}} = \left(\boldsymbol{1} + \boldsymbol{Y_{out} G_d T_{dq}^{-1}}\left[\boldsymbol{G_c} - \boldsymbol{G_{decoup}}\right]\boldsymbol{T_{dq}}\right)^{-1}\boldsymbol{Y_{out}} \tag{9}$$

$$\boldsymbol{Y_{PLL}} = \boldsymbol{G_{vf} T_{PLLv}} - \left(\boldsymbol{G_c} - \boldsymbol{G_{deoup}}\right)\boldsymbol{T_{PLLi}} - \boldsymbol{T_{PLLd}} \tag{10}$$

B. PCS Stablity Analysis

The PCS stability contains two perspectives: the stability of the PCS control loop and the interaction stability between PCS and grid. The stability of the first perspective can be guaranteed by designing PCS controller with a stable closed-loop gain [17].

The stability of the second perspective should consider both the PCS as well as the grid condition. However, actual grid condition can be complicated and changing with time, and the admittance of the grid side PCS may cause instability at different frequency areas. One conservative stability analysis approach is the passivity-based approach, meaning that when the phase of the inverter is within the passive region ($[-90^{\circ}, 90^{\circ}]$), the inverter will not cause interactive instability when connecting to a passive grid [11].

The PCS admittance is studied on a scaled system shown in Table I. The bode plot of grid side PCS admittance is shown in Fig. 4, where all four terms of the admittances contain non-passive frequency region. In the non-passive region, the admittance acts as a negative conductor which reduces the damping capability of the system and can potentially lead to unstable conditions. For the coupling admittances Y_{dq} and Y_{qd},

TABLE I. ELECTRICAL PARAMETERS

Parameters	Values
DC-link voltage (V_{dc})	200 V
AC phase voltage (V_{ac})	81 V
Current base (I_b)	15 A
Fundamental frequency (f)	60 Hz
Converter filter impedance	L=0.575 mH, R=0.25 Ω
DC-link capacitor (C_{dc})	5400 uF
Control frequency (f_c)	10 kHz
Digital control delay (T_d)	150 us (10 kHz)
PI controller parameter (10 kHz)	k_p=0.027, k_i=12 (f_b=750 Hz)
PLL parameter	k_{pPLL}=0.66, k_i=11.1
Voltage feedforward filter (ω_{vf})	$\omega_{vf} = 2 \times \pi \times 10$ rad/s
Grid side shunt capacitor (C_g)	150 uF
Grid line impedance	L_g=0.575 mH, R_g=0.25 Ω

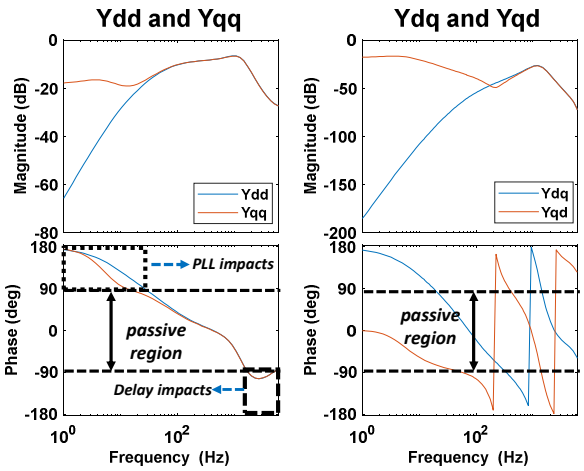


Fig. 4. Grid side PCS output admittance bode plot.

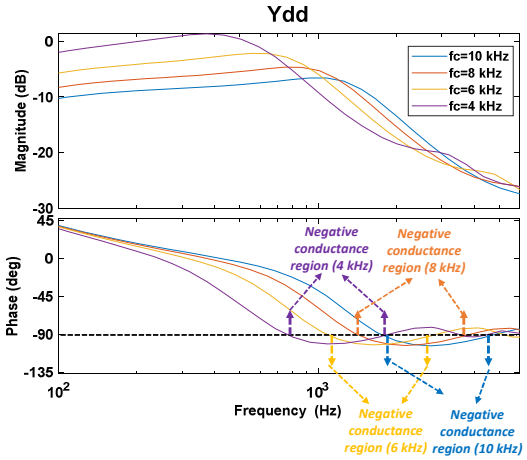


Fig. 5. d axis admittance (Y_{dd}) at different control frequencies (k=1.5).

the magnitude of the negative sequence conductance is much smaller than the negative conductance in the main axis admittances Y_{dd} and Y_{qq}, meaning that the main axis admittances will have larger impacts on the stability. In this paper, the stability analysis will focus on the main axis admittances.

From Fig. 4, the negative conductance of main axis admittances contains two regions, which are impacted by the PLL [16] and control delay, respectively. The PLL impacts can be reduced by changing the PLL bandwidth or utilizing advanced PLL strategies. The delay impacts can be reduced by delay compensation which may complicate the control design or designing the control system with small delay which may also be difficult as the MV converter usually requires complex control system.

IV. Stability Enhancement Solution from HV SiC MOSFET-Based PCS

Due to the fast-switching speed and low switching loss of SiC MOSFETs, compared with Si-based PCS, HV SiC MOSFET-based PCS converters can achieve higher control frequency to move the non-passive region, and leave more flexibility for the controller bandwidth design, which can potentially benefit the system stability.

A. Benefit from Non-Passive Region Moving

From (7), the control delay on each axis is shown in (11)

$$G_{dd,q}(j\omega) = e^{-kT_c s}|_{s=j\omega} = \cos(\omega k T_c) - j\sin(\omega k T_c) \quad (11)$$

where the negative resistance is in the non-passive region $[\frac{f_c}{4k}, \frac{3f_c}{4k}]$ and f_c is the control frequency. Therefore, by increasing the control frequency, the SiC MOSFET-based grid side PCS can move the effective region of control delay to a higher frequency, which may impact the non-passive region of output PCS admittance. Fig. 5 shows the Y_{dd} for 10 kHz, 8 kHz, 6 kHz, and 4 kHz control frequency, respectively. The PI controller parameters (10 kHz parameters are given as an example in Table I) are reduced in proportion to the frequency decrease to ensure the stability of the PCS control loop at different frequencies. According to Fig. 5, the negative conductance range of d axis admittance is moving with the control frequency, meaning that the higher control frequency can move the non-passive region of PCS output admittance to a higher frequency.

The negative conductance can destabilize the system. In an ASMG, if the grid harmonics are located in the non-passive region or grid impedance interacts with the PCS admittance in the non-passive region, the negative conductance will decrease the damping of grid and can cause potential oscillation in the non-passive region. Fortunately, the line impedance in the grid can dampen high-frequency harmonics. In Fig 6, the π model of the grid lines is utilized to explain the line damping capability [18]. When the frequency of harmonic current increases, the impedance of L_{line} increases and the impedance of C_{line} decreases to provide a smaller impedance path, and both changes improve the filtering capability of the harmonic current.

Therefore, when the negative conductance region is increased by the control frequency, the potential oscillation frequency caused by the negative conductance will also increase. When the oscillation frequency is higher, the line damping capability is stronger, and the oscillation impacts are smaller, showing that high control frequency can enhance the grid stability by moving the non-passive region of the PCS admittance to high frequencies.

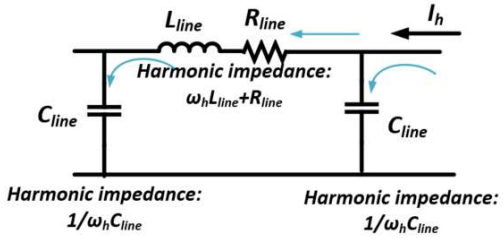


Fig. 6. π model of the main grid line.

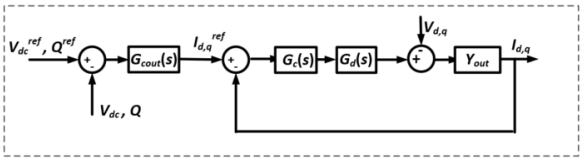


Fig. 7. Simplified control loop for control bandwidth impact analysis.

B. *Benefit to Control Bandwidth from System Stability Perspective*

Based on the admittance derivation in (9), the controller matrix $\boldsymbol{G_c}$ is in the main part of the admittance that can potentially impact the non-passive region of the admittance. The design of the controller parameters can determine the control bandwidth of the PCS. A PCS with higher control bandwidth can respond faster to the grid transients, which will benefit the ASMG dynamic performance.

Next, an examination of the impact of $\boldsymbol{G_c}$ on the PCS output admittance is conducted. The control diagram in Fig. 3 is simplified to that shown in Fig. 7, where all the disturbances are ignored and only the main control loop is kept. The simplified output admittance can be derived in (12):

$$Y_{PCSgsp} = \frac{1}{\frac{1}{Y_{out}} + G_c G_d}, \tag{12}$$

where all the terms in (12) are scalars and Y_{out} is shown in (13).

$$Y_{out} = \frac{1}{sL + R} \tag{13}$$

Therefore, combining (11)-(13), the simplified output admittance can be derived in (14)

$$Y_{PCSgsp} = \frac{1}{sL + R + \left(k_p + \frac{k_i}{s}\right)(e^{-kT_c s})} \tag{14}$$

Then in the frequency domain, it can be written as:

$$Y_{PCSgsp}(j\omega) = \frac{1}{A + jB} \tag{15}$$

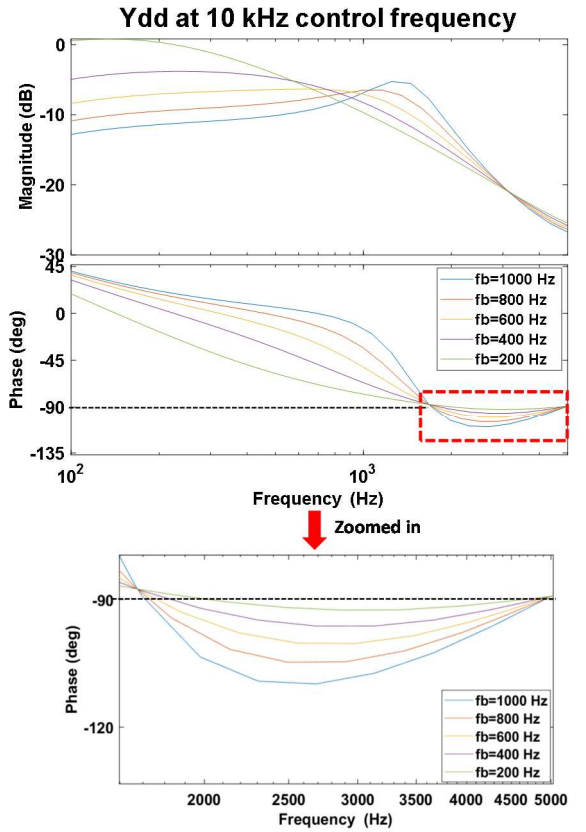
where

$$A = k_p \cos(\omega k T_c) - \frac{k_i}{\omega}\sin(\omega k T_c) + R \tag{16}$$

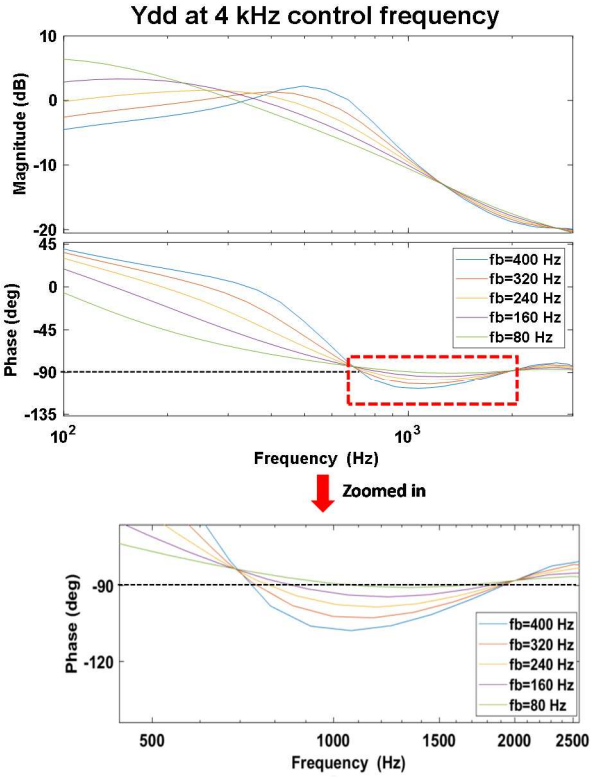
$$B = \omega L - k_p \sin(\omega k T_c) - \frac{k_i}{\omega}\cos(\omega k T_c) \tag{17}$$

Based on (15)-(17), in the non-passive region the real part of the output admittance is determined by the controller parameters, non-passive region frequency, and filter resistance. From (17), two preliminary conclusions can be drawn based on this derivation:

- The non-passive region may be avoided by reducing the controller parameters to meet (18).



(a)



(b)

Fig. 8. Y_{dd} for different control bandwidths: (a) 10 kHz control frequency; (b) 4 kHz control frequency.

- The negative conductance value and phase are also impacted by the frequency of non-passive region (when ω is larger, $\frac{k_i}{\omega}$ is smaller, ωL is larger).

$$R \geq \max\left|k_p \cos(\omega k T_c) - \frac{k_i}{\omega}\sin(\omega k T_c)\right| \qquad (18)$$

Although these conclusions are drawn based on a simplified control diagram, it can also be known that applying smaller control parameters k_p, k_i and locating the non-passive region at higher frequency can potentially reduce the negative sequence conductance in the non-passive region to benefit the system stability. However, smaller k_p and k_i usually mean smaller control bandwidth, meaning that the interaction stability may limit the controller bandwidth.

On the other hand, the frequencies of the non-passive region can also impact the negative sequence conductance value. For the HV SiC MOSFET-based PCS, the non-passive region is moved to higher frequency range, compared with the Si-based PCS, which results in potentially lower negative conductance in the non-passive region, which leaves more margin for the controller bandwidth design.

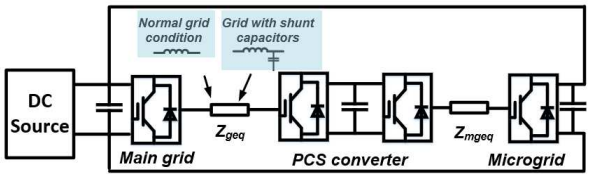
The bode plot of PCS output admittance in (8) with different control parameters at 4 kHz and 10 kHz are shown in Fig. 8, where the phase margin for the controller is designed at 90° and the control bandwidth decreases. When the control frequency is 10 kHz, the worst phase at 1 kHz control bandwidth is around -110°; When the control frequency is 4 kHz, the worst phase at 400 Hz control bandwidth is around -108°. Also, at 10 kHz, when the control bandwidth is 400 Hz, the worst phase is only -96°. With same control bandwidth, the non-passive region area decreases when the control frequency increases. Therefore, considering the interaction stability, the higher control frequency can leave more margin for the control bandwidth design.

V. Experimental Demonstration

Experimental verifications are realized on a converter-based HTB [13]. The configuration and hardware setup are shown in Fig. 9. The main grid and microgrid are emulated by two-level converters, both for a normal grid condition and for a grid connected with shunt capacitor conditions are emulated. In the testing, the line is emulated with an inductor. The shunt capacitors are applied to emulate a reactive power compensator, which may cause potential oscillations. The parameters are summarized in Table I. Two main cases are applied to demonstrate the non-passive region moving as well as the control bandwidth impacts with considering the interaction stability.

A. Stability Enhancment by Non-Passive Region Moving

Based on the grid line impedance, inverter impedance and shunt capacitance in Table I, two resonant points are 581 Hz and 784 Hz, meaning that if the non-passive region has



(a)

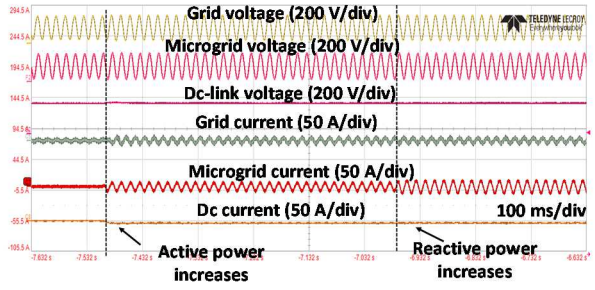
(b)

Fig. 9. PCS experimental testing: (a) testing architecture; (b) hardware

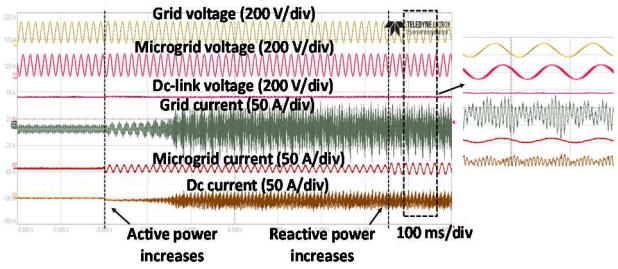
intersection with these two frequencies, oscillations may occur. The grid side PCS is tested at 4 kHz and 10 kHz, where the corresponding non-passive regions of 4 kHz operation and 10 kHz operation are [666.7 Hz, 2000 Hz] and [1666.7 Hz, 5000 Hz], respectively. Therefore, the non-passive region of 4 kHz will intersect with the oscillation point, while the 10 kHz operation will not.

Four cases are tested, and the results are shown in Fig. 10. In Fig. 10 (a) and (b), the grid side PCS is operating at 4 kHz with 300 Hz designed control bandwidth. In Fig. 10(a), no shunt capacitors are applied, and in Fig. 10(b), shunt capacitors are applied. The results show that when the shunt capacitors are applied, the PCS resonates with the main grid while no oscillation occurs when there is no capacitor. The results demonstrate that the PCS control loop is stable, and the oscillation comes from the system interaction.

The testing of 10 kHz operation with 750 Hz control bandwidth is shown in Fig. 10(c) and (d), where shunt capacitors are not applied in Fig. 10(c) and applied in Fig. 10(d). The results show that the grid side PCS can work with the main grid without oscillation for both conditions. The FFT analysis for shunt capacitor applied cases of grid current is shown in Fig. 11, where for 4 kHz case, the oscillation occurs at 815 Hz while the 10 kHz case does not have obvious oscillation other than at the switching frequency. Therefore, the testing results can demonstrate that the non-passive region moves with as the control frequency increases, which may avoid oscillation at low frequency.



(a)



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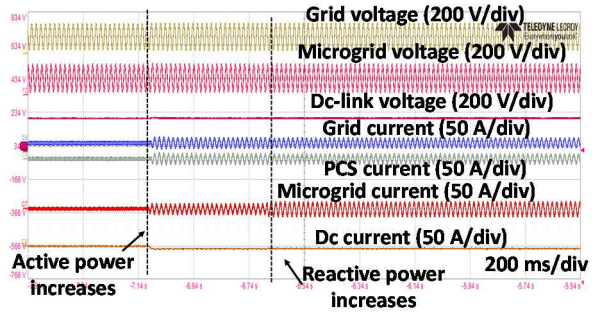
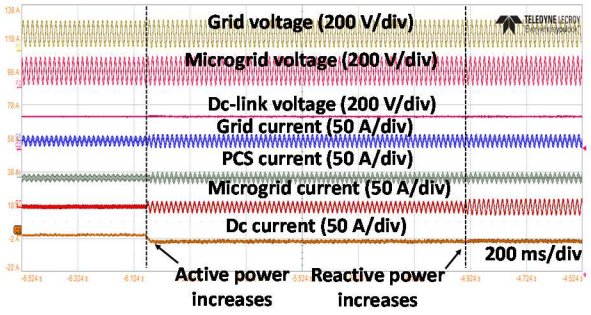


(c)

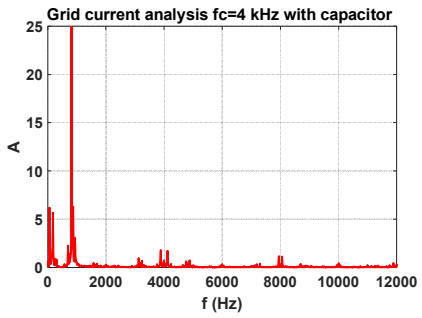


(d)

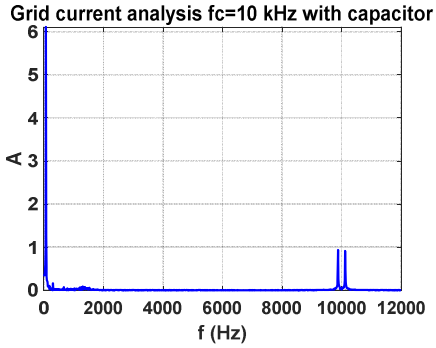
Fig. 10. PCS experimental testing: (a) without shunt capacitor (4 kHz, stable); (b) with shunt capacitor (4 kHz, unstable); (c) without shunt capacitor (10 kHz, stable); (d) with shunt capacitor (10 kHz, stable).

B. System Stability Requirements on PCS Control Bandwidth Design

The second testing is realized under 4 kHz by changing the control bandwidth. The control bandwidths for three cases are 400 Hz, 300 Hz, and 200 Hz, respectively. Test results are shown in Fig. 12. When a shunt capacitor is applied, the oscillation is dampened with the control bandwidth decreasing,

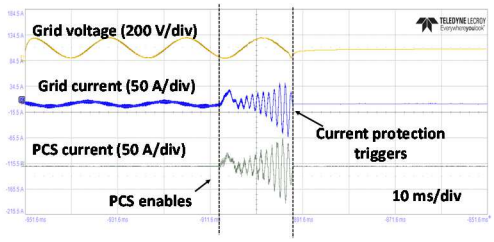


(a)



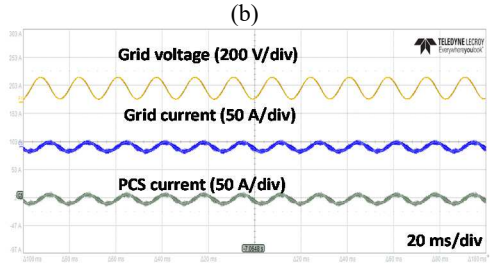
(b)

Fig. 11. FFT analysis of grid current: (a) with shunt capacitor (4 kHz, unstable); (d) with shunt capacitor (10 kHz, stable).



(a)

(b)



(c)

Fig. 12. Control bandwidth changing at 4 kHz with shunt capacitor: (a) 400 Hz bandwidth; (b) 300 Hz bandwidth; (c) 200 Hz bandwidth.

showing that low control bandwidth can result in better interaction stability. When the control bandwidth is 400 Hz, the oscillation increases and the current keeps increasing. Eventually, the current protection of the emulators is triggered. When the control bandwidth is 300 Hz, the current oscillation also exists but it will not trigger the protection with the same threshold, meaning the damping at this bandwidth is better than 400 Hz. When the control bandwidth is 200 Hz, there is no oscillation observed, showing that the interaction will limit the control bandwidth. In order to increase the control bandwidth, the control frequency needs to be increased.

VI. Conclusion

In this paper, the stability enhancement capability resulting from using a HV SiC MOSFET-based ASMG PCS is analyzed and demonstrated. Based on the analysis of PCS decoupling capability and output admittance derivation, potential interaction stability issues are stated including that the control delay in PCS control loops may cause harmonic instability issues under certain grid conditions. To solve this harmonic issue, either smaller control delay or smaller control bandwidth is required, where SiC devices show advantages compared to similar rated Si devices.

By utilizing HV SiC MOSFET-based PCS with high control frequency, the interaction instability can be eliminated, since it can move the non-passive region in the admittance of PCS to higher frequency to be away from the grid interaction zone. Additionally, high control frequency can provide more flexibility on control bandwidth design considering the interaction stability limitations. By examining several different grid conditions, control frequency and control bandwidth during experimental verifications on a converter-based HTB, the stability enhancement of SiC MOSFET-based PCS is demonstrated.

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