Paralleling Operation of 10 kV SiC MOSFET-Based Modular Multi-Level Converters (MMCs) for Scalable Asynchronous Microgrid Power Conditioning System

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***Abstract*—An asynchronous microgrid (ASMG) with silicon carbide (SiC) MOSFET-based power conditioning system (PCS) is an attractive option for future microgrids, which can potentially improve microgrid dynamic performance and grid power quality. To support future microgrids' needs for higher power, scaling PCS power via paralleling multiple modules or converters is a potential solution. In this paper, a strategy for scalable ASMG PCS operation is proposed. MMC-based PCSs are implemented to demonstrate the proposed strategy, including MMC paralleling operation analysis and corresponding control functions. Experimental results are provided to demonstrate the scalable PCS operation at 25 kV rated voltage.**

Keywords—Asynchronous microgrid, modular multilevel converter, converter paralleling, power conditioning system, medium voltage converter, high voltage, SiC MOSFET.

I. INTRODUCTION

Medium voltage (MV) ASMGs with PCSs are attracting more and more research attention [1-2]. In an ASMG, as shown in Fig. 1, a back-to-back connected converter-based PCS is applied as the microgrid interface, which can improve the microgrid dynamic performance [3-4], support grid voltage [5], etc. With the development of high voltage (HV, >3.3 kV) SiC devices [6-7], the HV SiC MOSFET-based PCS is a potential solution for ASMG implementation as it can realize high operation efficiency and power density, and achieve high control bandwidth [8-10].

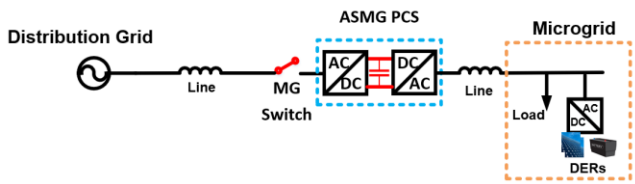


Fig. 1. ASMG concept

For ASMG applications, existing research has focused on the PCS implementation and system-level benefit demonstration. In order for the technology to be demonstrated in the field, the PCS scalability and reliability are necessary concerns, especially for future large and complex microgrids. One of the key solutions for these issues is paralleling multiple PCS subunits, which can achieve higher PCS power rating to support larger microgrids and promote the ASMG resilience.

MMCs have been utilized in ASMGs as PCSs due to their natural modularity, high-quality output voltage and other advantages [2,11]. Numerous research attention has been paid on MMCs, including hardware design, circulating current control, modulation, etc. [12-13]. However, little research has focused on the MMC paralleling, especially for SiC MOSFET-based MV MMCs, as it has challenges on high control complexity, MV operation, and strong electromagnetic interference (EMI) noises.

In this paper, 10 kV SiC MOSFET-based MMCs are applied as the building blocks for the PCSs to demonstrate the scalable PCS operation. The scalable PCS operation strategy is described first. Then the theoretical analysis of MMC paralleling is conducted including basic operation as well as the common mode circulating current (CMCC) study. A leader-follower structure [14] based closed-loop control is designed and experimental verifications are provided for a 13.8 kV ASMG.

The rest of the paper is organized as: Section II proposes the PCS scalable operation strategy. Section III discusses the operation of MMC-based sub-PCS for scalable PCS operation. Section IV provides the hardware setup and experimental results, and conclusions are drawn in Section V.

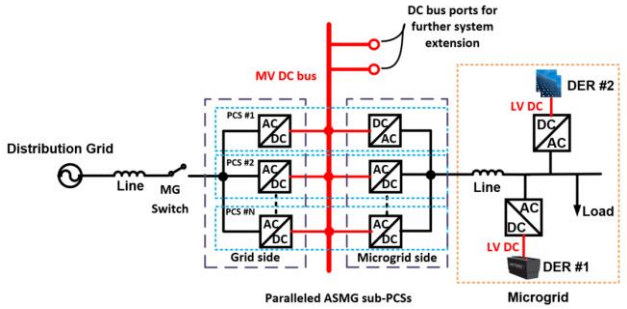


Fig. 2. Proposed scalable ASMG PCS operation strategy.

II. ASMG PCS Scalability Strategy

In an ASMG, the proposed PCS scalability plan is shown in Fig. 2, where the scaled PCS is composed of *N* paralleled single sub-PCSs. In the proposed strategy, instead of directly paralleling multiple back-to-back connected sub-PCSs, both the ac sides and dc sides of the PCS are connected to realize the power scaling. Based on this structure, all the grid side ac/dc converters can form a group to share the active power, provide reactive power, and regulate dc-link voltage. The microgrid side dc/ac converters also work as a group to establish microgrid voltage and support the load.

Compared with only paralleling the ac sides of PCSs, the proposed scalable strategy can bring more redundancy to the whole system. For example, in the proposed strategy, if one of the grid side ac/dc inverters fails, the corresponding microgrid side dc/ac inverter can still operate by obtaining power and dc voltage from the common dc-link. In the meantime, all the dc sides of the PCSs are connected to form a MV dc bus, which can be used for potential further system expansion such as forming dc microgrids to realize a hybrid microgrid [15].

However, one of the main challenges of the proposed PCS scalability strategy is that the common ac-dc-ac connected sub-PCSs require more complicated control strategies for PCS operation. In this paper, the microgrid PCS is applied to demonstrate the operation of the proposed scalability strategy.

III. MMC Paralleling Operation for Scalable PCS

A 10 kV SiC MOSFET-based, 5-level MMC is applied as a building block for one sub-PCS [11]. As shown in Fig. 3, scalable PCS operation is demonstrated on the microgrid side with two sub-PCSs, which requires paralleling operation of MMC. In this part, the control of MMC paralleling is discussed from system level that enables ASMG scalable operation and individual MMC converter level.

A. ASMG Scalable Operation Required Control

In grid-connected mode, the microgrid side PCS works as a grid-forming source to support microgrid voltage and frequency. To realize grid-forming capability, two main types of approaches may be applied for paralleled inverters, which

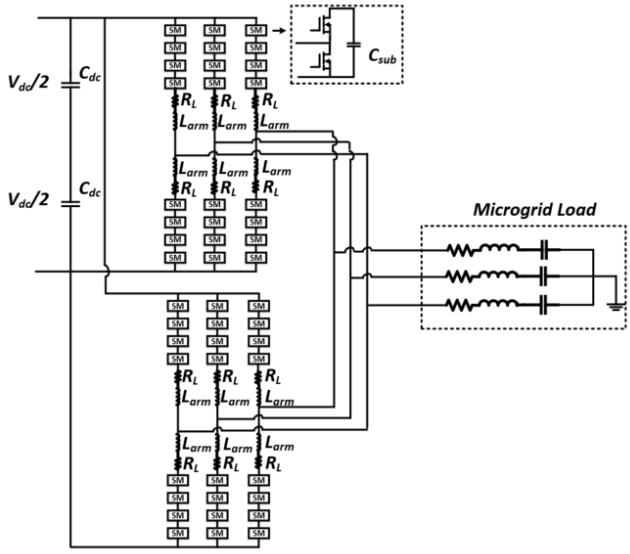


Fig. 3. MMC-based PCS paralleling structure

are decentralized approach such as droop control [16] and centralized approach like leader-follower structure based paralleling strategy [14]. The decentralized approaches only require local information, and each converter can independently serve as a grid-forming source. However, interaction instability and power sharing accuracy are potential issues [17]. Centralized approaches can realize more accurate power sharing; however, a communication link is required.

For PCS paralleling, since all the microgrid side dc/ac converters form as a group to support the microgrid, leader-follower based paralleling structure is applied, which is shown in Fig. 4. One of the microgrid side sub-PCSs works as the leader to form a dual-loop control. For the outer loop, the microgrid voltage is regulated to generate the total current references for both leader and follower converters and provide the microgrid with stable frequency. The inner loop of the

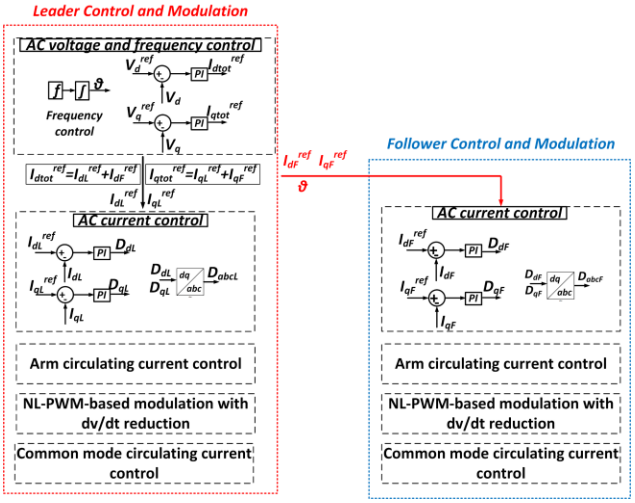


Fig. 4. Leader-follower-based MMC paralleling control strategy.

leader shares part of the current with the follower. The follower only contains the current loop and controls the output current to the reference received from the leader. For the two sub-PCS paralleling case, the relationships of current references are shown as:

$$I_{dtot}^{ref} = I_{dL}^{ref} + I_{dF}^{ref} \tag{1}$$

$$I_{qtot}^{ref} = I_{qL}^{ref} + I_{qF}^{ref} \tag{2}$$

where I_{dtot}^{ref} and I_{qtot}^{ref} are the total current required by the microgrid load, and current references with subscript *L* and F represent references for leader and follower, respectively. For both the leader and the follower, the allowable current references ranges are described in (3) and (4)

$$\begin{cases} \sqrt{\left(I_{dL}^{ref}\right)^2 + \left(I_{qL}^{ref}\right)^2} \le I_L^{max} \\ \sqrt{\left(I_{dF}^{ref}\right)^2 + \left(I_{qF}^{ref}\right)^2} \le I_F^{max} \end{cases} \tag{3}$$

$$\begin{cases} \dfrac{I_{dL}^{ref}}{I_{dF}^{ref}} \ge 0 \\ \dfrac{I_{qL}^{ref}}{I_{qF}^{ref}} \ge 0 \end{cases} \tag{4}$$

where I_L^{max} and I_F^{max} are the maximum current rating for the leader and follower. Equation (4) represents that the current references assigned to leader and follower should have the same direction to avoid circulating current between the leader and follower. Within the allowable operation range, the current sharing between leader and follower can be flexible.

B. MMC Operation Required Control

1) Second Order Circulating Current Control

In one phase leg of an MMC shown in Fig. 5, the submodule voltage can be modelled as a controlled voltage source. Taking phase *a* as an example and ignoring the arm inductor voltage drop, the arm voltages and currents can be expressed as:

$$\begin{cases} v_{aU} = \dfrac{V_{dc}}{2} - V_a \sin(\omega t) \\ v_{aL} = \dfrac{V_{dc}}{2} + V_a \sin(\omega t) \end{cases} \tag{5}$$

$$\begin{cases} i_{aU} = \dfrac{I_{dc}}{3} + \dfrac{I_a}{2}\sin(\omega t + \theta) \\ i_{aL} = \dfrac{I_{dc}}{3} - \dfrac{I_a}{2}\sin(\omega t + \theta) \end{cases} \tag{6}$$

where V_a and I_a are the voltage and current magnitude of phase *a*, $cos\theta$ is the power factor of phase *a*. According to (5) and (6), the power on upper and lower arms can be written as:

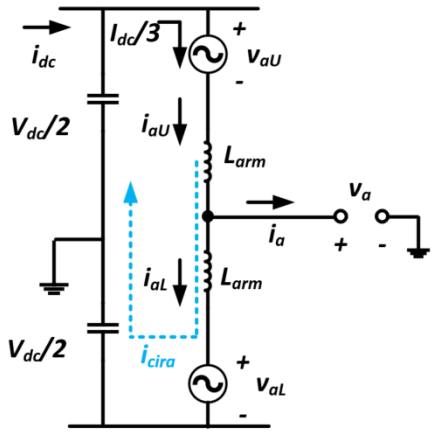


Fig. 5. One phase leg model of MMC arm.

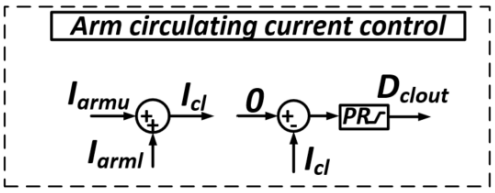


Fig. 6. Control diagram for arm circulating current control.

$$\begin{cases} p_{aU} = v_{aU} i_{aU} = \dfrac{V_{dc} I_{dc}}{6} + A_1(\omega) - A_2(2\omega) \\ p_{aL} = v_{aL} i_{aL} = \dfrac{V_{dc} I_{dc}}{6} - A_1(\omega) - A_2(2\omega) \end{cases} \tag{7}$$

where

$$\begin{cases} A_1(\omega) = \dfrac{V_{dc} I_a}{4}\sin(\omega t + \theta) - \dfrac{V_a I_{dc}}{3}\sin(\omega t) \\ A_2(2\omega) = -\dfrac{V_a I_a}{4}[\cos(2\omega + \theta) - \cos(\theta)] \end{cases} \tag{8}$$

$A_2(\omega)$ is a second order term that can cause second voltage ripple on the submodule capacitors to result in second order circulating current denoted as I_{cira} on upper and lower arms, leading to arm current distortion and extra losses. Therefore, second order circulating current control is applied to suppress the circulating current, which is shown in Fig. 6 [2].

The control is realized in stationary coordinates, where the upper and lower arm current is added to calculate the circulating current within each arm. The circulating current is directly regulated by a proportional-resonant (*PR*) controller with resonant frequency at double line frequency. As shown in Fig. 4, the second order circulating current control is applied to all the arms in both the leader and follower.

2) Impoved Nearest-Level Pulse Width Modulation

For HV SiC MOSFET-based PCS, MV converter can be realized with small numbers of submodule, which can reduce the control system complexity. For MMCs with limited submodule number, nearest-level pulse width modulation (NL-PWM) is an attractive solution as it can realize the submodule

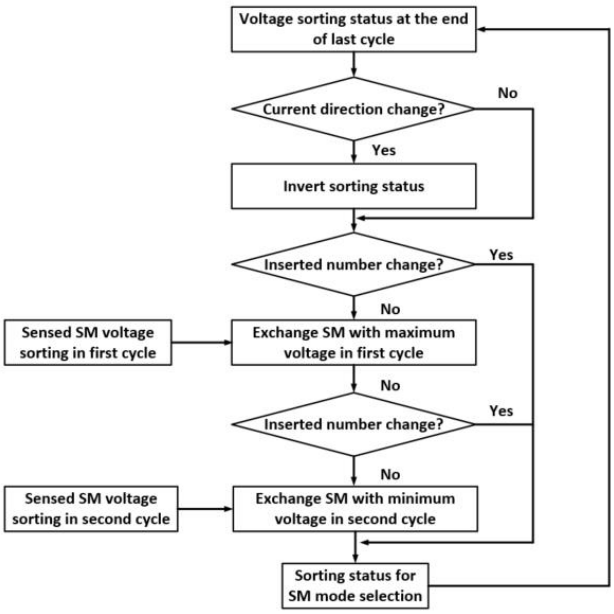


Fig. 7. Enhanced voltage sorting strategy for NL-PWM.

voltage balancing in an easy way as well as maintain output voltage quality [11]. However, the high *dv/dt* induced by switching HV SiC MOSFETs poses challenges to the control noise immunity. Therefore, to mitigate the *dv/dt* impact, the voltage sorting strategy of NL-PWM is improved, which is shown in Fig.7 [18].

The enhanced voltage sorting strategy limits changing of submodule voltage sorting status to at most once in one control cycle. A two-step approach is applied: in the first control cycle, the submodule with the maximum voltage exchanges status with the one in the last cycle; in the second control cycle, the sorting of submodule with minimum voltage exchanges the status with the one in last cycle. Moreover, the inserted numbers for upper and lower arms are determined by (9)

$$k_{inserted} = floor\left(\frac{v_{armu.l}^{ref}}{V_{dc}}N\right) \tag{9}$$

where *floor*(*x*) is the function to find the next smaller integer of *x*. $v_{armu.l}^{ref}$ are the generated voltage references for upper and lower arms. In the voltage sorting strategy, if the inserted number changes, the sorting status will remain the same for one cycle to further reduce the *dv/dt*. After the sorting process is completed, the NL-PWM approach is applied to generate gate signals and realize voltage balancing control. The detailed *dv/dt* analysis under different voltage sorting statuses and inserted number change are discussed in [18].

C. CMCC Control

According to the proposed scalability strategy in Fig. 2, the common dc-link connection provides a low impedance path for CMCC, which is shown in Fig. 8. The CMCC may include both low-frequency components and high-frequency components.

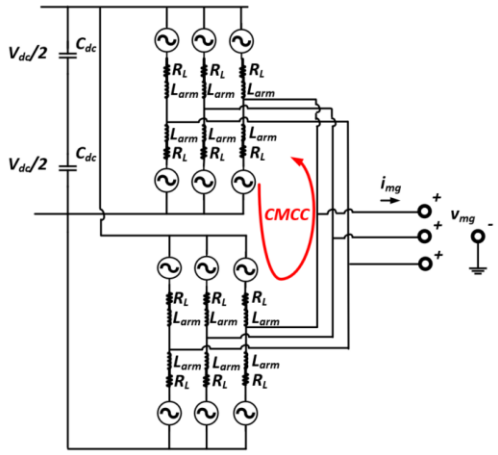


Fig. 8. CMCC path for paralleled MMCs.

The arm inductors can eliminate the high frequency CMCC while the low-frequency CMCC cannot be well filtered by the arm inductors as their impedances are relatively low at low frequencies. To deal with the low-frequency CMCC, control solution should be applied.

Third order harmonic current is the commonest low frequency CMCC, which is generated by the third order harmonic voltages. In the existing literatures, third order components have been observed in the output voltages of MMCs [19-20]. The third order harmonics in the MMC output voltage may result from different reasons such as MMC operation, control algorithms, and modulation strategies. However, the third order voltage harmonics have not attracted enough research attention as MMCs usually do not provide paths for third order harmonic currents.

In the MMC paralleling operation, to eliminate the potential third order CMCC, a *PR*-controller based third order harmonic regulator is applied, which is shown in Fig. 9, where the CMCC of each MMC is defined in (10):

$$I_{CM} = i_a + i_b + i_c \tag{10}$$

The CMCC controller directly regulates the CMCC of each MMC to be 0 with *PR* controller resonating at 180 Hz in the stational coordinates.

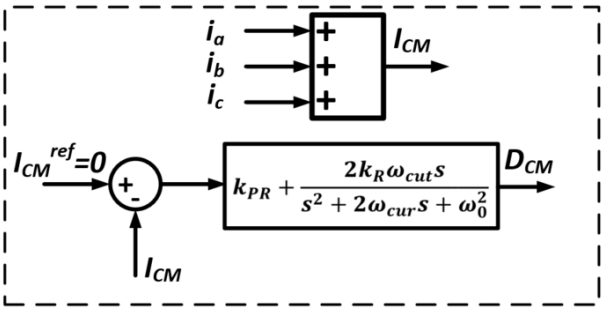


Fig. 9. Proposed controller for CMCC.

IV. Experimental Validations

A. Hardware Setup

1) Testing System Setup

The experimental setup realizes the circuit in Fig. 3 with the parameters in Table I. The hardware implementation is shown Fig. 10. The setup includes six phase-leg cabinets for two three-phase MMCs. The microgrid is modelled as a combination of resistor and capacitor loads. The tested MMCs are composed of 10 kV SiC MOSFETs with rated voltage at 25 kV dc, and 13.8 kV ac line to line voltage, which are implemented for actual ASMG PCSs. The control frequency of each MMC is 10 kHz.

2) Control Architecture and Controller Hardware

The control architecture of the two paralleled MMCs is shown in Fig. 11, where each MMC has its own central and phase controllers. The enable/stop commands and power sharing strategies are issued from the human-machine interface (HMI) to the central controller. The central controller realizes the voltage and current control to issue duty cycles to phase controllers, and the phase controller generates the PWM signals to its corresponding phase-leg cabinet.

The HMI communicates with the central controller through serial communication; the central controller links with the phase controller with optical fibers because the phase controller is in the converter cabinet, where the electromagnetic noise is severe because of fast switching by the high voltage SiC devices. By using optical fibers, the direct noise impacts on the central controller can be isolated.

To realize the proposed leader-follower structure, serial communication link is set up between central controllers, where the leader generates the total current references and shares references with the follower based on HMI commands. Besides current references, the phase angle of the leader is also shared with the follower through communication.

The controller hardware implementation is shown in Fig. 12. The central controller is composed of one DSP f28335 for control calculation and one FPGA (Cyclone IV) for data transfer. The phase controller utilizes the same type of FPGA as well since the FPGA has relatively better noise immunity compared with the DSP.

B. Expermental Results

The testing results are demonstrated from three cases: (1) power sharing change, (2) CMCC control verification, and (3) full voltage operation.

1) Scalable PCS Operation with Power Sharing Change

This operation is demonstrated at +- 6 kV dc voltage, which is shown in Fig. 13. The PCS can form balanced microgrid voltage to support load in the microgrid, showing that the basic MMC operation can be realized. The load current is shared by two MMCs. Before time t_1, two MMCs realize the equal sharing of loads. At time t_1, the sharing references are changed to be

TABLE I. Operation Conditions

Parameters	Values
DC-link voltage (V_{dc})	25 kV
AC line to line voltage (V_{ac})	13.8 kV
Load (RC in series)	R=250 Ω, C=1.25 uF
Line frequency (f)	60 Hz
Arm filter (L and R_L)	L=90 mH, R_L= 5 mΩ
Submodule capacitance (C_{sub})	8.75 μF
Submodule number per arm (N)	4
Control frequency (f_c)	10 kHz

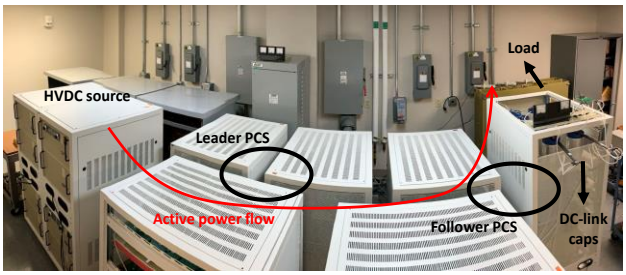


Fig. 10. Testing setup for scalable PCS operation.

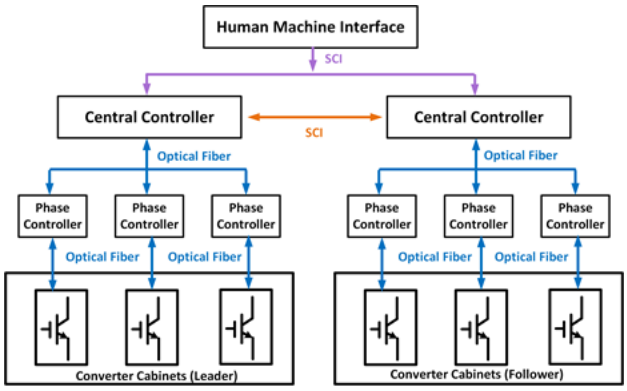
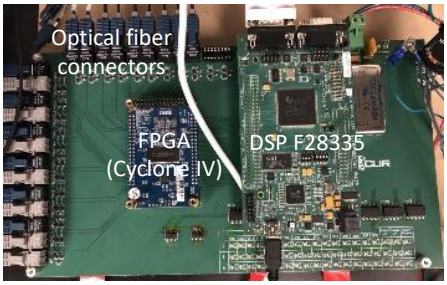
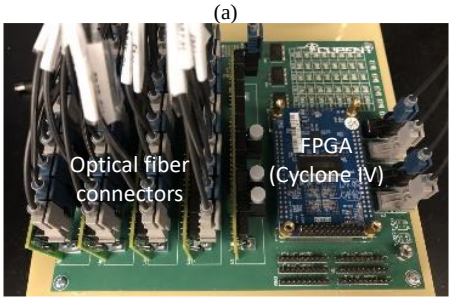


Fig. 11. Parallel PCS control architecture.



(a)



(b)

Fig. 12. Controller hardware: (a) central controller; (b) phase controller.

4:1, meaning that the leader PCS supports 80% of the load while the follower only contributes 20%. The leader PCS current increases from 1.24 A (peak) to 1.98 A (peak), while the follower PCS current decreases from 1.23 A (peak) to 0.5A (peak), following the sharing ratio closely.

Before and after the sharing ratio change, the microgrid voltage and load current keep stable, showing that the proposed leader-follower structure can realize flexible current sharing among sub-PCSs with negligible impacts on the microgrid support.

2) *CMCC Control Verification*

The testing results of CMCC control are shown in Fig, 14, where the testing is conducted at 16 kV dc-link voltage. The load sharing ratio between the leader and the follower is also 4:1. The CMCC control is verified by comparing the leader sub-PCS current when the CMCC control is enabled and disabled. The harmonics analysis of the leader current is shown in Fig. 14(c). The testing results indicate that when the CMCC control is applied, the third order circulating current is diminished by 48.8%, which proves the efficacy of the proposed CMCC control.

3) *Full Voltage Operation*

The rated voltage testing of scalable PCS operation is demonstrated in Fig. 15, where the dc-link voltage of two sub-PCSs is 25 kV and the ac line to line voltage is 13.8 kV which is one of the standard voltage levels for MV distribution grids. The load sharing ratio at full voltage is 1:1. The leader PCS and follower PCS generate the same output current at 2.6 A (peak). The testing results demonstrate that the stable microgrid voltage can be established and accurate current sharing among different sub-PCSs can be realized, showing the proposed control strategy can assist the scalable PCS operation in actual ASMG conditions.

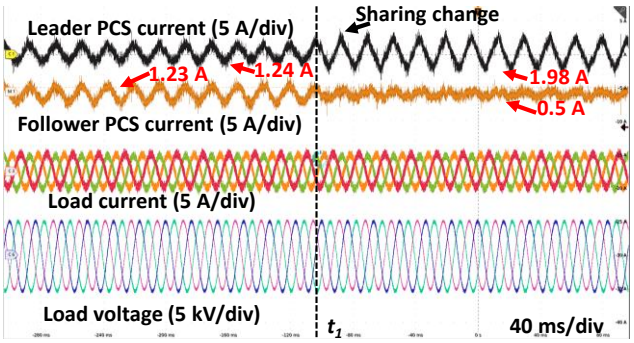
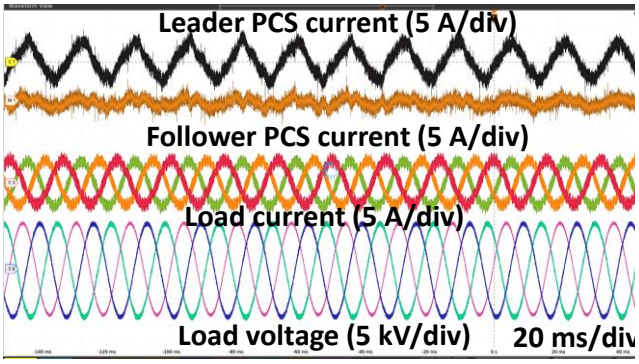


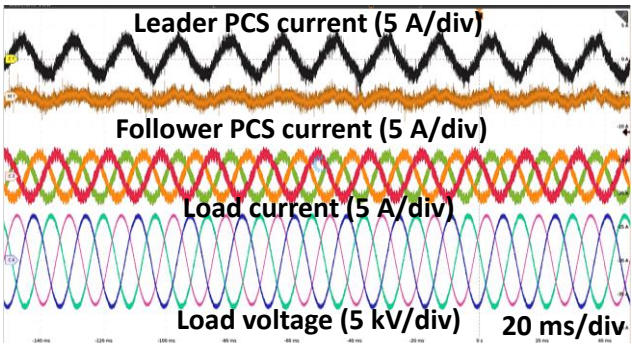
Fig. 13. Testing results of power sharing change.

V. Conclusion

In this paper, a PCS scalable operation strategy is proposed to support future large ASMGs. The 10 kV SiC MOSFET-



(a)



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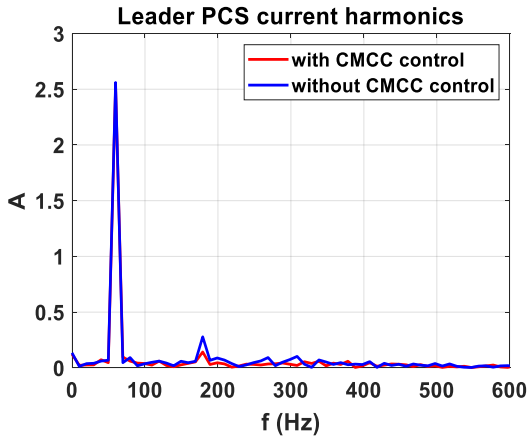

(c)

Fig. 14. Testing results with 4:1 load sharing: (a) without CMCC control; (b) with CMCC control; (c) FFT analysis of phase current.

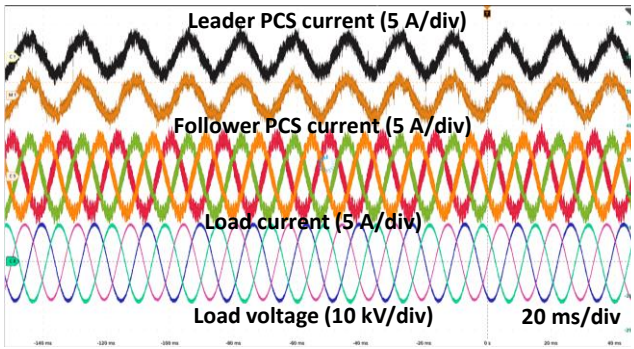

Fig. 15. Testing results at full voltage (25 kV dc, 13.8 kV ac).

based MMCs are applied as the sub-PCSs to demonstrate scalable PCS operation. A leader-follower structure based paralleling control is applied as the system-level power sharing strategy. To realize the paralleling operation, the operation of SiC-based MMC is discussed and the potential circulating current from MMC paralleling is derived. Based on the MMC operation analysis, corresponding control functions are designed, implemented, and tested with two actual PCSs for 13.8 kV ASMGs up to the rated voltage. The testing result demonstrated that the proposed power sharing strategy can realize flexible and accurate power sharing among different sub-PCSs and the proposed CMCC controller can eliminate the third order circulating current.

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