2021 IEEE Applied Power Electronics Conference and Exposition (APEC) | 978-1-7281-8949-9/21/$31.00 ©2021 IEEE | DOI: 10.1109/APEC42165.2021.9487192

An Inrush Current Limit Method for SiC-based Multi-level Grid-connected Converter During Low-Voltage Ride-Through

Haiguo Li[1*], Zihan Gao[1], Shiqi Ji[1], Yiwei Ma[1], Fred Wang[1,2]
[1] Min H. Kao Department of Electrical Engineering and Computer Science, the University of Tennessee, Knoxville, TN, USA
[2]Oak Ridge National Laboratory, Oak Ridge, TN, USA
*hli96@vols.utk.edu

***Abstract*—Low-voltage ride-through is one of the grid requirements for grid-connected converters, and during the transient of grid voltage change, a large inrush current could be induced due to the control delay of the converter. This inrush current is more severe in SiC-based multi-level converters due to the small filter inductance, which is selected based on harmonics consideration. In this paper, a PWM mask method is used to limit the inrush current of a cascaded H-bridge-based grid-connected converter during the transient of grid voltage change. Simulation and experiment results are provided to validate this method.**

Keywords—Inrush current, low-voltage ride-through, grid voltage drop, PWM mask

I. INTRODUCTION

During the transient of the grid voltage change, the output voltage of the grid-connected converter cannot be immediately changed due to the control delay. As a result, the voltage on the filter inductor will be large, and then an inrush current occurs. Compared to Si-based two-level converters, the SiC-based multi-level converter will have a larger inrush current during the grid voltage change because of the smaller filter inductance, which is selected based on the grid-side current harmonic requirement. The large inrush current may saturate the inductor or even damage devices. Increasing the filter inductance can reduce the inrush current, but also increase the converter size, weight, and cost.

In [1, 2], active and reactive current injection strategy is discussed during low-voltage ride-through (LVRT) to support the grid voltage and reduce the risk of overcurrent, but this method cannot limit the inrush current at the transient of grid voltage change. In [3], an adaptive low-pass notch PLL is used to get a fast and smooth transient response to the grid voltage change, but the inrush current during the transient is still out of the control range of the controller. In [4], the dc-link voltage is regulated during LVRT to keep a high modulation ratio and to reduce the high-frequency harmonics, but the dc-link voltage regulation is slow compared to the grid voltage drops. In [5], a negative sequence voltage is added to the positive sequence voltage when a fault happens, but the control delay still impacts the controller response time to the grid voltage drop, and an inrush current still exists. Therefore, existing papers mainly focus on the steady-state (millisecond to the second range) operation of the converter when facing an LVRT, but the transient (microsecond to millisecond range) performance of the converters during the grid voltage change has been rarely discussed.

The PWM mask method is previously proposed in [6] to limit the overload and short circuit current of a three-phase inverter. However, no detailed analysis of the PWM mask threshold value setting, considering the control loop delay, has been introduced, which is important when the rate of rising of the inrush current is high. Besides, this method has not been tested under the grid-connected mode.

In this paper, the PWM mask method is used to limit the inrush current of a SiC-based multi-level grid-connected converter during the transient of grid voltage change, and the threshold value setting is analyzed considering the control loop delay.

The rest of this paper is organized as follows. First, the inrush current during grid voltage drop is theoretically analyzed in Section II. Then, the operating principle of the PWM mask method and the threshold value determination are introduced in Section III. In section IV, the method is verified with simulation first and then with experimental test. Finally, this paper concludes with Section V.

II. INRUSH CURRENT ANALYSIS DURING GRID VOLTAGE CHANGE

A. Converter Configuration

As shown in Fig. 1, a three-phase four-wire power conditioning system (PCS) converter is used to connect an 850V DC grid to the 13.8 kV AC grid. The PCS converter needs to meet the grid requirements, of which LVRT is an important one. Therefore, the design of the PCS converter, especially the DC/AC stage, has to meet grid requirements. Since this paper focuses on the DC/AC stage, the DC/DC stage is simplified.

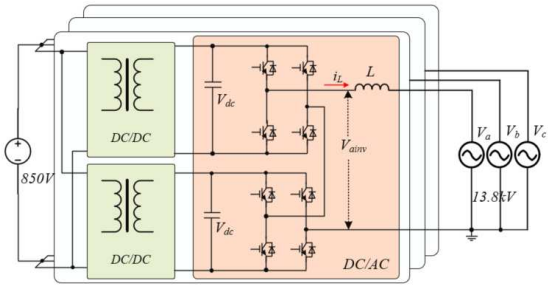

Fig. 1. The PCS converter topology.

The converter parameters of the DC/AC stage are shown in Table I. The AC side filter inductance is around 0.009 p.u., which is selected based on the grid-side current harmonic requirement, thanks to the high switching frequency and multi-level voltage. Because of the three-phase four-wire configuration, the following analysis is based on phase A, but it can be easily extended to phase B and C.

TABLE I. SYSTEM PARAMETERS

Parameter	Value
AC grid root mean square (RMS) voltage (phase-to-neutral) V_a, V_b, V_c	8 kV
MV DC-link voltage V_{dc}	6.7 kV
PCS converter power rating	100 kVA
Filter inductor L	44 mH (0.009 p.u.)
Switching frequency of each device	10 kHz
Sampling and control frequency	10 kHz

B. Inrush Current Analysis

To analyze the inrush current during the transient of the grid voltage change, the differential equation of the filter inductor L is derived as

$$V_L = L\frac{di_L}{dt} = V_{ainv} - V_a \quad (1)$$

and the averaged inductor voltage during a switching cycle is

$$\bar{V}_L = L\frac{d\bar{i}_L}{dt} = \mathrm{d}\cdot V_{dc} - V_a \quad (2)$$

where d is the instantaneous duty cycle of the DC/AC converter.

In the steady-state operation, since the filter inductance is only 0.009 p.u., the averaged voltage drop between the inductor is small, and the averaged output voltage of the converter should be close to the grid voltage.

The grid voltage, V_a, could suddenly change due to some grid transients, such as grid faults, motor starting, etc. However, even though with grid voltage feedforward control, it will take some time, Td, for the converter controller to detect and respond to the grid voltage change. During the short period, before the controller response to the grid voltage change, the duty cycle, d, is almost constant. Then, the inductor voltage becomes large due to the sudden change of V_a, which will induce the rapid increase of the inductor current. The inductor current change can be calculated as

$$\Delta i_L = \frac{d\cdot V_{dc} - V_{a\_after}}{L}T_d \approx \frac{V_{a\_before} - V_{a\_after}}{L}T_d \quad (3)$$

where V_a_before and V_a_after are the grid voltages before the voltage change and the voltage after the voltage change, respectively.

The converter controller generally has a process as shown in Fig. 2. In each control cycle, the converter will first sample the variables, including DC-link voltages, grid AC voltages, inductor AC currents, etc. Then, the controller executes the control calculation to get the new duty cycle for the next PWM period. However, the calculated duty cycle cannot be updated to the PWM pulses until the next duty cycle reload action happens.

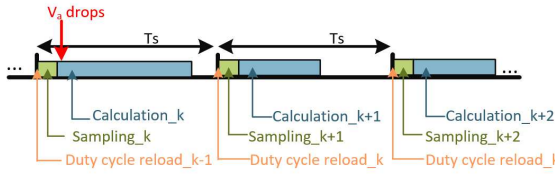

Fig. 2. Converter controller delay.

Therefore, the worst case happens when the grid voltage, V_a, drops just after the kth sampling has been completed. The controller detects the grid voltage drop through the voltage sampling in the $(k+1)^{th}$ cycle. Then, the controller calculates the new duty cycle, which will be updated to the PWM output in the $(k+2)^{th}$ period. In this case, the control delay, T_d, is around two control cycles, i.e.

$$T_d = 2T_s \quad (4)$$

Besides, based on the feedforward realization of the converter controller, the controller delay could be longer than $2T_s$ if the grid voltage detection, mostly the phase-locked loop (PLL), is slow. Also, any low pass filter in the grid voltage sampling circuit or any digital filter in the converter controller will increase the control delay too.

To estimate the inrush current in the converter, assume the grid voltage suddenly drops from the normal peak voltage to 0. The control delay is assumed to be two times of the control cycles. Then, the inductor current change during that period is

$$\Delta i_L = \frac{V_{ainv} - V_a}{L}\times T_d = \frac{8\ \mathrm{kV}\times\sqrt{2} - 0}{44\ mH}\times 200\ us = 51.4\mathrm{A} \quad (5)$$

and its per-unit value is

$$\Delta i_{L\_pu} = \frac{\Delta i_L}{I_{base}} = \frac{51.4\mathrm{A}}{5.9A} = 8.7\ p.u. \quad (6)$$

The real inrush current could be higher than the calculated value, considering the saturation of the filter inductor. The large inrush current during the transient of grid voltage change could either trigger the converter protection or damage the converter components, such that the converter will fail to ride through the grid low voltage. Therefore, a method is needed to reduce the inrush current to survive that transient period.

III. OPERATING PRINCIPLE OF THE PWM MASK METHOD

A. PWM Mask Operating Principle

The PWM mask method can be used to limit the inrush current during the transient of grid voltage drop though temporarily mask the PWM pulses. The working process of the PWM mask method is shown in Fig. 3. The inductor currents are measured and used to compare with two preset threshold values, I_{th1} and I_{th2}, to determine if the PWMs need to be masked or released.

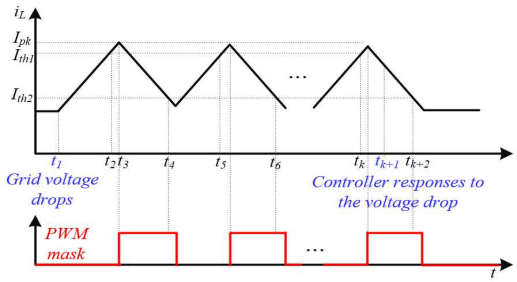

Fig. 3. Inductor current during PWM mask period.

When the PWMs are masked, all devices are turned off, and the inductor current flows through the device diode, and the output voltage of the converter is

$$V_{ainv} = -2V_{dc} \quad (7)$$

Then, the inductor current differential equation during the control delay period becomes

$$\frac{di_L}{dt} = \begin{cases} \frac{V_{a\_before} - V_{a\_after}}{L} & \text{if PWMs are released} \\ \frac{-\text{sign}(i_L)2V_{dc} - V_{a\_after}}{L} & \text{if PWMs are masked} \end{cases} \quad (8)$$

so when PWMs are masked, the inductor current will decrease because of the opposite sign of the converter output voltage.

The whole process is as follows. At time $t=t_1$, the grid voltage, V_a, drops to 0, and the inductor current starts to increase due to the large voltage difference between the inductor terminals. At time $t=t_2$, the inductor current exceeds the preset threshold value 1, I_{th1}, but PWMs will not be masked until $t=t_3$ due to the control loop delay. At $t=t_3$, all PWMs in the phase are masked, and the inductor current starts to decrease. At $t=t_4$, the inductor current drops below the preset threshold value 2, I_{th2} ($I_{th2}<I_{th1}$), the PWMs are released after a short delay caused by the current detection and gate driver control loop. However, at this moment, the converter controller may still have not detected or responded to the grid voltage drop, then the inductor current will increase again. Until $t=t_{k+1}$, the converter controller starts to regulate its output voltage based on the new grid voltage, V_{a_after}, the inductor current can be regulated by the controller after the PWMs are released.

B. PWM Threshold Value Determination

To limit the inrush current effectively and make the converter ride through the grid low voltage period, several aspects need to be considered when determining the PWM mask threshold values I_{th1} and I_{th2}.

First, the larger PWM mask threshold value needs to be smaller than the minimum converter instantaneous overcurrent protection values, including both the hardware instantaneous overcurrent protection, $I_{ins\_OC\_hw}$, such as device desaturation protection, and software instantaneous overcurrent protection, $I_{ins\_OC\_sw}$. This aims at preventing the converter from trip during the transient of the grid voltage change. Since the overcurrent protection values are within the device capability, this criterion can also make sure that the inrush current does not exceed the device capability.

Then, the larger PWM mask threshold value should be larger than the maximum peak current of the converter in the steady-state operation. Otherwise, the PWM mask method will be falsely triggered, and it will increase the converter switching loss and impact the control.

Therefore, the PWM mask threshold value should be within the range of:

$$I_{pk\_steadystate} < I_{th1} < \min(I_{ins\_OC\_hw}, I_{ins\_OC\_sw}) \quad (9)$$

and some margin is necessary to get effective control of the PWM mask.

In addition, although hardware protection can be realized by the PWM mask method, there is still some control delay, which results in a larger inrush current limitation than the preset threshold value, as shown in Fig. 3.

A general control loop of the PWM mask is shown in Fig. 4, and the total PWM mask control delay consists of the current sensor delay, the current sampling regulation circuit delay, the comparator delay, signal transmission delay, the PWM mask logic delay, the PWM signal transmission delay, as well as the device switching delay. Therefore, the total PWM mask control delay is

$$T_{d\_pwm\_mask} = t_3 - t_2 = \sum_{k=1}^{8} t_{dk} \quad (10)$$

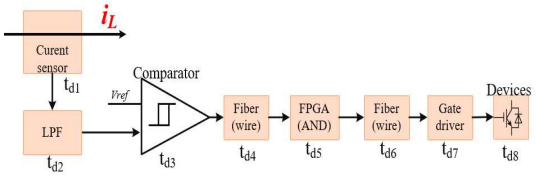

Fig. 4. PWM mask control loop.

Therefore, to limit the inrush current at a certain value, I_{pk}, the PWM mask threshold value, I_{th1}, should be

$$I_{th1} \approx I_{pk} - \frac{V_{a\_before} - V_{a\_after}}{L} T_{d\_pwm\_mask} \quad (11)$$

The smaller PWM mask threshold value, I_{th2}, is used to release the PWMs, and it works with I_{th1} to generate a hysteresis comparator so that the device will not be frequently turned on and off, avoiding large device switching losses. Also, the smaller the I_{th2}, the longer the inductor current needs to decrease after the PWMs are masked, and therefore the less the device switching actions. Therefore, the range of I_{th2} could be

$$0 < I_{th2} < I_{th1} \quad (12)$$

However, a too-small I_{th2} may lead to a longer transient since the PWMs may not be released when the converter controller has responded to the grid voltage drop.

IV. Simulation and Experimental Test Results

A. Simulation Results

The PWM mask method is emulated together with the PCS DC/AC converter in MATLAB/Simulink. To estimate the device thermal performance, a device thermal model has also been developed. The PWM mask threshold values, I_{th1} and I_{th2}, are set at 3 p.u. and 1.5 p.u. respectively, considering the delay of the PWM mask control loop.

Fig. 5 shows the waveforms of the grid voltages, inductor currents, and the device junction temperature during the LVRT transient without PWM mask function. The grid voltage suddenly drops from 1.1 p.u. to 0.4 p.u. at t=0.15 s, and the inrush current reaches 6.5 p.u. due to the control delay and the small inductance. The device junction temperature increases to around 190 ºC, which is out of the device's maximum junction temperature, 175 ºC, listed in the datasheet.

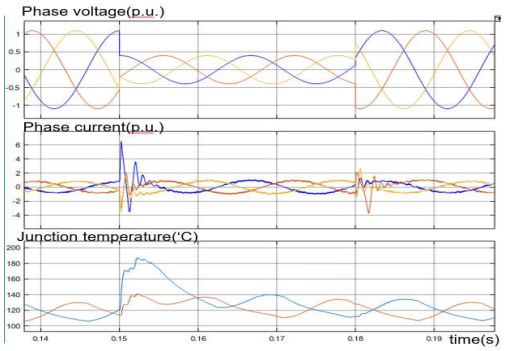

Fig. 5. Simulation waveforms of LVRT transient without PWM mask

With the PWM mask method, the inrush current is effectively limited. As shown in Fig. 6, with the PWM mask

method, the inrush current is limited at 3 p.u., and the device junction temperature does not have a large increase.

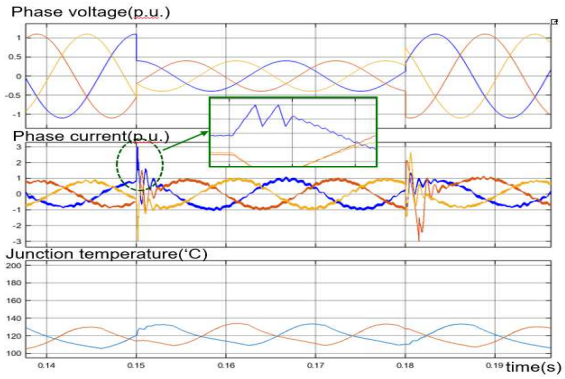

Fig. 6. Simulation waveforms of LVRT transient with PWM mask

B. Experimental Results

The method has been tested on a single-phase small-scale prototype setup, as shown in Fig. 7. The test setup diagram is shown in Fig. 8, and the parameters are summarized in Table II.

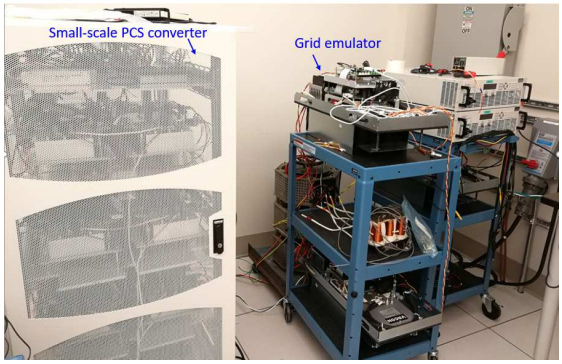

Fig. 7. Experiment setup.

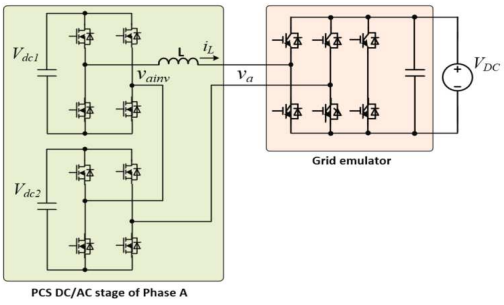

Fig. 8. Experiment setup diagram.

A three-phase converter works as a grid emulator, and it is supplied from the DC-link by a DC power supply. To get a fast grid voltage change, open-loop control is adapted in the grid emulator controller. During the steady state, the grid emulator output 90 V RMS (1 p.u.) / 60 Hz voltage. During the fault period, the grid voltage suddenly drops to 18 V RMS (0.2 p.u.) and keeps that low voltage for 0.5 seconds.

The small-scale PCS converter also consists of two full bridges, and the AC side of the PCS converter is directly connected to the grid emulator. Without the DC/DC stages, the single-phase PCS converter operates as a STATCOM. The PCS converter is controlled to ride through the whole period of the grid voltage variation, and the PWM mask threshold values I_{th1} and I_{th2} are set at 25 A and 15 A, respectively.

TABLE II. EXPERIMENT TEST SETUP PARAMETERS

Parameter		Value
Grid emulator	DC voltage V_{DC}	150 V
	AC RMS voltage v_a	90 V
	AC voltage frequency	60 Hz
	Switching, sampling, and control frequency	10 kHz
PCS Converter	Rated phase RMS current	3.2 A
	DC-link voltage V_{dc1}=V_{dc2}=100V	6.7 kV
	filter inductor L	0.67mH (0.0084p.u.)
	Switching, sampling and control frequency	10 kHz
	PWM mask threshold value I_{th1}	25 A
	PWM release threshold value I_{th2}	15 A

The waveforms of the grid voltage v_a, PCS converter output PWM voltage v_{ainv}, the PWM mask signal, the inductor current i_L, and the PCS DC-link voltages V_{dc1} and V_{dc2} are recorded during the test.

Fig. 9 shows the waveforms without the PWM mask function. It can be found that when the grid voltage suddenly drops from 1 p.u. to 0.2 p.u., an inrush current of 54 A occurs. When the grid voltage recovered, an inrush current of 60 A also occurs.

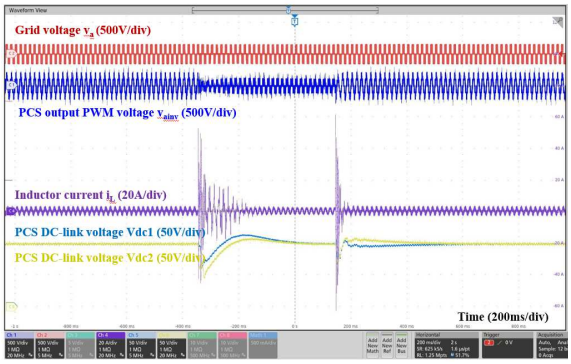

Fig. 9. LVRT transient without PWM mask method.

Fig. 10 shows the zoomed-in of the grid voltage drop in Fig. 9, and Fig. 11 shows the zoomed-in of the grid voltage recovery in Fig. 9. From the two figures, it can be found that at the moment of the grid voltage change (drop/recover), the PCS output voltage does not change too much. It takes around 200 us (2 control cycles) for the PCS converter controller to detect and respond to the grid voltage change and the inrush current. In the PCS converter controller, the second-order general integrator (SOGI) based PLL is used. This type of PLL is relatively slow to detect the grid voltage change, so it overall takes around 6 control cycles (i.e., 600 us) for the PCS converter to fully respond to the grid voltage change.

Besides the inrush current, there is also a large current control transient and a large DC-link voltage variation, which will also impact the converter operation.

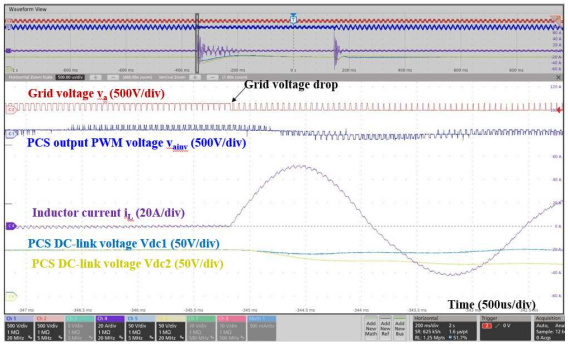

Fig. 10. Zoomed in of the grid voltage drop transient in Fig. 9.

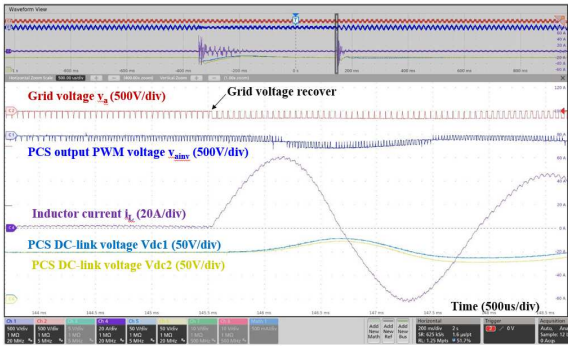

Fig. 11. Zoomed in of the grid voltage recovery transient in Fig. 9.

Then, another test was conducted with the PWM mask function. As shown in Fig. 12, the inrush currents during both the grid voltage drop and the grid voltage recovery are around 26 A, which are significantly reduced compared to the previous values.

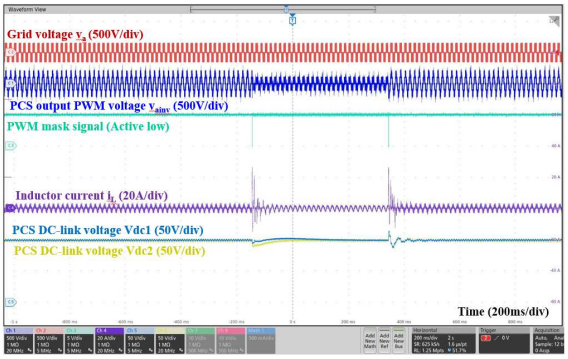

Fig. 12. LVRT transient with the PWM mask method.

Fig. 13 shows the zoomed-in of the grid voltage drop transient in Fig. 12. At the moment of grid voltage drop, the inductor current starts to increase, when the current value equals the PWM mask threshold value, Ith1, the PWM mask signal becomes low, and it is detected by an FPGA, in which the PWMs are masked. It can also be found that when the PWMs are masked, the inductor current flows through the MOSFET body diodes, and the PCS converter output voltage equals $-(V_{dc1}+V_{dc2})$. During the PWM mask period, the inductor current decreases, and when it is around the 2nd threshold value Ith2, the PWM mask signal goes high and the PWMs are released. The PWMs are masked three times before the converter fully responds to the grid voltage drop.

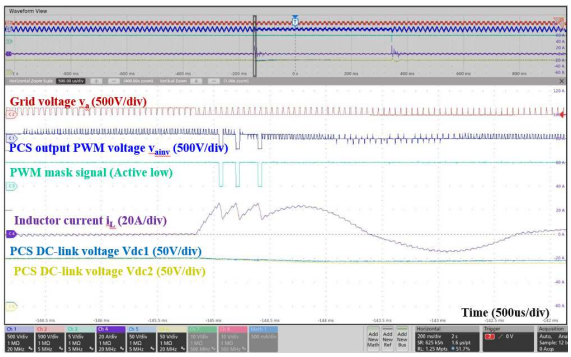

Fig. 13. Zoomed-in the grid voltage drop transient in Fig. 12.

Fig. 14 shows the zoomed-in figure of the grid voltage recovery transient in Fig. 12. Similar to what happened during the grid voltage drop, when the inductor current increases to around 25 A, the PWMs are masked, and when the current decreases to be less than 15A, the PWMs are released.

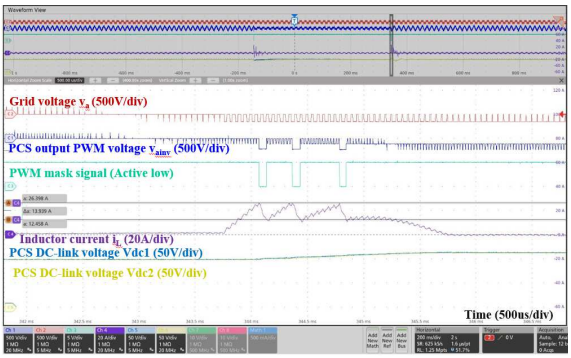

Fig. 14. Zoomed-in of the grid voltage recovery transient in Fig.

With the PWM mask method, not only the inrush currents are limited, the current transients and the DC-link voltage variation are reduced too. Therefore, these tests verified the function of the PWM mask method.

V. CONCLUSION

In this paper, a PWM mask method is introduced to limit the inrush current of a grid-connected converter during the transient of grid voltage change. The main reason for the inrush current is the sampling and control delay of the converter controller. Since the converter cannot immediately respond to the grid voltage change, the voltage difference between the filter inductor induces an inrush current. With a certain grid voltage change and constant control delay, the smaller the inductance the higher the inrush current. The PWM mask method limits the inrush current by temporarily mask the PWM pulses. The determination of the PWM mask threshold values needs to consider the converter steady-state operation condition, protection, as well as the PWM mask control loop delay. In both the simulation and experimental tests, the inrush currents during the grid voltage change are limited to the designed values, which verified the method.

ACKNOWLEDGMENT

This work was supported primarily by the Advanced Manufacturing Office (AMO), United States Department of Energy, under Award no. DE-EE0008410. This work made use of the shared facilities of the Engineering Research

Centre Program of the National Science Foundation and the Department of Energy under NSF Award no. EEC-1041877. The authors would like to acknowledge the contribution of Southern Company and Powerex.

REFERENCES

[1] C. Lee, C. Hsu, and P. Cheng, "A Low-Voltage Ride-Through Technique for Grid-Connected Converters of Distributed Energy Resources," *IEEE Transactions on Industry Applications,* vol. 47, no. 4, pp. 1821-1832, 2011.

[2] H. Chen, C. Lee, P. Cheng, R. Teodorescu, and F. Blaabjerg, "A Low-Voltage Ride-Through Technique for Grid-Connected Converters With Reduced Power Transistors Stress," *IEEE Transactions on Power Electronics,* vol. 31, no. 12, pp. 8562-8571, 2016.

[3] D. Shin, K. Lee, J. Lee, D. Yoo, and H. Kim, "Implementation of Fault Ride-Through Techniques of Grid-Connected Inverter for Distributed Energy Resources With Adaptive Low-Pass Notch PLL," *IEEE Transactions on Power Electronics,* vol. 30, no. 5, pp. 2859-2871, 2015.

[4] G. Ding F. Gao, H. Tian, C. Ma, M. Chen, G. He, Y. Liu., "Adaptive DC-Link Voltage Control of Two-Stage Photovoltaic Inverter During Low Voltage Ride-Through Operation," *IEEE Transactions on Power Electronics,* vol. 31, no. 6, pp. 4182-4194, 2016.

[5] P. Piya, M. Ebrahimi, M. Karimi-Ghartemani, and S. A. Khajehoddin, "Fault Ride-Through Capability of Voltage-Controlled Inverters," *IEEE Transactions on Industrial Electronics,* vol. 65, no. 10, pp. 7933-7943, 2018.

[6] D. Liu, A. Hu, G. Wang, and J. Guo, "Triple-loop-controlled overload or short circuit current limiter and protection for three phase inverter," in *2009 International Conference on Applied Superconductivity and Electromagnetic Devices*, 2009, pp. 201-205.