Decoupling Capacitor Design for Multi-Inverter Based Grid Emulator System

Yunting Liu
CURENT, Department of EECS
The University of Tennessee
Knoxville, TN, USA
yliu193@utk.edu

Haiguo Li
CURENT, Department of EECS
The University of Tennessee
Knoxville, TN, USA

Yiwei Ma
CURENT, Department of EECS
The University of Tennessee
Knoxville, TN, USA

Jingxin Wang
CURENT, Department of EECS
The University of Tennessee
Knoxville, TN, USA

Leon M. Tolbert
CURENT, Department of EECS
The University of Tennessee
Knoxville, TN, USA

Fred Wang
CURENT, Department of EECS
The University of Tennessee
Oak Ridge National Laboratory
Knoxville, TN, USA

Kevin L. Tomsovic
CURENT, Department of EECS
The University of Tennessee
Knoxville, TN, USA

***Abstract*— CURENT's grid emulator contains multiple inverters to mimic the behaviors of several grid elements. The filtering inductor at the ac terminal of an inverter filters out the switching ripple current. However, the voltage on the point of common coupling (PCC) still contains switching harmonics. A decoupling capacitor at the PCC can effectively suppress the switching ripple voltage and improve voltage quality of the grid emulator. This paper provides a reduced order model of the multi-inverter system. With this reduced model, the PCC voltage harmonics can be derived. The decoupling capacitor of the PCC is designed to suppress the switching ripple based on the reduced model. Simulation and experimental results are provided to validate the proposed model and the decoupling capacitor design.**

Keywords—multi-inverter, power quality, filter design, decoupling capacitor

I. INTRODUCTION

Real-time grid emulator is a tool that tests grid behaviors in a real-time manner. CUENT's power electronics based reconfigurable real-time grid emulator, also known as the hardware test-bed (HTB), is developed as a unique emulation platform to overcome various issues with digital emulators and conventional hardware-based emulators [1]. The HTB uses identical power electronics inverters to emulate the external properties of typical grid elements. Each inverter is programmed digitally with the built-in digital signal processors (DSPs) to behave as various devices/equipment in an electrical system, including sources, loads, and transmission/distribution equipment.

The HTB system contains multiple inverters interconnected to an ac link as shown in Fig. 1. The point of common coupling (PCC) voltage is distorted by switching frequency harmonics since the PWM pulses from each inverter are coupled to the interconnection point. The contribution of each inverter depends on the filtering inductance of the inverter and the interconnection configuration.

To clean the high frequency noise at the PCC, LCL filters are commonly adopted [2]. However, the LCL network may interact with the inverter controller and lead to inherent instability at the resonance frequency [3]–[6]. Theoretically, a line resistor can help with voltage/current resonant damping. However, the line resistance increases the system power loss. To avoid this additional power loss, a virtual damping resistor has been proposed in [7]–[9] to replace the actual resistor and improve the system stability. However, each of the aforementioned methods is based on a specific scenario, and normally the more complicated method is not suitable for a large interconnected system such as the HTB system. Also, the control method in literature is not suitable for CURENT's HTB system since the HTB inverter control needs to be focused on emulating grid elements.

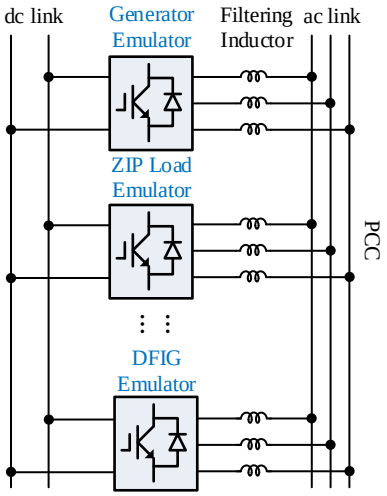

Fig. 1. System configuration of hardware test-bed.

This work was supported primarily by the Engineering Research Center Program of the National Science Foundation and the Department of Energy under NSF Award Number EEC-1041877 and the CURENT Industry Partnership Program.

This paper provides a simple decoupling capacitor design that is suitable for multi-inverter based HTB system that can effectively clean the high frequency components on the inverter PCC. The reduced order model of the HTB system is derived in this paper. The decoupling capacitor design is based on the reduced order model of the system. This paper is organized as follows. The system configuration is provided in Section II. The reduced order modeling of multi-inverter system is derived in Section III. The decoupling capacitor design is provided in Section IV. The simulation and experiment results are provided in Section V to validate the effectiveness of the derived model and designed decoupling capacitor.

II. System Configuration

The grid elements are emulated by inverters in the HTB system. The inverters are programmed to have the same steady-state and dynamic response as the emulated grid elements. The grid elements could be considered as either current-controlled voltage sources or voltage-controlled current sources. For example, the impedance-type load is normally emulated by a voltage-controlled current source inverter. The inverter measures the terminal voltage to derive the corresponding terminal current as if the terminal voltage is fed to an impedance-type load. The selection of voltage-control or current-control depends on the property of the emulated elements and the scenarios. In general, either the inverter terminal voltage or current is measured as the input of the emulated grid element model. Then, the resulting current or voltage reference is calculated from the grid element model and given to the inverter controller to track. This ensures that the inverter behaviors follow the emulated grid element model. The general emulation principle is shown in Fig. 2.

The available active-type grid elements in the HTB system include synchronous generators [10], [11], wind turbine generators [12], PV generators [13], battery energy storage system (BESS) [14] and flywheel energy storage systems [15]. The available passive-type grid elements include induction motor [16], constant impedance/current/power loads (i.e. ZIP load) [17], nonlinear load [18], as well as power electronics interfaced loads (motor drives, EV chargers, data center). The available transmission or distribution level elements are ac lines [19] (including series-compensated lines), shunt compensators (static synchronous compensators or STATCOM) and HVDC converters. Certain types of bus and line faults can also be emulated.

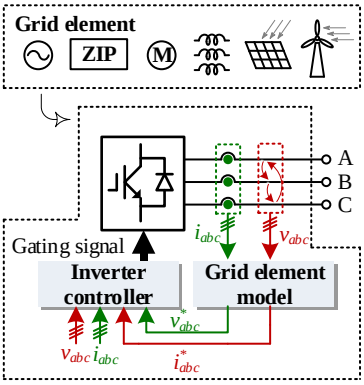

Fig. 2. Emulator operating principle.

III. Modeling of Multi-Inverter System

The multi-inverter system under analysis of this paper is shown in Fig. 3. Each full-bridge inverter has identical filtering inductor L_f. All inverters are connected to the decoupling capacitor C_f. Each inverter can be modeled as a voltage source that contains a broad spectrum of harmonics. To simplify the analysis, the circuit is modeled in single-phase form. The modeling of the multi-inverter system is shown in Fig. 4. Since the decoupling capacitor C_f is in delta connection, the equivalent single-phase decoupling capacitor $C_d = \sqrt{3}C_f$.

Using superposition, the PCC voltage can be formulated as the sum of each individual voltage source's impact on the PCC. Fig. 5 shows the equivalent circuit of the superposition method. The PCC voltage can be formulated as,

$$V_{PCC}^{(n)} = \frac{\frac{1}{\frac{n-1}{sL_f}+sC_d}}{\frac{1}{\frac{n-1}{sL_f}+sC_d}+sL_f} \cdot V_n \tag{1}$$

$$V_{PCC}^{(n)} = \frac{1}{1+sL_f\left(\frac{n-1}{sL_f}+sC_d\right)} \cdot V_n \tag{2}$$

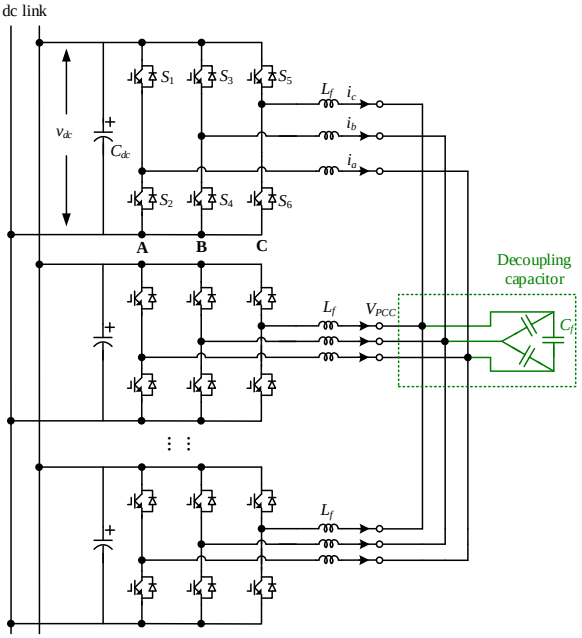

Fig. 3. Multi-inverter system in HTB.

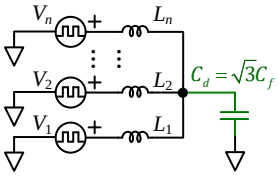

Fig. 4. Modeling of the multi-inverter system.

$$V_{PCC}^{(n)} = \frac{1}{n+s^2 L_f C_d} \cdot V_n \tag{3}$$

where $V_{PCC}^{(n)}$ is the resulting PCC voltage from inverter n, n is the number of the inverter, V_n is the voltage output of each inverter n, L_f is the filtering inductance, and C_d is the decoupling capacitor. Therefore,

$$V_{PCC} = \frac{1}{n+s^2 L_f C_d} \cdot (V_1 + V_2 + \cdots + V_n) \tag{4}$$

Assume that all inverter PWM outputs have similar spectra. Eq. (4) can be simplified as

$$V_{PCC} = \frac{n}{n+s^2 L_f C_d} \cdot V_{inv} \tag{5}$$

where V_{inv} is the PWM voltage output from one inverter.

IV. Decoupling Capacitor Design

Eqs. (1)-(5) formulated the PCC voltage with decoupling capacitors. If no decoupling capacitors are placed on the PCC, the equivalent circuit becomes Fig. 6. The PCC voltage can be formulated as,

$$V_{PCC}^{(n)} = \frac{1}{n} \cdot V_n \tag{6}$$

Therefore,

$$V_{PCC} = \frac{1}{n} \cdot (V_1 + V_2 + \cdots + V_n) \tag{7}$$

Assume that all inverter PWM outputs have a similar spectrum. Eq. (7) can be simplified as

$$V_{PCC} = V_{inv} \tag{8}$$

where V_{inv} is the PWM voltage output from one inverter. From (8), the spectra of PCC voltage are the same as inverter PWM voltage output. Therefore, the PCC voltage has a wide spectrum of harmonics especially at the switching frequency.

With the decoupling capacitor on the PCC, the transfer function becomes (5). The magnitude of the harmonic component on PCC voltage is

$$V_{PCC} = \frac{n}{n-\omega^2 L_f C_d} \cdot V_{inv} \tag{9}$$

In general, (9) is a monotonically increasing function of ω until the worst case,

$$n - \omega_0^2 L_f C_d = 0 \tag{10}$$

$$\omega_0 = \sqrt{\frac{n}{L_f C_d}} \tag{11}$$

where ω_0 is the resonance frequency. Normally, the magnitude of the switching-frequency harmonic component on the PCC voltage is expected to be limited to less than 5% compared to the fundamental component.

From (9), the magnitude of the fundamental component on the PCC voltage is

$$V_{PCC}^{f} = \frac{n}{n-\omega_f^2 L_f C_d} \cdot V_{inv}^{f} \tag{12}$$

where ω_f is the fundamental frequency. The magnitude of the switching-frequency harmonic on PCC voltage is

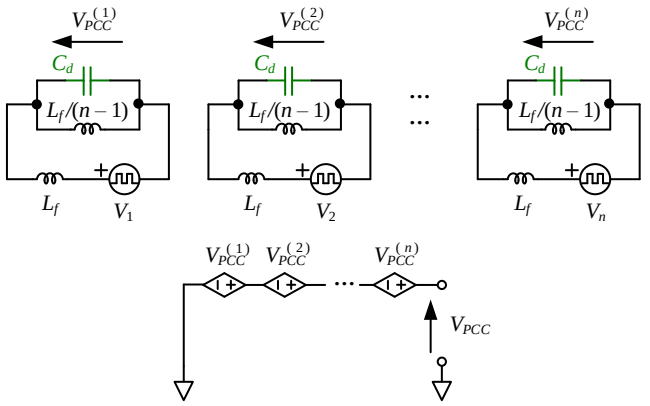

Fig. 5. Equivalent circuit of the superposition method.

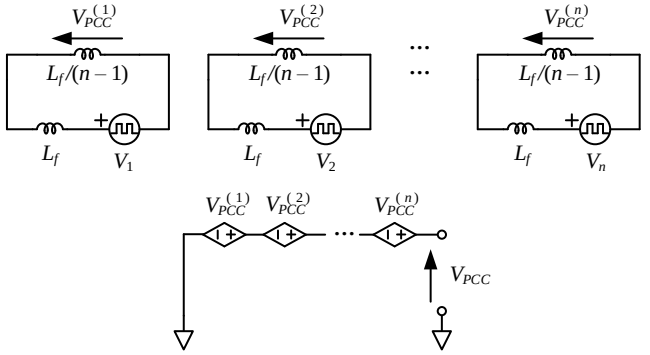

Fig. 6. Equivalent circuit of multi-inverter system without decoupling capacitors.

$$V_{PCC}^{s} = \left|\frac{n}{n-s^2 L_f C_d}\right| \cdot V_{inv}^{s} = \frac{n}{-n+\omega_s^2 L_f C_d} \cdot V_{inv}^{s} \tag{13}$$

where ω_s is the switching frequency. The sign of $n/(n+s^2 L_f C_d)$ becomes negative when the frequency gets higher. Typically, the sign becomes negative at switching frequency ω_s. The switching-frequency component magnitude as a percentage of the fundamental component is,

$$\frac{V_{PCC}^{s}}{V_{PCC}^{f}} = \frac{\frac{n}{-n+\omega_s^2 L_f C_d}}{\frac{n}{n-\omega_f^2 L_f C_d}} \cdot \frac{V_{inv}^{s}}{V_{inv}^{f}} \tag{14}$$

Define $G_{PCC} = V_{PCC}^{s}/V_{PCC}^{f}$ to represent the ratio of the switching harmonics magnitude and the fundamental component magnitude at the PCC. Define $G_{inv} = V_{inv}^{s}/V_{inv}^{f}$ to be the ratio of switching harmonics magnitude and the fundamental component magnitude at the midpoint of inverters

$$G_{PCC} = \frac{\frac{n}{-n+\omega_s^2 L_f C_d}}{\frac{n}{n-\omega_f^2 L_f C_d}} \cdot G_{inv} \tag{15}$$

$$G_{PCC} = \frac{n-\omega_f^2 L_f C_d}{-n+\omega_s^2 L_f C_d} \cdot G_{inv} \tag{16}$$

$$G_{PCC}^{max} > G_{PCC} = \frac{n-\omega_f^2 L_f C_d}{-n+\omega_s^2 L_f C_d} \cdot G_{inv} \tag{17}$$

where G_{PCC}^{max} is the maximum boundary for PCC harmonics.

$$G_{PCC}^{max}\left(-n+\omega_s^2 L_f C_d\right) > G_{inv}\left(n-\omega_f^2 L_f C_d\right) \quad (18)$$

$$\omega_s^2 L_f C_d G_{PCC}^{max} + \omega_f^2 L_f C_d G_{inv} > G_{PCC}^{max} n + G_{inv} n \quad (19)$$

$$\left(\omega_s^2 G_{PCC}^{max} + \omega_f^2 G_{inv}\right) L_f C_d > \left(G_{PCC}^{max} + G_{inv}\right) n \quad (20)$$

$$L_f C_d > \frac{\left(G_{PCC}^{max}+G_{inv}\right)n}{\left(\omega_s^2 G_{PCC}^{max}+\omega_f^2 G_{inv}\right)} \quad (21)$$

$$C_d > \frac{\left(G_{PCC}^{max}+G_{inv}\right)n}{\left(\omega_s^2 G_{PCC}^{max}+\omega_f^2 G_{inv}\right)L_f} \quad (22)$$

Theoretically, the resonant frequency ω_0 should be higher than the switching frequency to maintain system stability.

$$\omega_0 = \sqrt{\frac{n}{L_f C_d}} > \omega_s \quad (23)$$

In actual inverter prototyping, the power loss of the inverters can be modeled as a damping resistance and in turn suppress the resonant at ω_0. Hence, the boundary from (23) is neglected in this paper.

From (22), the range of decoupling capacitor is

$$C_d > \frac{\left(G_{PCC}^{max}+G_{inv}\right)n}{\left(\omega_s^2 G_{PCC}^{max}+\omega_f^2 G_{inv}\right)L_f} \quad (24)$$

Besides the range of decoupling capacitor (24), the decoupling capacitor should not change the emulator behaviors. Each emulator should follow the emulated model and the control. A big decoupling capacitor will significantly change the output behaviors of the grid emulators. Typically, the decoupling capacitor that follows (24) should be small enough and will not change the low frequency components of the output current/voltage of emulators.

V. Experiment Verification

To verify the decoupling capacitor design derived in Section V, a decoupling capacitor with two values are tested. The parameters of CURENT's HTB system are used to find the decoupling capacitor design. The key parameters of the studied HTB system is summarized in Table I. The schematic of the experimental circuit is shown in Fig. 3.

TABLE I. KEY PARAMETERS OF HTB SYSTEM

Number of inverters, n	3
Filtering inductor, L_f	0.5 mH
Switching frequency, ω_s	20 kHz
Fundamental frequency, ω_0	60 Hz
Maximum switching ripple at PCC, $G_{PCC}^{\max}$	50%
Switching frequency component in PWM, G_{inv}	100%
Decoupling capacitor, C_f	0.1 μF, 1 μF

The PCC voltage waveform without decoupling capacitors is shown in Fig. 7. From Fig. 7, the PCC voltage contains rich switching frequency harmonics. Please note that the magnitude of fundamental components (60 Hz) and the magnitude of switching harmonics (20 kHz) are both around 60 V. The ratio

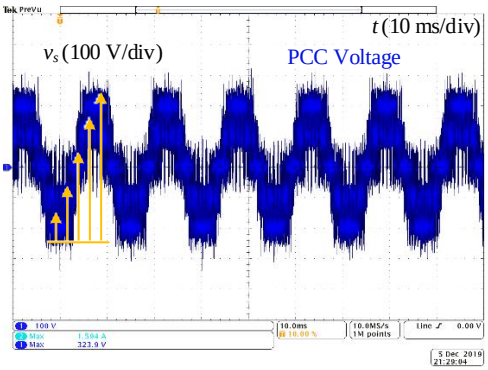

Fig. 7. PCC voltage without decoupling capacitor.

of the switching harmonics and fundamental components is around 100%.

For the system with the configuration summarized in Table I, the range of the decoupling capacitor C_f is should be greater than 1 μF according to (24). To verify the effectiveness of this range, two decoupling capacitors are selected with values of 0.1 μF and 1 μF, where the 0.1-μF decoupling capacitor is out of the desired range and the 1-μF decoupling capacitor is within the range.

Fig. 8 shows the bode plot of (5) to represent the HTB system with the decoupling capacitor. Both selections of decoupling capacitor with the number of inverters from 2 to 5 are plotted. Fig. 9 shows the zoom-in magnitude of (5) at different frequencies. From Fig. 9, the damping effect of the 1-μF

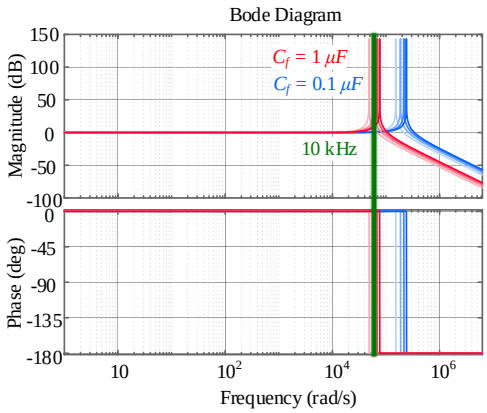

Fig. 8. Bode plot of the HTB system with decoupling capacitor.

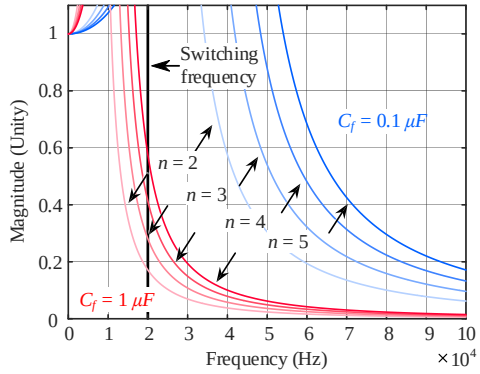

Fig. 9. Magnitude of PCC voltage with respect to frequency.

decoupling capacitor is better than the 0.1-μF decoupling capacitor, especially at the switching frequency of the system (from 20 kHz).

The experiment results of the 0.1-μF decoupling capacitor are shown in Figs. 10 and 11. Fig. 10 shows the PCC voltage, and Fig. 11 shows the PCC voltage fast Fourier transform (FFT) analysis. The high frequency component (20 kHz) is rich in the PCC voltage with the 0.1-μF decoupling capacitor.

The experiment results of the 1-μF decoupling capacitor are shown in Figs. 12 and 13. Fig. 12 shows the PCC voltage, and Fig. 13 shows the PCC voltage fast Fourier transform (FFT) analysis. The high frequency component is much reduced on the PCC voltage with the 1-μF decoupling capacitor.

VI. Conclusion

The grid emulator normally contains multiple inverters to mimic the behaviors of several grid elements. Each inverter contains a filtering inductor at the ac terminal to filter out the switching ripple current. However, the voltage on the PCC contains rich switching harmonics. This paper analytically determines the decoupling capacitor design for a given multi-inverter system. Both analytical calculation and the experiments show that the 0.1-μF decoupling capacitor cannot significantly remove the switching harmonics at PCC, whereas the 1-μF decoupling capacitor can effectively remove the switching harmonics at PCC.

References

[1] Y. Ma, J. Wang, F. Wang, and L. M. Tolbert, "Converter-based reconfigurable real-time electrical system emulation platform," *Chinese J. Electr. Eng.*, vol. 4, no. 1, pp. 20–27, 2018.

[2] P. Cai, X. Wu, Y. Yang, W. Yao, W. Liu, and F. Blaabjerg, "Design of digital filter-based highly robust active damping for LCL-filtered grid-tied inverters," *IEEE Southern Power Electronics Conference (SPEC)*, Singapore, Singapore, 2018, pp. 1-8.

[3] E. Twining and D. G. Holmes, "Grid current regulation of a three-phase voltage source inverter with an LCL input filter," *IEEE Trans. Power Electron.*, vol. 18, no. 3, pp. 888–895, 2003.

[4] J. Dannehl, F. W. Fuchs, and S. Hansen, "PWM rectifier with LCL-filter using different current control structures," *Eur. Conf. Power Electron. Appl. EPE*, pp. 1–10, 2007.

[5] F. Liu, Y. Zhou, S. Duan, J. Yin, B. Liu, and F. Liu, "Parameter design of a two-current-loop controller used in a grid-connected inverter system with LCL filter," *IEEE Trans. Ind. Electron.*, vol. 56, no. 11, pp. 4483–4491, 2009.

[6] X. Shi, Z. Wang, Y. Ma, L. Hang, L. M. Tolbert, and F. Wang, "Modeling and control of an LCL filter based three-phase active rectifier in grid emulator," in *Conference Proceedings - IEEE Applied Power Electronics Conference and Exposition - APEC*, 2013, pp. 992–998.

[7] M. Liserre, A. Dell'Aquila, and F. Blaabjerg, "Genetic algorithm based design of the active damping for a LCL-filter three-phase active rectifier," *Conf. Proc. - IEEE Appl. Power Electron. Conf. Expo. - APEC*, pp. 234–240, 2003.

[8] K. Koiwa, M. Rosyadi, A. Umemura, R. Takahashi, and J. Tamura, "Sensorless virtual resistance damping method for grid-connected three-phase PWM converter with LCL filter," *Int. Conf. Electr. Mach. Syst. ICEMS*, pp. 1746–1749, 2013.

[9] M. Wu and D. D. C. Lu, "Adding virtual resistance in source side converters for stabilization of cascaded connected two stage converter systems with constant power loads in DC microgrids," *Int. Power Electron. Conf. IPEC-Hiroshima - ECCE Asia*, pp. 3553–3556, 2014.

[10] L. Yang, X. Zhang, Y. Ma, J. Wang, L. Hang, K. Lin, L. M. Tolbert, F. Wang, and K. Tomsovic, "Hardware implementation and control design of generator emulator in multi-converter system," *Conf. Proc. - IEEE Appl. Power Electron. Conf. Expo. - APEC*, pp. 2316–2323, 2013.

[11] L. Yang, J. Wang, Y. Ma, J. Wang, X. Zhang, L. M. Tolbert, F. Wang, and K. Tomsovic, "Three-phase power converter-based real-time synchronous generator emulation," *IEEE Trans. Power Electron.*, vol. 32, no. 2, pp. 1651–1665, 2017.

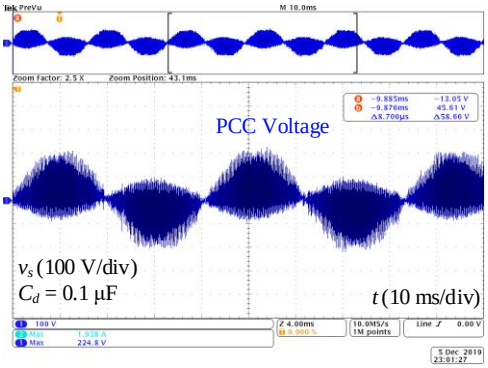

Fig. 10. PCC voltage with 0.1-μF decoupling capacitor.

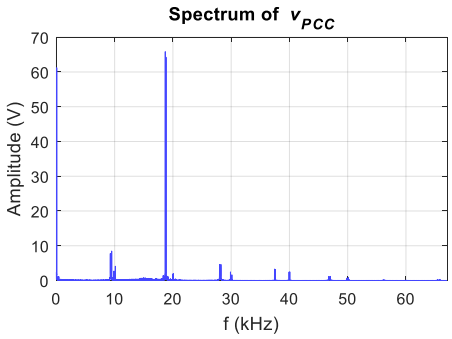

Fig. 11. PCC voltage spectrum with 0.1-μF decoupling capacitor.

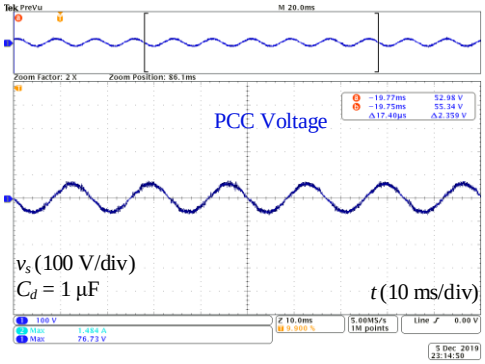

Fig. 12. PCC voltage with the 1-μF decoupling capacitor.

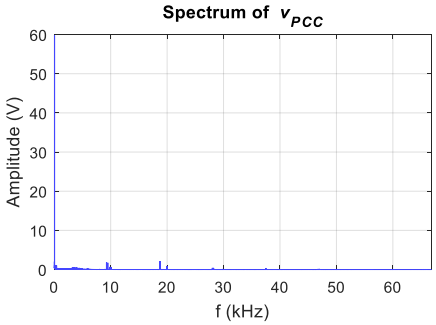

Fig. 13. PCC voltage spectrum with the 1-μF decoupling capacitor.

[12] Y. Ma, L. Yang, J. Wang, F. Wang, and L. M. Tolbert, “Emulating full-converter wind turbine by a single converter in a multiple converter based emulation system,” *Conf. Proc. - IEEE Appl. Power Electron. Conf. Expo. - APEC*, pp. 3042–3047, 2014.

[13] W. Cao, Y. Ma, J. Wang, L. Yang, J. Wang, F. Wang, and L. M. Tolbert, “Two-stage PV inverter system emulator in converter based power grid emulation system,” *IEEE Energy Convers. Congr. Expo.*, pp. 4518–4525, 2013.

[14] J. D. Boles, Y. Ma, J. Wang, D. Osipov, L. Tolbert, and F. Wang, “Converter-based Emulation of Battery Energy Storage Systems (BESS) for Grid Applications,” *IEEE Trans. Ind. Appl.*, vol. 55, no. 4, pp. 1–1, 2019.

[15] J. Wang, L. Yang, C. Blalock, and L. M. Tolbert, “Flywheel energy storage emulation using reconfigurable hardware test-bed of power converters,” *Elect. Energy Storage Applicat. and Technologies*, 2013.

[16] J. Wang, Y. Ma, L. Yang, L. M. Tolbert, and F. Wang, “Power Converter-based Three-phase Induction Motor Load Emulator,” in *IEEE Applied Power Electronics Conference and Exposition (APEC)*, 2013, pp. 3270–3274.

[17] J. Wang, L. Yang, Y. Ma, J. Wang, L. M. Tolbert, F. Wang, and K. Tomsovic, “Static and dynamic power system load emulation in a converter-based reconfigurable power grid emulator,” *IEEE Trans. Power Electron.*, vol. 31, no. 4, pp. 3239–3251, 2016.

[18] M. Kesler, E. Ozdemir, M. C. Kisacikoglu, and L. M. Tolbert, “Power converter-based three-phase nonlinear load emulator for a hardware testbed system,” *IEEE Trans. Power Electron.*, vol. 29, no. 11, pp. 5806–5812, 2014.

[19] S. Zhang, B. Liu, S. Zheng, Y. Ma, F. Wang, and L. M. Tolbert, “Development of a converter-based transmission line emulator with three-phase short-circuit fault emulation capability,” *IEEE Trans. Power Electron.*, vol. 33, no. 12, pp. 10215–10228, 2018.