Three-Phase DC Capacitor-Less Solid-State Variable Capacitor

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***Abstract*—Grid-connected full bridge inverters typically have a bulky electrolytic dc capacitor to absorb the unbalanced power from the ac side. The electrolytic capacitors are vulnerable and normally have shorter lifetime than other components in the converter. In most full-bridge inverter applications, the dc voltage is required to be relatively constant. However, in reactive power compensation applications, such as solid-state variable capacitor (SSVC), the constant dc-bus voltage is unnecessary since the dc bus is floating. This paper proposes a three-phase dc capacitor-less SSVC, which removes the electrolytic dc capacitor from the circuit by releasing the constraints on dc bus voltage fluctuation. The dc voltage is supported by ac side voltage directly. The remaining dc capacitance has a value of only 3% compared to that of the conventional three-phase SSVC. The proposed three-phase dc capacitor-less SSVC is validated by simulation.**

Keywords—SSVC, dc capacitor, reactive power, ripple voltage

I. INTRODUCTION

The conventional single-phase solid-state variable capacitor (SSVC) adopts H-bridge configuration to mimic the behavior of a capacitor. The H-bridge configuration suffers from the ripple power pulsating at twice the line frequency (2-ω). Conventionally, the ripple power is filtered by a bulky dc capacitor bank, resulting in low power density. Normally, to generate 1-p.u. reactive power, the H-bridge ends up with 10-p.u. dc capacitor [1]. Several power decoupling methods have been proposed to deal with this 2-ω ripple power in single-phase applications [2]–[11]. The fundamental idea of power decoupling methods is to transfer most of the ripple power from the dc capacitor to an extra energy storage component with relatively smaller size.

Unlike the single-phase inverter, the three-phase full bridge inverter does not need to have bulky dc capacitor because the 2-ω ripple power does not exist in a balanced three-phase system. However, sufficient dc capacitance is still necessary since the dc capacitor needs to absorb the ripple power introduced by an unbalanced load condition. The three-phase inverter dc capacitance is determined by the worst expected unbalanced condition.

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A constant dc voltage is not always necessary in applications such as SSVC because the dc capacitor is floating. Several control methods have been proposed to allow larger dc voltage ripple on the dc bus by increasing the dc voltage level [12]–[14], which allows a smaller dc-bus capacitance. The dc capacitance relies on the capability of the proposed control and the allowed dc voltage variation. Liu *et al*. [15] proposed a dc capacitor-less active capacitor that eliminate the dc capacitor from the single phase inverter by utilizing the grid voltage to support the dc bus voltage.

This paper proposes a three-phase dc capacitor-less SSVC that utilizes the grid voltage to support the dc bus voltage. Therefore, only an extremely small dc capacitor is needed on the dc bus. This paper is organized as follows. Section II explains the operating principle of the proposed three-phase dc capacitor-less SSVC. Section III provides the mathematical model of the proposed circuit. The control strategy of the proposed SSVC is presented in Section IV. The simulation results are provided in Section V for verification purposes.

II. OPERATING PRINCIPLE OF THREE-PHASE DC CAPACITOR-LESS SSVC

The basic idea is to rely on the grid side ac voltage to support the dc link voltage so that the dc link capacitor only processes the switching-frequency components. Since the dc capacitor does not need to filter the low frequency harmonics, the bulky electrolytic capacitor is no longer needed. Only a snubber capacitor remains in the hardware. Fig. 1 shows the three-phase dc capacitor-less SSVC circuits. The dc voltage is supported by

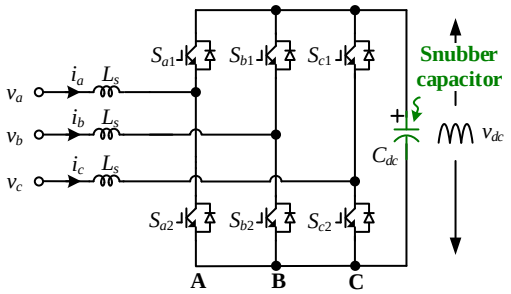


Fig. 1. Three-phase dc capacitor-less SSVC.

alternating through the three line voltages (whichever is the largest).

At steady state, the phase voltages are

$$v_a = \sqrt{2}V_s \sin(\omega t), \tag{1}$$

$$v_b = \sqrt{2}V_s \sin(\omega t - 2\pi/3), \tag{2}$$

$$v_c = \sqrt{2}V_s \sin(\omega t + 2\pi/3), \tag{3}$$

At steady state, the line currents are

$$i_a = \sqrt{2}I_s \cos(\omega t), \tag{4}$$

$$i_b = \sqrt{2}I_s \cos(\omega t - 2\pi/3), \tag{5}$$

$$i_c = \sqrt{2}I_s \cos(\omega t + 2\pi/3), \tag{6}$$

where V_s is the phase voltage RMS value, I_s is the line current RMS value, and ω is the line frequency. The resulting line voltages are

$$v_{ab} = v_a - v_b = \sqrt{6}V_s \sin(\omega t + \pi/6), \tag{7}$$

$$v_{bc} = v_b - v_c = \sqrt{6}V_s \sin(\omega t - \pi/2), \tag{8}$$

$$v_{ca} = v_c - v_a = \sqrt{6}V_s \sin(\omega t + 5\pi/6). \tag{9}$$

Since v_{ab}, v_{bc}, and v_{ca} are alternatingly supporting the dc-bus voltage, the dc voltage can be formulated as

$$v_{dc} = v_{ab}G_{ab} + v_{bc}G_{bc} + v_{ca}G_{ca}, \tag{10}$$

where G_{ij} is a gate function,

$$G_{ab} = \begin{cases} 1 & \pi/6 \le \omega t \le \pi/2 \\ 0 & else \\ -1 & 7\pi/6 \le \omega t \le 3\pi/2 \end{cases}, \tag{11}$$

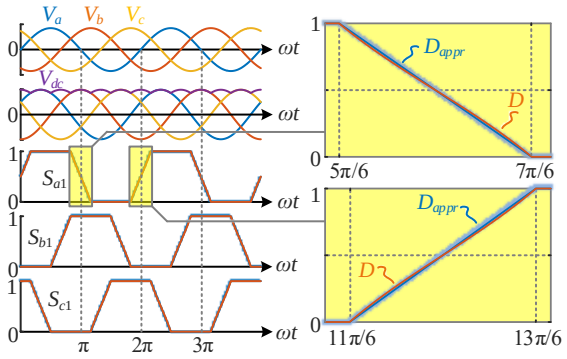


Fig. 2 Modulation strategy of three-phase dc capacitor-less SSVC.

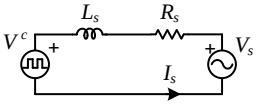


Fig. 3. Equivalent circuit of the three-phase SSVC in *d-q* frame.

$$G_{bc} = \begin{cases} 1 & 5\pi/6 \le \omega t \le 7\pi/6 \\ 0 & else \\ -1 & -\pi/6 \le \omega t \le \pi/6 \end{cases}, \tag{12}$$

$$G_{ca} = \begin{cases} 1 & -\pi/2 \le \omega t \le -\pi/6 \\ 0 & else \\ -1 & \pi/2 \le \omega t \le 5\pi/6 \end{cases}. \tag{13}$$

When $G_{ab} = 1$, v_{ab} is selected to support the dc voltage. The switches S_{a1} S_{b2} are on and S_{a2} S_{b1} are off. The remaining phase operates at a duty cycle D, where D satisfies

$$v_{cb} = D \cdot v_{dc}. \tag{14}$$

Since $v_{dc} = v_{ab} = \sqrt{6}V_s \sin(\omega t + \pi/6)$, combining (8) and (14) yields

$$D = \frac{v_{cb}}{v_{dc}} = \frac{\sqrt{6}V_s \sin(\omega t + \pi/2)}{\sqrt{6}V_s \sin(\omega t + \pi/6)} = \frac{1}{\tan \omega t \cos(\pi/6) + \sin(\pi/6)}. \tag{15}$$

The linearization of D has a good approximation within the region of $\omega t \in [\pi/6 \quad \pi/2]$, therefore

$$D \approx -\frac{3}{\pi}(\omega t - \pi/2). \tag{16}$$

$-3/\pi$ is the slope of the D reference, the constant term $-1/2\pi$ corrects the time offset. The comparison of (15) and (16) is illustrated in Fig. 2. The minor mismatch can be compensated by closed-loop control which will be presented in later sections. Similar to $G_{ab} = 1$, when $G_{ab} = -1$, v_{ba} is selected to support the dc voltage. The switches S_{a2} S_{b1} are on and S_{a1} S_{b2} are off. The remaining phase operates at the duty cycle D, where D satisfies

$$D \approx \frac{3}{\pi}\left(\omega t - \frac{7}{6}\pi\right). \tag{17}$$

where $\frac{7}{6}\pi$ is a constant that corrects the time offset. The derivation of duty cycle in other regions of time is similar and therefore omitted in this paper. The complete modulation of the three-phase dc capacitor-less SSVC is shown in Fig. 2. The lower switches S_{a2}, S_{b2}, and S_{c2} are complimentary to S_{a1}, S_{b1}, and S_{c1}, respectively.

III. Modeling of DC Capacitor-Less SSVC

A. External Dynamic Model

The external dynamic model of the proposed three-phase dc capacitor-less SSVC is similar to a three-phase inverter. Fig. 3 shows the equivalent circuit of the three-phase SSVC system in *d-q* frame. V_s is the source voltage; V^c is the output voltage of SSVC converter at the bridge circuit terminal. I_s is the ac current, L_s is the filtering inductance, and R_s is the equivalent circuit resistance. The *abc* frame to *dq* frame transformation is formulated as follows,

$$V_s = \begin{bmatrix} v_d \\ v_q \\ v_0 \end{bmatrix}$$

$$= \frac{2}{3}\begin{bmatrix} sin(\theta) & sin\left(\theta - \frac{2\pi}{3}\right) & sin\left(\theta + \frac{2\pi}{3}\right) \\ cos(\theta) & cos\left(\theta - \frac{2\pi}{3}\right) & cos\left(\theta + \frac{2\pi}{3}\right) \\ \frac{1}{2} & \frac{1}{2} & \frac{1}{2} \end{bmatrix}\begin{bmatrix} v_a \\ v_b \\ v_c \end{bmatrix}, \quad (18)$$

$$V^c = \begin{bmatrix} v_d^c \\ v_q^c \\ v_0^c \end{bmatrix}$$

$$= \frac{2}{3}\begin{bmatrix} sin(\theta) & sin\left(\theta - \frac{2\pi}{3}\right) & sin\left(\theta + \frac{2\pi}{3}\right) \\ cos(\theta) & cos\left(\theta - \frac{2\pi}{3}\right) & cos\left(\theta + \frac{2\pi}{3}\right) \\ \frac{1}{2} & \frac{1}{2} & \frac{1}{2} \end{bmatrix}\begin{bmatrix} v_a^c \\ v_b^c \\ v_c^c \end{bmatrix}, \quad (19)$$

where v_*^c is the converter mid-point output voltage.

$$I_s = \begin{bmatrix} i_d \\ i_q \\ i_0 \end{bmatrix}$$

$$= \frac{2}{3}\begin{bmatrix} sin(\theta) & sin\left(\theta - \frac{2\pi}{3}\right) & sin\left(\theta + \frac{2\pi}{3}\right) \\ cos(\theta) & cos\left(\theta - \frac{2\pi}{3}\right) & cos\left(\theta + \frac{2\pi}{3}\right) \\ \frac{1}{2} & \frac{1}{2} & \frac{1}{2} \end{bmatrix}\begin{bmatrix} i_a \\ i_b \\ i_c \end{bmatrix}. \quad (20)$$

In three phase three wire system, the sum of all phases currents is zero,

$$i_a + i_b + i_c = 0\ . \quad (21)$$

Therefore,

$$i_0 = 0\ . \quad (22)$$

The active power absorbed by the inverter is

$$p = \frac{3}{2}v_d i_d + \frac{3}{2}v_q i_q\ . \quad (23)$$

The reactive power absorbed by the inverter is

$$q = \frac{3}{2}v_d i_q - \frac{3}{2}v_q i_d\ . \quad (24)$$

From the equivalent circuit, the dynamic behavior of the converter can be formulated as

$$L_s\frac{dI_s}{dt} + R_s I_s = V_s - V^c\ . \quad (25)$$

Since both the magnitude and the phase of I_s are functions of time, (25) can be re-written as,

$$L_s\frac{dI_s}{dt} + \omega L_s \times I_s + R_s I_s = V_s - V^c\ , \quad (26)$$

or

$$L_s\frac{d}{dt}\begin{bmatrix} i_d \\ i_q \end{bmatrix} + \omega L_s\begin{bmatrix} -i_q \\ i_d \end{bmatrix} + R_s\begin{bmatrix} i_d \\ i_q \end{bmatrix} = \begin{bmatrix} V_d - V_d^c \\ V_q - V_q^c \end{bmatrix}. \quad (27)$$

Fig. 4 shows the block diagram of the SSVC external dynamics derived from (26) and (27). Fig. 4 shows that the active current i_d and reactive current i_q are coupled with each other through the ac filtering inductance L_s.

B. Internal Dynamic Model

The SSVC contains a dc capacitor. The dynamics of the dc capacitor are analyzed in this section. In instantaneous power theory [16], the instantaneous reactive power q does not affect the dc link capacitor voltage. Only the instantaneous active power p is accumulated in dc link capacitor. Therefore,

$$p_{dc} = \frac{3}{2}v_d i_d + \frac{3}{2}v_q i_q = C_{dc}v_{dc}\frac{dv_{dc}}{dt}\ , \quad (28)$$

where p_{dc} is the instantaneous active power seen by the dc link. The dc capacitor voltage dynamic (28) will be used to compensate the dc voltage in later sections.

IV. Control Strategy

The SSVC's inherent purpose is to generate reactive power. Therefore, p and q should be controlled accordingly. From (23) and (24), the instantaneous power can be simplified as follows if i_d is controlled to 0.

$$p = \frac{3}{2}v_q i_q\ , \quad (29)$$

$$q = \frac{3}{2}v_d i_q\ . \quad (30)$$

This is normally the case for SSVC since the SSVC provides reactive power only. In order to generate the required reactive power, the active current and reactive current controller are established in this paper. The complete current control is shown in Fig. 5. The cross-coupling terms with ωL_s are small and therefore neglected.

i_d and i_q are the active current and reactive current, respectively. The coupling effect of active and reactive current can be neglected in practice since the term $\omega i_{d/q} L_s$ is relatively small.

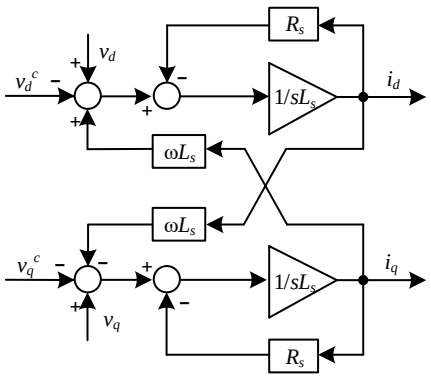


Fig. 4. Block diagram of the SSVC external dynamics.

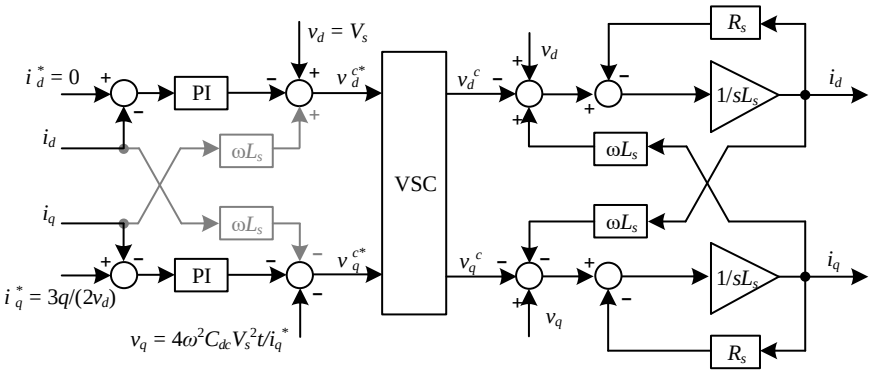


Fig. 5. Three-phase SSVC current controller.

The dc capacitor needs to be compensated with proper instantaneous active power in order to follow the fluctuating dc voltage. From (29) and (30):

$$\frac{3}{2} v_q i_q = C_{dc} v_{dc} \frac{dv_{dc}}{dt} . \quad (31)$$

Take $v_{dc} = v_{cb}$ (from $-\pi/6$ to $\pi/6$) for example.

$$C_{dc} v_{dc} \frac{dv_{dc}}{dt} = C_{dc}\sqrt{6}V_s \sin(\omega t - \pi/2) \frac{d\sqrt{6}V_s \sin(\omega t - \pi/2)}{dt} \quad (32)$$

$$C_{dc} v_{dc} \frac{dv_{dc}}{dt} = 6C_{dc} V_s^2 \sin(\omega t - \pi/2) \frac{d \sin(\omega t - \pi/2)}{dt} \quad (33)$$

$$C_{dc} v_{dc} \frac{dv_{dc}}{dt} = 6\omega C_{dc} V_s^2 \sin(\omega t - \pi/2) \cos(\omega t - \pi/2) \quad (34)$$

$$C_{dc} v_{dc} \frac{dv_{dc}}{dt} = -6\omega C_{dc} V_s^2 \cos \omega t \sin \omega t \quad (35)$$

When $-\pi/6 < \omega t < \pi/6$, $\cos\omega t \approx 1$ and $\sin\omega t \approx \omega t$. Therefore, (35) can be re-written as

$$C_{dc} v_{dc} \frac{dv_{dc}}{dt} = -6\omega^2 C_{dc} V_s^2 t . \quad (36)$$

Insert (36) into (31),

$$\frac{3}{2} v_q i_q = -6\omega^2 C_{dc} V_s^2 t , \quad (37)$$

$$v_q = -4\omega^2 C_{dc} V_s^2 t / i_q . \quad (38)$$

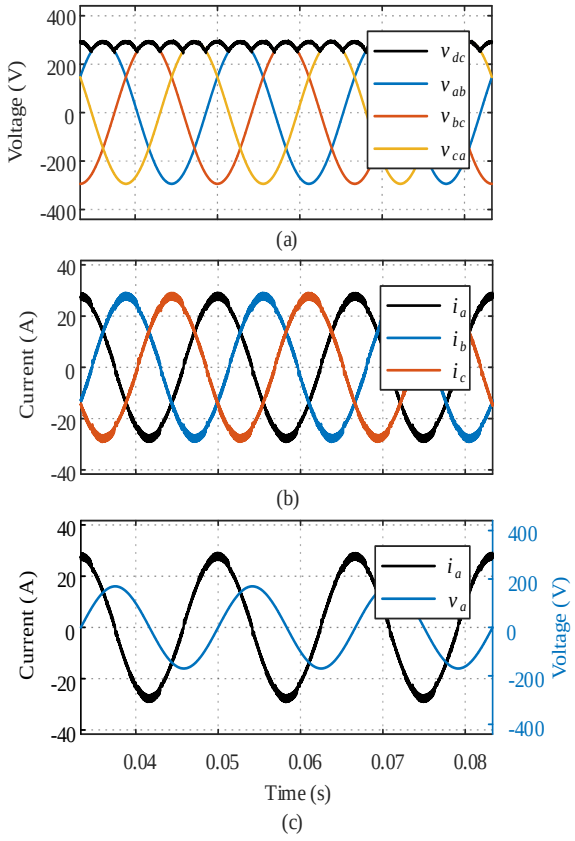
In order to compensate the dc voltage to follow the desired waveform, a feedforward v_q^c component needs to be added to the final v_q^{c*} reference. The complete control diagram of three-phase dc capacitor-less SSVC is shown in Fig. 5.

V. Simulation

To verify the proposed three-phase dc capacitor-less SSVC, the simulation is conducted in Matlab. The key parameters of the simulation study are summarized in Table I. The schematic of the simulation circuit is shown in Fig. 1.

TABLE I. KEY PARAMETERS OF SIMULATION

dc capacitance, C_{dc}	6 μF
Filtering inductance, L_s	0.1 mH
Phase voltage, V_s	120 V
Switching frequency, f_{sw}	10 kHz
Power rating, Q	10 kvar
Line frequency, f_0	60 Hz



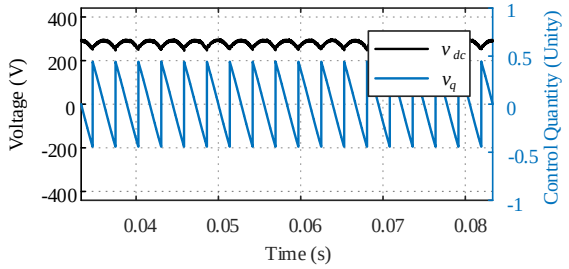


Fig. 7. v_q compensation for maintaining the dc link voltage fluctuation.

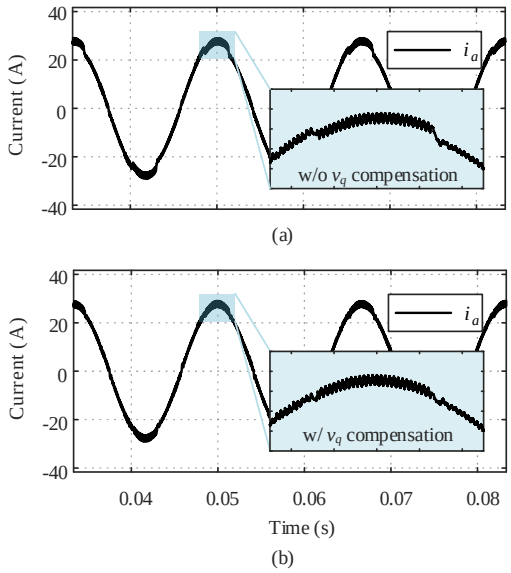


Fig. 8. Phase *a* current (a) without v_q compensation; (b) with v_q compensation.

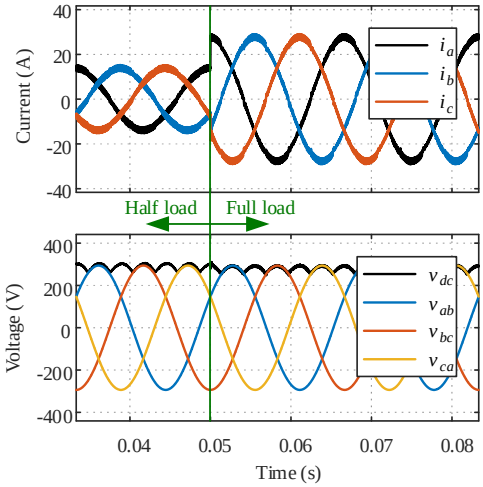


Fig. 9. Converter dynamics with step change of reactive power generation.

The waveforms of the three-phase dc capacitor-less SSVC at steady state are shown in Fig. 6. Fig. 6(a) shows the line voltages and the dc link voltage. From Fig. 6(a), the dc link voltage is clamped by the maximum line voltage. Fig. 6(b) shows the line current. Fig. 6(c) shows the phase angle between the line current and phase voltage. The converter is generating reactive power. Fig. 7. Shows the v_q compensation for maintaining the dc link voltage fluctuation. This compensation follows (38). Fig. 8 shows the current waveforms with and without the v_q compensation. Fig. 9 shows the converter dynamics with a step change of reactive power generation.

VI. Conclusion

Full bridge inverters typically have bulky electrolytic dc capacitor to absorb the unbalanced power from the ac side. The electrolytic capacitors are vulnerable and normally have shorter lifetime than other components in the converter. In most full-bridge inverter applications, the dc voltage is required to be relatively constant. However, in reactive power compensation applications, the constant dc-bus voltage is unnecessary since the dc bus is floating.

This paper proposes a three-phase dc capacitor-less SSVC, which removes the electrolytic dc capacitor from the circuit by releasing the constraints on dc bus voltage fluctuation. The dc voltage is supported by ac side voltage directly. The remaining dc capacitance required is only 3% compared to that of the conventional three-phase SSVC. The proposed three-phase dc capacitor-less SSVC is validated by simulation.

References

[1] Y. Liu, X. Wang, and F. Z. Peng, "An H-bridge-based single-phase VAr generator with minimum dc capacitance," *IEEE J. Emerg. Sel. Top. Power Electron.*, vol. 6, no. 4, pp. 2001-2014, Dec. 2018.

[2] Y. Ohnuma and J. I. Itoh, "A novel single-phase buck PFC ac-dc converter with power decoupling capability using an active buffer," *IEEE Trans. Ind. Appl.*, vol. 50, no. 3, pp. 1905-1914, 2014.

[3] Y. Lei, C. Barth, S. Qin, W-C Liu, I. Moon, A. Stillwell, D. Chou, T. Foulkes, Z. Ye, Z. Liao, and R. C. N. Pilawa-Podgurski, "A 2-kW single-phase seven-level flying capacitor multilevel inverter with an active energy buffer," *IEEE Trans. Power Electron.*, vol. 32, no. 11, pp. 8570-8581, 2017.

[4] K. Mozaffari, M. Amirabadi, and Y. Deshpande, "A single-phase inverter/rectifier topology with suppressed double-frequency ripple," *IEEE Trans. Power Electron.*, vol. 33, no. 11, pp. 9282-9295, 2018.

[5] S. Qin, Y. Lei, C. Barth, W. C. Liu, and R. C. N. Pilawa-Podgurski, "A high power density series-stacked energy buffer for power pulsation decoupling in single-phase converters," *IEEE Trans. Power Electron.*, vol. 32, no. 6, pp. 4905-4924, 2017.

[6] W. Qi, H. Wang, X. Tan, G. Wang, and K. D. T. Ngo, "A novel active power decoupling single-phase PWM rectifier topology," in *Conference Proceedings - IEEE Applied Power Electronics Conference and Exposition - APEC*, Fort Worth, TX, 2014, pp. 89-95.

[7] R. Wang, F. Wang, D. Boroyevich, R. Burgos, R. Lai, P. Ning, and K. Rajashekara, "A high power density single-phase PWM rectifier with active ripple energy storage," *IEEE Trans. Power Electron.*, vol. 26, no. 5, pp. 1430-1443, 2011.

[8] R. Chen, Y. Liu, and F. Z. Peng, "DC capacitor-less inverter for single-phase power conversion with minimum voltage and current stress," *IEEE Trans. Power Electron.*, vol. 30, no. 10, pp. 5499-5507, 2015.

[9] H. Li, K. Zhang, H. Zhao, S. Fan, and J. Xiong, "Active power decoupling for high-power single-phase PWM rectifiers," *IEEE Trans. Power Electron.*, vol. 28, no. 3, pp. 1308-1319, 2013.

[10] Y. Sun, Y. Liu, M. Su, X. Li, and J. Yang, "Active power decoupling method for single-phase current-source rectifier with no additional active switches," *IEEE Trans. Power Electron.*, vol. 31, no. 8, pp. 5644-5654, 2016.

[11] R. Chen, Y. Liu, and F. Z. Peng, "A solid state variable capacitor with minimum capacitor," *IEEE Trans. Power Electron.*, vol. 32, no. 7, pp. 5035–5044, 2017.

[12] L. Gu, K. Yao, X. Ruan, and M. Xu, "Means of eliminating electrolytic capacitor in ac/dc power supplies for LED lightings," *IEEE Trans. Power Electron.*, vol. 24, no. 5, pp. 1399-1408, 2009.

[13] F. Gao, D. Li, P. C. Loh, Y. Tang, and P. Wang, "Indirect dc-link voltage control of two-stage single-phase PV inverter," in *IEEE Energy Conversion Congress and Exposition, ECCE*, San Jose, CA, 2009, pp. 1166-1172.

[14] B. Wang, X. Ruan, K. Yao, and M. Xu, "A method of reducing the peak-to-average ratio of LED current for electrolytic capacitor-less ac-dc drivers," *IEEE Trans. Power Electron.*, vol. 25, no. 3, pp. 592-601, 2010.

[15] Y. Liu and F. Z. Peng, "Real dc capacitor-less active capacitors," *Conf. Proc. - IEEE Appl. Power Electron. Conf. Expo. - APEC*, pp. 44–51, 2017.

[16] H. Akagi, Y. Kanazawa, and A. Nabae, "Instantaneous reactive power compensators comprising switching devices without energy storage components," *IEEE Trans. Ind. Appl.*, vol. IA-20, no. 3, pp. 625-630, 1984.