Quasi-Static Time Series Fatigue Simulation for PV Inverter Semiconductors with Long-Term Solar Profile

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***Abstract* —Power system simulations with long-term data tend to have large time steps varying from one second to a few minutes. However, for PV inverter semiconductors, the minimum thermal stresses cycle is with line frequency. This requires the time step of the fatigue simulation to be much smaller than the line period. This small time step results in poor simulation speed, especially for long-term simulations. This paper proposes a fast fatigue simulation for inverter semiconductors using the quasi-static time series (QSTS) simulation concept. The fatigue analysis typically focuses on the peak and valley values of a strain and neglect the transients from peaks to valleys. The proposed simulation utilizes this property of fatigue analysis and calculates the steady state of the semiconductor junction temperature only. The resulting time step of the fatigue simulation is 15 minutes, which is consistent with the solar dataset without losing accuracy.**

***Index Terms*—Fatigue analysis, fast simulation, inverter aging, solar photovoltaic energy.**

I. Introduction

Solar photovoltaic (PV) integration requires power electronic inverters to interface with the electric grid. Many literatures have reported that the power electronic devices have shorter lifetime compared to its connected PV panel [1], [2]. For example in a PV system, the lifetime of PV panels is normally warrantied at 20–25 years, whereas the PV inverter lifetime is usually limited to less than 15 years [1]. Semiconductors are among the most vulnerable components that lead to inverter failure [3], and they are sensitive to temperature. High operating temperature and rapid, large thermal cycling are the two main reasons that lead to more rapid semiconductor aging [4], [5].

To extend the lifetime of PV inverters, many methods have been tested on a simulation-based aging analysis to evaluate the performance of the proposed methods. Reigosa *at al*. [6] presented a lifetime model to predict the fatigue level of the semiconductor bond wires. Similar lifetime models are also used in [5], [7], [8]. This lifetime model of semiconductors has the potential to extend to grid-level simulations and incorporate into reliability studies. The power systems level simulations typically adopt quasi-static time series (QSTS) approach to evaluate a system with the data ranging from several days to several years [9]. The QSTS approach can effectively reduce the computational burden for a long-term simulation while keeping an acceptable accuracy.

This paper proposed a fast semiconductor fatigue simulation approach that can be extended to grid-level long-term simulations. The proposed approach incorporates the PV inverter profiles as the input and estimates the fatigue level of the inverter semiconductors as the output. The proposed approach uses the Fast Fourier Transform (FFT) and the frequency domain response of the semiconductor electrothermal model to accelerate the junction temperature calculation.

This paper is organized as follows. Section II presents a frequency-domain fast electrothermal simulation method to translate the power loss into semiconductor junction temperature. Section III discusses the fatigue analysis of semiconductors using the rainflow counting method. Section IV provides a case study to show the results of the proposed semiconductor fatigue analysis simulation. Finally, Section V concludes this paper.

II. Fast Electrothermal Simulation

This section discusses the electrothermal simulation using an FFT approach to find the junction temperature.

A. Semiconductor Power Loss Formulation

The power losses of an inverter are considered as the heat source for device junction temperature rise. And large junction temperature variation and high average value are considered as the key factors which leads to accelerated device aging. The power losses of semiconductors consist of two parts: 1) switching loss and 2) conduction loss. The semiconductor switching loss and conduction loss for the PV inverter's semiconductors of this paper follow [10]. An IGBT-based PV inverter is selected as the model for the fatigue analysis in this

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TABLE I. IGBT KEY PARAMETERS

Part No.	Manufacturer	$V_{0,IGBT}$	R_{IGBT}	T_j	V_{GE}	V_{CE}	I_C	E_{on}	E_{off}
IKW60N60H3	Infineon	1.06 V	0.024 Ω	175 °C	0/15 V	400 V	60 A	2.63 mJ	1.46 mJ

TABLE II. DIODE KEY PARAMETERS

Part No.	Manufacturer	$V_{0,D}$	R_D	T_j	Q_{rr}	V_{ref}	I_{ref}
IKW60N60H3	Infineon	0.76 V	0.025 Ω	175 °C	2.8 μC	400 V	60 A

TABLE III. DIODE AND IGBT (IKW60N60H3) FOSTER MODEL

	Thermal Resistance (K/W)					Thermal Capacitance (sec.)				
	R_1	R_2	R_3	R_4	R_5	τ_1	τ_2	τ_3	τ_4	τ_5
Diode	0.049	0.23	0.31	0.27	0.20	7.50×10^{-6}	2.20×10^{-4}	2.3×10^{-3}	1.55×10^{-2}	0.108
IGBT	0.0034	0.072	0.082	0.196	0.0093	3×10^{-5}	2.7×10^{-4}	3×10^{-3}	1.56×10^{-2}	0.2275

paper. The key parameters of the IGBT/diode pair are summarized in Tables I and II.

B. Electrothermal Model

The thermal model of a diode can be represented by a branch of an *RC* network (Foster model) [11]. The Foster model uses linear components (*RC*) to capture the linear properties of the thermal behavior and eliminate the nonlinearities. The accuracy of a Foster model is acceptable for steady state analysis, and so the electrothermal model for the semiconductors in this paper adopts the Foster model. The power losses will be passed through the device Foster model and result in the device junction temperature. The Foster models of the diodes and IGBTs of this paper are summarized in Table III.

The electrothermal model of this paper adopts a typical discrete IGBT module with an on-chip anti-parallel diode. The power losses generated in the IGBT/diode junctions will flow to the case of the IGBT module through several layers of materials, such as solder, metal, ceramic, etc., and finally results in a case temperature, T_c. The case of an IGBT module normally will be attached to a heat sink by the thermal paste. The resulting heat sink temperature is T_h. The heat sink dissipates the heat to the ambient by convection.

The detailed electrothermal model of the IGBT modules with anti-parallel diode packs is shown in Fig. 1. The switching loss (P_{sw}) and conduction loss (P_{con}) are the heat source for each IGBT and diode. The thermal impedance of thermal paste is typically small, and hence neglected in this paper. The Foster model for the heatsink used in this paper is summarized in Table IV.

C. Fast Junction Temperature Calculation

Theoretically, common simulation algorithms such as Euler-Maruyama method can be adopted to find the junction temperature. The power loss of semiconductors typically cycles

TABLE IV. HEATSINK THERMAL PARAMETERS

Heatsink Part Number	C247-025
Manufacturer	Ohmite
Surface Area	7312 mm^2
Thermal Resistance	3~9 °C/W (5 °C/W for this paper)
Thermal Capacitance	1000 sec.

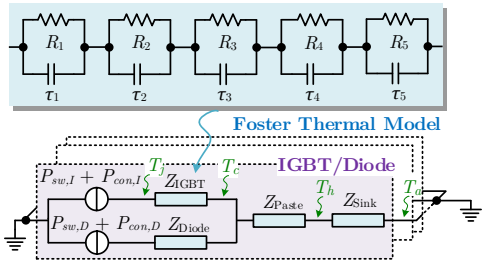

Fig. 1. Detailed thermal model of PV inverter using discrete IGBT-diode pack.

in a period of 60 Hz, and the Euler-Maruyama method requires the time step to be much smaller than 1/60 s (typically around 100 μs) in order to achieve an acceptable accuracy [12]. Such small time-steps are computationally burdensome for long-term simulations.

Quasi-static simulations are widely adopted in long-term power system simulations and achieve acceptable accuracies [9]. The basic idea of the quasi-static simulation is to calculate the steady states of the system and use the steady states to represent the system during the whole period of a time step. The time step of a quasi-static simulation varies from a second to several minutes depending on the simulation data type and accuracy requirements. This paper leverages quasi-static time series simulation to simulate the fatigue of inverter semiconductors over longer periods of time. The proposed simulation has a good potential to co-simulate with any simulation which also adopts the quasi-static concept.

The quasi-static simulation only computes the steady state of the system; all transients will be neglected. The fatigue simulation using rainflow counting algorithms only counts the peak and valley of a strain cycle. The path to reach a peak from a valley, or vice versa, is noncritical. Hence, any intermediate transients between the peak and valley are not of interest in a fatigue simulation. Quasi-static concept, which neglects transients, are suitable for fatigue simulations. To find the steady state of semiconductor thermal stress, the heat source (device power loss) can be decomposed into several sinusoids by FFT. The steady state response of the electrothermal model for each sinusoid can be calculated using phasors. Then, the inverse Fourier transform will be applied to the phasor forms of the junction temperature to find the time-domain waveforms. Thus, the peak and valley from the inverse FFT can be recorded

and sent to the rainflow-counting algorithms. Fig. 2 shows the FFTs of a sample IGBT power loss waveform.

From Fig. 2, the magnitudes of the harmonics over 240 Hz are relatively small, and therefore, can be neglected. The inverse Fourier transform from the selected harmonics is shown in Fig. 3. Fig. 3 also shows the original waveforms of time-domain IGBT power loss. The recovered time-domain waveform with the dc to fourth-order harmonics has already achieved an acceptable accuracy. Hence, this paper selects the spectrum from dc to 4th harmonics as the heat source for the junction temperature.

The selected harmonics from the power loss FFT are then applied to the electrothermal model of the semiconductors to calculate the corresponding steady-state junction temperature in frequency-domain. The junction temperature phasors are then inversed back to time domain to find the peaks and valleys. The recovered time-domain junction temperature with the ambient temperature at 25 °C is shown in Fig. 4.

III. Fatigue Analysis

The fatigue analysis of PV inverter semiconductors contains two parts. The first part is to evaluate the operating conditions, such as junction temperature profile, of semiconductors by using rainflow counting algorithm. The second part is to map the operating conditions to the accumulated fatigue model.

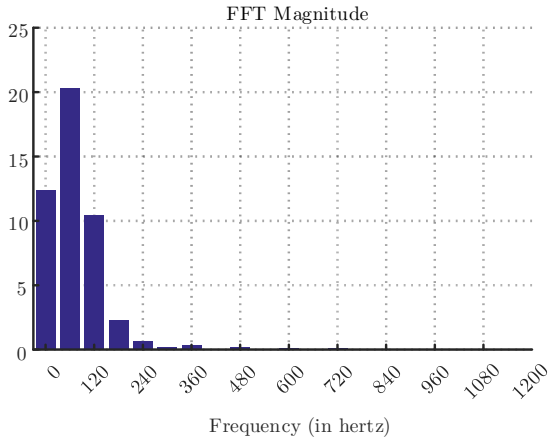

Fig. 2. Typical IGBT power loss FFT.

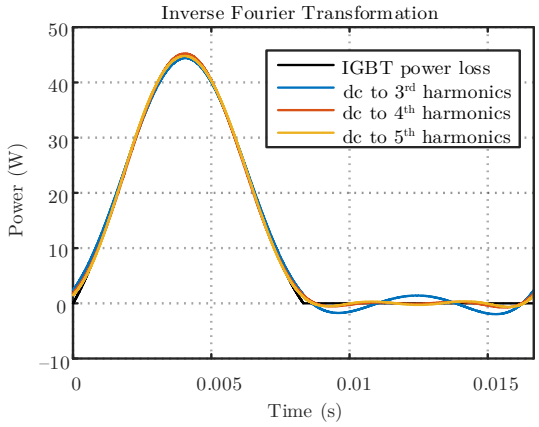

Fig. 3. Inverse Fourier transform of IGBT power loss.

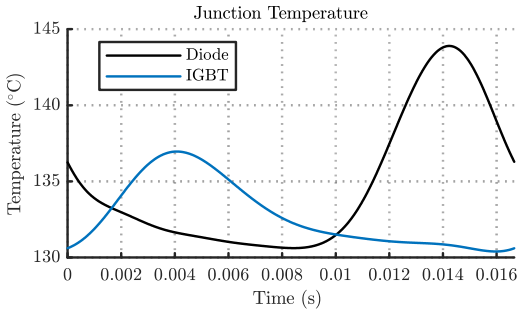

Fig. 4. Recovered time-domain semiconductor junction temperature for one electric cycle (60 Hz).

A. Rainflow Counting

Rainflow counting is a standard algorithm to evaluate the fatigue data of a system [13]. The basic idea of rainflow-counting algorithms is to count the strain cycle over a certain period of time. Each strain cycle is described with three key parameters: the peak value, valley value, and the stress duration. For the rainflow-counting algorithm of the inverter semiconductors, the strain is the junction temperature of each device. The peak and valley refer to the local maximum and minimum value of junction temperature profile. The stress duration is the time duration that starts with the valley of the cycle and ends with the peak of the cycle. The rainflow-counting algorithm of this paper follows the standard algorithm described in [11]. The peak and valley are recorded from the junction temperature profile. Then, each strain cycle and its associated parameters will be mapped into the lifetime model of semiconductors.

B. Accumulated Fatigue Model

The rainflow-counting data can be mapped to a fatigue level by using the semiconductor lifetime model. The lifetime model of semiconductors is an empirical equation to associate some aging factors to a lifetime expectation. For instance, the semiconductor lifetime model of this paper follows [14],

$$N_f = A \times (\Delta T_j)^{\alpha} \times (ar)^{\beta_1 \Delta T_j + \beta_0} \times \left[\frac{C+(t_{on})^{\gamma}}{C+1}\right] \times exp\left(\frac{E_1}{k_b \times \bar{T}_j}\right) \times f_d \quad (1)$$

where N_f is the number of cycles to failure. This parameter indicates that a new semiconductor device is going to fail after N_f cycles of use for a given operating condition. $\bar{T}_j$ is the mean junction temperature of a semiconductor. ΔT_j is the junction temperature variation in a strain cycle. t_{on} is time of the strain from the valley to the peak. The other parameters are related to the semiconductor material physics and are given in Table V [14]. The lifetime model is tested in a way that a periodic thermal stress is applied to a semiconductor until it fails. The thermal stress is applied during 0 to t_{on} of each period, and then the thermal stress is released during t_{on} to the end of this period. The applied thermal stress has a variation of ΔT_j and a mean temperature of $\bar{T}_j$. The semiconductor is expected to fail after N_f cycles under this test condition.

There are various cumulative damage models in the literature for reliability engineering assessment. The accumulated damage model of this paper follows Miner's rule, which is a linear cumulative damage model [15]. The assumption of Miner's rule is that the damage of the IGBT modules is independent of the stresses experienced during its life cycle, which means each cycle from the rainflow counting will create a damage independently. The sum of the damage from all rainflow cycles will be the accumulated damage of the device. The accumulated fatigue can be expressed as follows,

$$AF = \sum_i \frac{n_{f,i}}{N_{f,i}} \tag{2}$$

where $N_{f,i}$ is the number of cycles to failure given the condition i, and $n_{f,i}$ is the number of cycles that the device is exposed under the condition i. $n_{f,i}$ is obtained from the rainflow-counting algorithm.

TABLE V.
PARAMETERS OF THE LIFETIME MODEL OF AN IGBT MODULE [16]

Parameter	Value	Experimental condition
A	3.4368×10^{14}	
α	-4.923	$5\ \mathrm{K} \le \Delta T_{junc} \le 80\ \mathrm{K}$
β_1	9.012×10^{-3}	
β_0	1.942	$0.19 \le ar \le 0.42$
C	1.434	
γ	-1.208	$0.07\ \mathrm{s} \le t_{on} \le 63\ \mathrm{s}$
f_d	0.6204	
E_a	0.06606 eV	$32.5^\circ\mathrm{C} \le T_{junc} \le 122^\circ\mathrm{C}$
k_B	8.6173324×10^{-5} eV/K	

IV. CASE STUDY

The proposed fatigue simulation is created in MATLAB. The fatigue simulation can be explained with the aid of Fig. 5. A seven-day PV inverter generation dataset is provided to the fatigue simulation. The power loss of each semiconductor then is calculated for the given PV generation profile. The power loss will be dissipated through the electrothermal *RC* network and result in a semiconductor junction temperature. Then, the semiconductor thermal profile is fed into the rainflow-counting algorithm to determine the device stress profile. The stress profile from the rainflow counting will be mapped to the accumulated fatigue result.

Fig. 6 shows the seven-day solar data used in this case study. The data are from a sampled MPPT profile of a PV inverter in

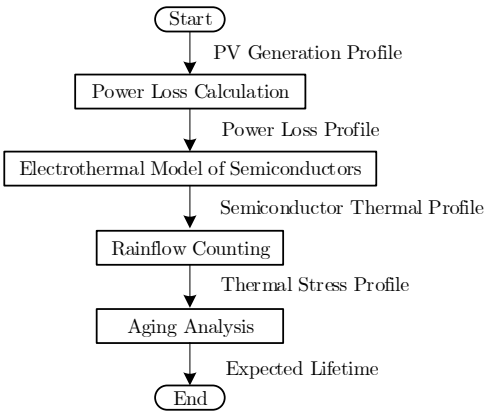

Fig. 5. Flowchart of the proposed fatigue simulation.

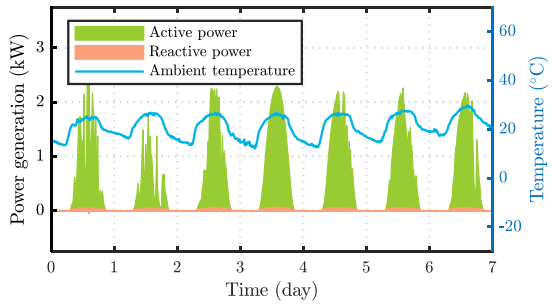

Fig. 6. Seven-day PV inverter generation profile for the case study.

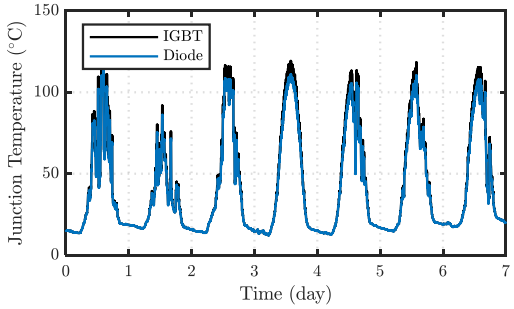

Fig. 7. Semiconductor junction temperature profile.

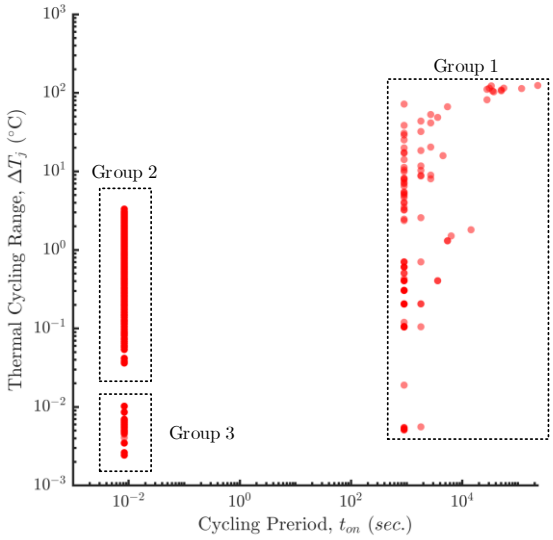

Fig. 8. Rainflow-counting results of the diode junction temperature profile.

Chattanooga, Tennessee from Aug. 1st, 2014 to Aug. 7th, 2014. The time step of the data is 15 minutes. The resulting inverter semiconductor junction temperature is shown in Fig. 7. The lowest junction temperature is the same as the ambient temperature. The highest junction temperature is around 120 °C.

The rainflow-counting results are shown in Fig. 8. The rainflow-counting result shows that the thermal cycles can be manually categorized into three groups. Group 1 refers to the cycles with low frequency. Group 1 cycles are caused by solar irradiance variation, which typically varies from a few seconds to a few hours. The main causes of the solar irradiance change are solar angle change, cloud cover, and temporary bird shading. The diurnal temperature variation also contributes to

the low-frequency cycles in Group 1. Group 2 refers to the cycles with a 60-Hz frequency during the time the PV inverter generates active power (daylight). Group 3 refers to the cycles with a 60-Hz frequency while the PV inverter is idling (night). The number of cycles for each group is shown in Fig. 9. Group 1 data are large in ΔT_j (greater than 5 °C) but the number of cycles is small (maximum one cycle for each stress condition). Group 2 data are relatively small in ΔT_j (between 0.02 to 5 °C) and the number of cycles is relatively large (in the order of 10^5). Group 3 data are extremely small in ΔT_j (less than 0.02) but the number of cycles is the largest (in the order of 10^6).

The accumulated fatigue results from the simulation is summarized in Table VI. The accumulated fatigue from the Group 1 stress consumes 0.323% of the semiconductor lifetime during the seven-day simulation. The accumulated fatigues from the Groups 2 and 3 are relatively small compared with Group 1. The accumulated fatigue result shows that the low frequency thermal cycling is the leading factor of the PV inverter semiconductor aging. The semiconductor is expected to have a lifetime of 3.4 years given the simulated condition.

TABLE VI. ACCUMULATED FATIGUE RESULTS FROM THE SIMULATION

Fatigue Type	t_{on} (s)	Accumulated Fatigue
Low Frequency Cycling	> 1/120	0.323%
60-Hz Cycling	1/120	9.01×10^{-6}%
Inverter Idling	1/120	6.46×10^{-19}%

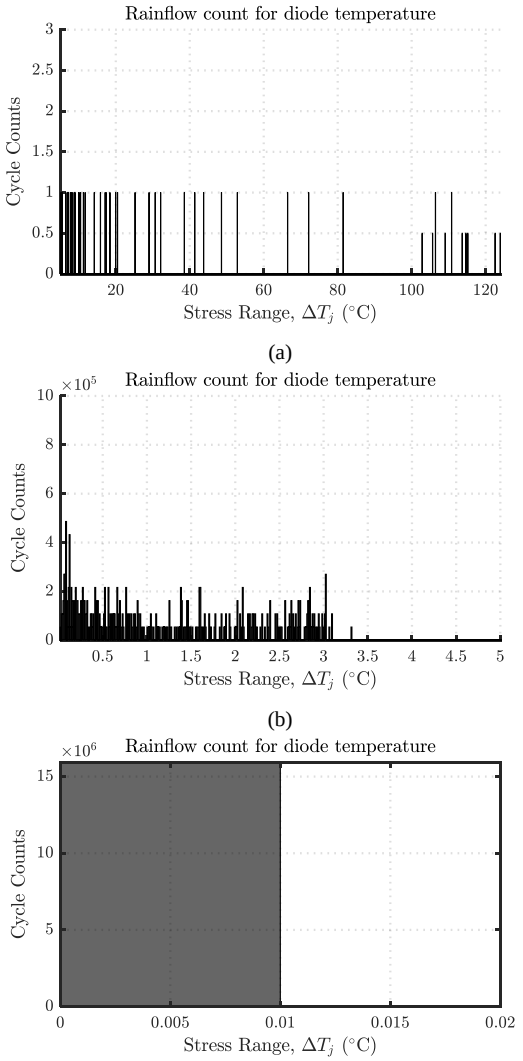

Fig. 9. Number of cycles for each group of thermal stresses. (a) Group 1; (b) Group 2; and (c) Group 3.

V. CONCLUSION

This paper presents a fast fatigue simulation for PV inverter semiconductors. The proposed simulation increases the time step from 100 μs (as used in conventional Euler-Maruyama method) to 15 minutes, the same as the solar profile data time step. The proposed fatigue simulation is suitable for long-term evaluation and co-simulation with other quasi-static simulation platforms for power systems. This paper presents the seven-day simulation results from the proposed fatigue simulation. The simulation results show that the fatigue stress of PV inverter semiconductors can be categorized into three groups. And the simulation result shows that the low-frequency thermal cycling is the key factor that leads to the semiconductor aging.

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