Aging Effect Analysis of PV Inverter Semiconductors for Ancillary Services Support

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Abstract: PV inverters can provide reactive power while generating active power. An ongoing microgrid implementation at Duke Energy actively engages non-utility PVs to generate/absorb reactive power in support of ancillary services to increase microgrid resiliency during extreme events. PV systems are requested to provide reactive power support: 1) in response to grid voltage variation to better regulate the local voltage; or 2) in response to utility incentives, such as following Transactive Energy System (TES) incentives. However, providing ancillary services might shorten the lifetime expectation of PV inverter semiconductors. This paper summarizes the potential impacts on a PV inverter semiconductor's lifetime when providing ancillary services. The analysis presented in this research work shows that providing reactive power support will increase the mean junction temperature and the junction temperature variation of the inverter diodes. This increased junction temperature will eventually lead to shorter diode lifetime. The lifetime estimation of semiconductors is briefly reviewed. The power losses of PV inverter semiconductors are derived as a support analysis to the junction temperature calculation. In addition, the impact of filtering inductor on the semiconductor current distribution is discussed. The theoretical analysis presented in this research work is supported by simulation results.

***Index Terms*— Aging, dc-ac power converters, photovoltaic systems, reactive power, thermal analysis**

I. Introduction

Solar photovoltaic (PV) integration requires power electronic inverters to interface with the power grid. Many literature have reported that the inverter's power electronic devices and passives (capacitors) have shorter lifetime compared to its associated PV panels [1], [2]. For example in a PV system, the lifetime of the PV panels is normally warrantied at 20–25 years, whereas the PV inverter lifetime is usually less than 15 years [1]. Due to the short lifetime of inverters, more than one half of the maintenance cost of PV system is consumed by inverters [3]. In addition, the utility power industry usually expects a long lifetime of the inverters so that the inverters could retire from the power grid at the same time as the whole PV system [4].

An industry-wide survey presented in [4] indicates that semiconductors and capacitors are the most vulnerable components that lead to inverter failure. The power losses of semiconductors and capacitors are dissipated as heat, and this heat dissipation increases the mean junction temperature and the temperature variation of semiconductors and capacitors. Literature have shown that the thermal stress (both mean junction temperature and junction temperature variation) may drastically reduce the lifetime of electrolytic capacitors [5] and semiconductors [6]-[8].

In addition to active power generation, PV inverters are requested to provide reactive power support in IEEE Standard 1547, as revised in 2018 [9]. Distributed systems and microgrids that adopt transactive energy systems (TES) also request PV inverters to provide ancillary services. The TES is a concept to engage more distributed energy

This work was primarily supported by U.S. Department of Energy Grid Modernization Lab Consortium. This work also made use of Engineering Research Center shared facilities supported by the Engineering Research Center Program of the National Science Foundation and the Department of Energy under NSF Award Number [EEC-1041877] and the CURENT Industry Partnership Program.

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resources (DERs), especially non-utility owned DERs, to participate in the operation of the power grid [10]–[13]. Alam *et al*. [10], [11] proposed a transactive approach to engage DERs to provide ancillary services.

TES can incentivize customers to provide ancillary services from the customer-owned DERs to improve the reliability and quality of the grid's power. The TES controller could publish low reactive power demand level when the utility reactive power generation is sufficient, which would discourage customers from generating reactive power [10], [11], [14]–[16]. The customer DERs could also publish low reactive power generation capability if the reactive power generation would decrease the profit of the customers [17]–[24] because it might require decreasing their real (active) power output.

Some literature have indicated that the engagement of DERs to provide ancillary services may have a negative effect on the lifetime of DER inverters due to increasing thermal stress [25], [26]. However, none of the literature theoretically quantify the increased thermal stress caused by reactive power generation. The reactive power may change the current distribution among inverter semiconductors. In addition, different current distribution may change the power loss distribution among the individual semiconductors. The impact of reactive power on other major components, such as dc capacitors and filtering inductors, is not as significant as that on semiconductors. Therefore, this paper selects inverter semiconductors as the objective of the ancillary services aging effect analysis.

Many power electronic literature have proposed solutions to extend the lifetime of inverters. Andresen *et al*. [27] proposed a maximum-power-point-tracking (MPPT) control for PV systems which limits the maximum junction temperature of the power semiconductors. Yang *et al*. [28], [29] also proposed a MPPT methodology to limit the maximum operating point which will limit the temperature indirectly. Also, PV inverter manufacturers design their products by derating the output power as ambient temperature increases [30]–[32]. However, none of the existing literature systematically study the mechanism of reactive power impact on PV inverter semiconductor aging.

This paper aims to fill these gaps in the literature by systematically analyzing the thermal stress of PV inverter semiconductors when the inverters provide reactive power during support of ancillary services that require the production/absorption of reactive power. A brief review on the lifetime estimation of PV inverter semiconductors is presented followed by the electrothermal model of the semiconductors. The analysis of the thermal model reveals that the reactive power generation will increase both the mean junction temperature and the junction temperature variation of the inverter diodes. This increased junction temperature will lead to shorter inverter lifetime. The power losses of PV inverter semiconductors derived in this paper provide a support analysis for the calculation of junction temperature. The theoretical analysis is supported by simulation results.

This paper is organized as follows. Section II provides the electrothermal model for typical PV inverter topologies. Section III formulates the power loss of semiconductors. Section IV analyzes the reactive power impact on the PV inverter power loss. Section V provides simulation results as evidence to support theoretical analysis in previous sections. Portions of this paper were presented at the 2020 IEEE PES General Meeting; Sections III, IV, V are new materials that were not included in the conference paper [33].

II. Electrothermal Model of PV Inverter

A. Background of Semiconductor Lifetime Expectation

The lifetime model of semiconductors can be formulated as follows [34],

$$N_f = A \times \left(\Delta T_j\right)^{\alpha} \times (ar)^{\beta_1 \Delta T_j + \beta_0} \times \left[\frac{C+(t_{on})^{\gamma}}{C+1}\right] \times exp\left(\frac{E_a}{k_b \times \bar{T}_j}\right) \times f_d \quad (1)$$

where N_f is the number of cycles to failure. This parameter indicates that a new semiconductor device is going to fail after N_f cycles of use for a given operating condition. $\bar{T}_j$ is the mean junction temperature of a semiconductor. ΔT_j is the junction temperature variation in time period of t_{on}. t_{on} is the thermal cycle period, which is typically the same as the electrical line period. The other parameters are given in Table I [34].

TABLE I.
PARAMETERS OF THE LIFETIME MODEL OF AN IGBT MODULE [34]

Parameter	Value	Experimental condition
A	3.4368×10^{14}	
α	– 4.923	5 K ≤ ΔT_{junc} ≤ 80 K
β_1	9.012×10^{-3}	
β_0	1.942	0.19 ≤ ar ≤ 0.42
C	1.434	
γ	– 1.208	0.07 s ≤ t_{on} ≤ 63 s
f_d	0.6204	
E_a	0.06606 eV	32.5 °C≤ T_{junc} ≤ 122 °C
k_B	8.6173324×10^{-5} eV/K	

From (1), the semiconductor lifetime is related to the mean junction temperature $\bar{T}_j$ and the junction temperature variation ΔT_j. When $\bar{T}_j$ and/or ΔT_j increase, the number of cycles to failure N_f will decrease.

B. Foster Thermal Model

The insulated-gate bipolar transistor (IGBT) type and metal-oxide-semiconductor field-effect transistor (MOSFET) type PV inverter have similar electrothermal models. This paper focuses on IGBT-type PV inverters since IGBT based PV inverters are more common especially for high power ratings (>5 kW) [35]. The electrothermal model of a typical discrete IGBT with anti-parallel diode with thermal management is shown in Fig. 1 [36]. IGBT and diode chips are the heat source in the inverter system. The heat generated in the IGBT's junction will flow to the case of the IGBT module through several layers of materials, such as solder, metal, ceramic, etc., and finally results in a case

temperature, T_c. The case of an IGBT normally will be attached to a heat sink by thermal paste. The resulting heat sink temperature is T_h. The heat sink dissipates the heat to the ambient by convection. Other types of thermal management systems include fans, cold plate, and water cooling.

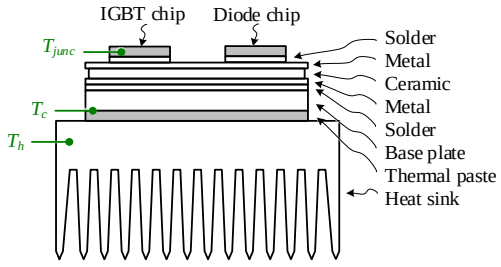


Fig. 1. Typical IGBT module with thermal management.

The Foster thermal model presented in [26] is used in this research work to estimate the thermal stress of a PV inverter. The Foster thermal model describes the temperature transient of an object by a branch of RC network. The detailed thermal model of a PV inverter composed of IGBTs with anti-parallel diode pack is shown in Fig. 2. The switching loss (P_{sw}) and conduction loss (P_{con}) are the heat source for each IGBT and diode. In a two-stage PV inverter, it normally contains 5 (single-phase) to 7 (three-phase) IGBTs depending on the topology.

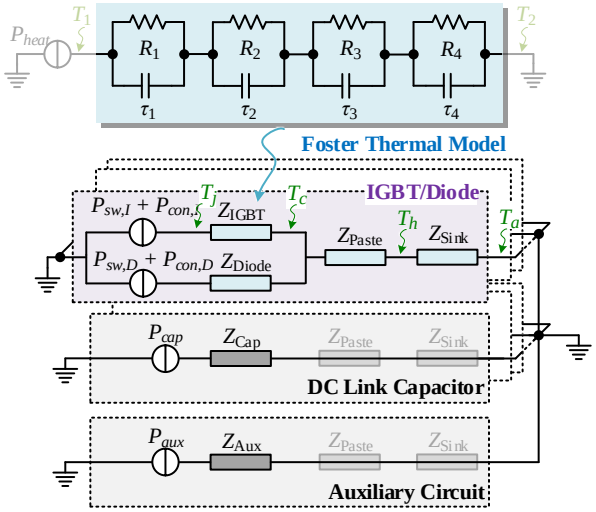


Fig. 2. Detailed thermal model of PV inverter using discrete IGBT-diode pack.

Each IGBT module is attached to a heat sink by thermal paste. The capacitor power loss (due to current flowing through its own parasitic resistance) is the heat source for each capacitor. Each PV inverter normally contains several capacitors on the dc link, and their thermal resistances are thermally in parallel. The capacitors and other auxiliary circuits such as printed circuit boards (PCBs), filtering inductors, and EMI filters may not have active thermal management or dedicated heat sinks depending on inverter design. The common IGBT-diode packages and their thermal models are summarized in Table II.

Several possible thermal models shown in Fig. 3 can be used to calculate junction temperature. For example, the junction temperature of the IGBT and diode of Fig. 3(a) can be formulated as (2) and (3),

$$T_{j,I} = \left(P_{sw,I} + P_{con,I}\right)\left(Z_{IGBT} + Z_{Paste} + Z_{Sink}\right) + T_{amb} \quad (2)$$

$$T_{j,D} = \left(P_{sw,D} + P_{con,D}\right)\left(Z_{Diode} + Z_{Paste} + Z_{Sink}\right) + T_{amb} \quad (3)$$

where subscript D indicates the variable associated with the diode, and subscript I indicates the variable associated with the IGBT. Z_{Paste} is the thermal paste thermal impedance. Z_{Sink} is the heatsink thermal impedance. T_{amb} is the ambient temperature. Other types of thermal models shown in Fig. 3 can also be formulated similar to (2) and (3). The derivation is omitted in this paper.

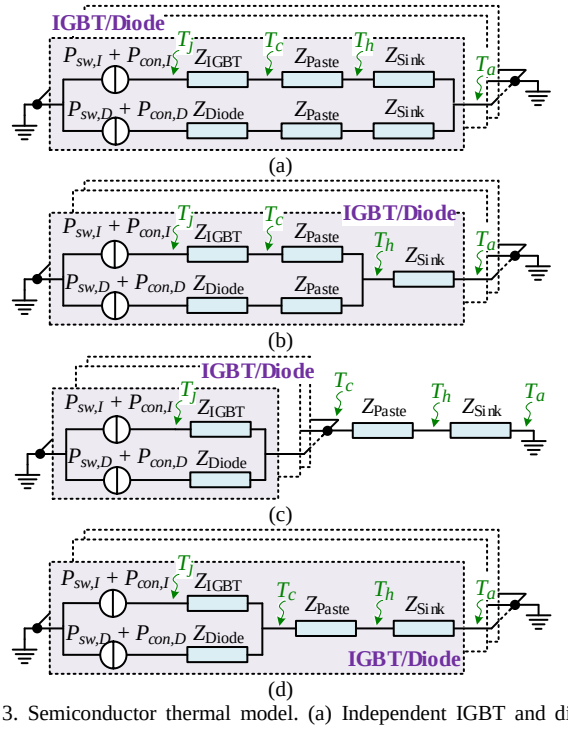


Fig. 3. Semiconductor thermal model. (a) Independent IGBT and diode package. Each IGBT/diode is attached to independent heatsink. (b) Independent IGBT and diode package. The IGBT and diode are sharing a heatsink. (c) Half/full bridge module that contains more than two IGBT-diode pairs in one package. The bridge module is attached to a heatsink. (d) IGBT packed with anti-parallel diode in single package. Each IGBT-diode module is attached to independent heatsink.

TABLE II. COMMON IGBT-DIODE PACKAGES AND THERMAL MODEL

Type	IGBT	Diode	Heatsink	Thermal Model
1	Discrete	Discrete	Independent heatsink for each IGBT and diode	Fig. 3(a)
2	Discrete	Discrete	Shared by IGBT and diode	Fig. 3(b)
3	Bridge Module	Built-in IGBT module	Shared by multiple bridge modules	Fig. 3(c)
4	Discrete	Built-in IGBT module	Independent heatsink for each IGBT-diode pair	Fig. 2, Fig. 3(d)

Each thermal impedance Z can be represented by

$$Z = \sum_n^l R_n \left(1 - e^{-\frac{t}{\tau_n}}\right) \quad (4)$$

where l is the number of terms in the Foster thermal model. R is the thermal resistance, and τ is the thermal time constant.

The Foster thermal model generally neglects the nonlinearities by modeling the thermal properties with a RC network. The superposition theorem can be applied to the semiconductor Foster model to calculate the semiconductor junction temperature. The mean junction temperature $\bar{T}_j$ is determined by the average power loss ($\bar{P}_{con}$ and $\bar{P}_{sw}$) of the semiconductors. And the thermal cycle ΔT_{junc} is determined by the power loss variation (ΔP_{con} and ΔP_{sw}) of the semiconductors which is due to the switching of the IGBTs and the variation of the ac current provided by the inverter.

III. Semiconductor Power Loss Formulation

The power losses of semiconductors consist of two parts: 1) switching loss and 2) conduction loss. A typical two-stage single-phase PV inverter topology is shown in Fig. 4. The following power loss evaluation is based on the PV inverter topology shown in Fig. 4. The semiconductors on the dc-dc side will not be analyzed in this paper because dc-dc stage operation is only affected by active power generation. The reactive power generation would slightly increase the current stress of dc-dc stage semiconductors due to the increasing power loss of the reactive power generation. Therefore, the semiconductors of the dc-dc stage will not be discussed in this paper.

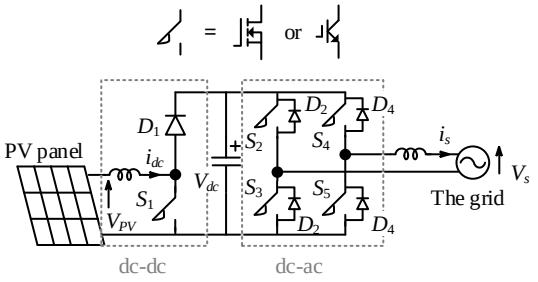


Fig. 4. Typical PV inverter topology.

A. Switching Loss

For a given IGBT, the switching loss is determined by the turn-on and turn-off energy, and the turn-on loss could be formulated as follows [37],

$$E_{on,I} = V_{dc} i_s \cdot \frac{1}{2} t_{on} \quad (5)$$

where t_{on} is the total time of current rising and voltage falling when power switches turn on. t_{on} is a fixed value once a specific switching device and its associated gate drive are selected. V_{dc} is the dc-link voltage; i_s is the load current. The switching loss during the IGBT's turn-on state is shown in Fig. 5(a) [37].

The average value of $E_{on,I}$ for the dc-ac side IGBT (S_2 - S_5) during the sinusoidal period of the inverter output current can also be calculated as [38],

$$E_{on,I} = \frac{\sqrt{2}}{2\pi} V_{dc} I_s \cdot t_{on} \quad (6)$$

where I_s is the rms value of the inverter output current. Similarly, IGBT (S_2 - S_5) turn-off loss can be calculated as [38],

$$E_{off,I} = \frac{\sqrt{2}}{2\pi} V_{dc} I_s \cdot t_{off} \quad (7)$$

The total IGBT (S_2 - S_5) switching loss is calculated as,

$$P_{sw,I} = (E_{on,I} + E_{off,I}) \cdot f_{sw} \quad (8)$$

where f_{sw} is the switching frequency.

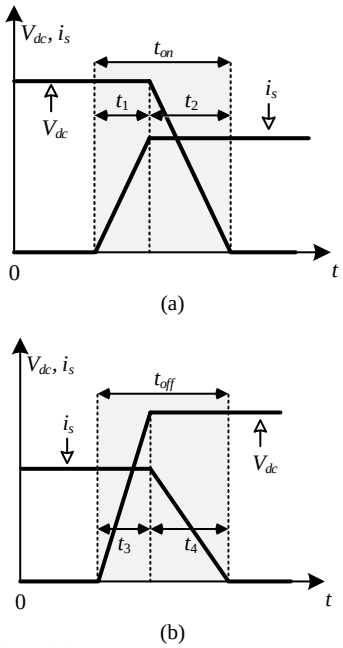


Fig. 5. Switching loss during IGBT's (a) turn-on time; and (b) turn-off time.

For a given MOSFET, the switching loss is similar to that for an IGBT and also follows (5)-(8).

Diode switching loss is generated by the reverse recovery during the turn-off transition. Normally, diode datasheets provide the value of reverse recovery energy loss $E_{rr,D}$ under the manufacturer's specified test conditions. The actual diode switching loss needs to be rescaled by the actual current and blocking voltage. The diode (D_2 - D_5) switching loss during the sinusoidal period of the inverter output current is calculated as [38],

$$P_{sw,D} = \left(\frac{\sqrt{2}}{\pi} \frac{I_s V_{dc}}{I_{ref} V_{ref}} E_{rr,D}\right) \cdot f_{sw} \quad (9)$$

where I_{ref} and V_{ref} are the testing current and voltage condition provided from the datasheet.

B. Conduction Loss

The conduction loss of an IGBT can be modeled by two components connected in series, a resistor and a dc voltage source as shown in Fig. 6(a). The dc voltage source represents the built-in voltage of the device p-n junction. The power losses in both the resistor and dc voltage source contribute to the IGBT conduction losses [38].

$$P_{con,IGBT} = I_{rms,IGBT}^2 R_{IGBT} + I_{avg,IGBT} V_{0,IGBT} \quad (10)$$

where $I_{rms,IGBT}$ and $I_{avg,IGBT}$ are the rms value and average

value of the current flowing through the IGBT collector to emitter. The details for determining $I_{rms,IGBT}$ and $I_{avg,IGBT}$ are summarized in the Appendix. $V_{0,IGBT}$ and R_{IGBT} are typically given by IGBT datasheets.

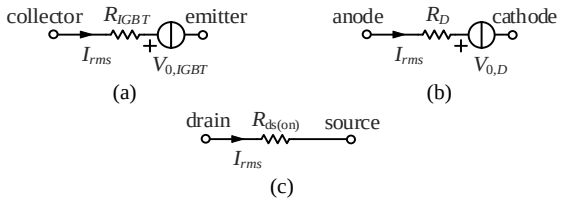


Fig. 6. Semiconductor conduction loss model. (a) IGBT; and (b) diode; (c) MOSFET.

The conduction loss of a diode is similar to an IGBT and can be modeled as shown in Fig. 6(b). The power losses in both the resistor and dc voltage source contribute to the diode conduction losses.

$$P_{con,D} = I_{rms,D}^2 R_D + I_{avg,D} V_{0,D} \tag{11}$$

where $I_{rms,D}$ and $I_{avg,D}$ are the rms value and the average value of the current flowing through the diode anode to cathode. The details of $I_{rms,D}$ and $I_{avg,D}$ are summarized in the Appendix. $V_{0,D}$ and R_D are typically given by diode datasheets.

For the MOSFET, the conduction loss could be formulated as follows [38],

$$P_{con,M} = I_{rms,M}^2 R_{ds(on)} \tag{12}$$

where $R_{ds(on)}$ is the drain-source on-resistance of a MOSFET as shown in Fig. 6(c). $I_{rms,MOSFET}$ is the MOSFET current rms value. The details of the $I_{rms,MOSFET}$ for a MOSFET-based dc-ac inverter is included in the Appendix.

The complete semiconductor switching loss and conduction loss for a PV inverter's possible devices are summarized in Table III.

IV. Reactive Power Impact on Power Loss

To evaluate the reactive power impact on the semiconductor power loss, the IGBT-diode type of PV inverter is selected in the following analysis. Assume that the output voltage and current follow,

$$v_s = \sqrt{2} V_s \sin(\omega t + \varphi) \tag{13}$$

$$i_s = \sqrt{2} I_s \sin \omega t \tag{14}$$

Assuming a fixed apparent output power $S = V_s I_s$ for the PV inverter, then the modulation function follows

$$m = \frac{M \sin(\omega t + \varphi) + 1}{2} \tag{15}$$

The modulation index M is typically 0.8~1 for PV inverters. The current conducted by S_2 IGBT can be formulated as

$$i_{S2} = \begin{cases} \sqrt{2} I_s \sin \omega t \cdot \frac{M \sin(\omega t + \varphi) + 1}{2} & i_s \geq 0 \\ 0 & i_s < 0 \end{cases} \tag{16}$$

The current conducted by D_2 diode can be formulated as

$$i_{D2} = \begin{cases} -\sqrt{2} I_s \sin \omega t \cdot \frac{M \sin(\omega t + \varphi) + 1}{2} & i_s < 0 \\ 0 & i_s \geq 0 \end{cases} \tag{17}$$

A. Average Power Loss

The power loss distribution among inverter semiconductors varies with respect to different output power factor (*pf*). In general, the reactive power will reduce the conduction loss of IGBTs and increase the conduction loss of diodes. Thus, the reactive power negatively impacts the diode thermal stress. The equivalent current that flows through the diode increases as the *pf* decreases. Fig. 7 shows the rms current $I_{rms,D}$ from (A.6), average current $I_{avg,D}$ from (A.7) and maximum current $I_{max,D}$ from (17) of the diode.

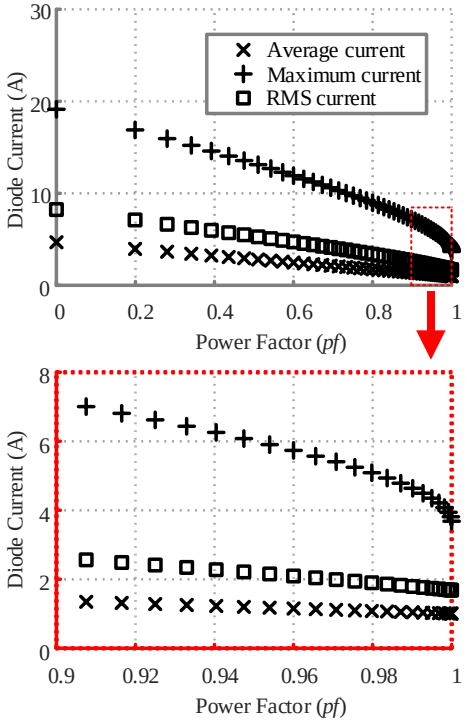


Fig. 7. Equivalent current rms, average, and maximum value that flows through diodes as power factor changes.

TABLE III. Semiconductor Power Loss

	Switching Loss	Conduction Loss
IGBT	$P_{sw,I} = (E_{on,I} + E_{off,I}) \cdot f_{sw}$	$P_{con,IGBT} = I_{rms,IGBT}^2 R_{IGBT} + I_{avg,IGBT} V_{0,IGBT}$
MOSFET	$P_{sw,M} = (E_{on,M} + E_{off,M}) \cdot f_{sw}$	$P_{con,M} = I_{rms,M}^2 R_{ds(on)}$
Diode	$P_{sw,D} = (\frac{\sqrt{2}}{\pi} \frac{I_s V_{dc}}{I_{ref} V_{ref}} E_{rr,D}) \cdot f_{sw}$	$P_{con,D} = I_{rms,D}^2 R_D + I_{avg,D} V_{0,D}$

More current flowing through diodes will increase the conduction loss of the diode. From (11), (A.6) and (A.7), the conduction loss of diode can be formulated as

$$P_{con,D} = \left(\frac{I_S^2}{4}R_D + \frac{I_S}{\sqrt{2}\pi}V_{0,D}\right) - \left(\frac{I_S^2}{4}\cdot\frac{8M}{3\pi}R_D + \frac{I_S}{\sqrt{2}\pi}\cdot\frac{\pi M}{4}V_{0,D}\right)pf \quad (18)$$

where *pf* is the power factor of the PV inverter output power. The diode conduction loss increases as the *pf* decreases.

As the power factor decreases, more current flows through diodes, and less current flows through the IGBTs (for a fixed apparent power). From (10), (A.4) and (A.5), the conduction loss of an IGBT can be formulated as

$$P_{con,IGBT} = \left(\frac{I_S^2}{4}R_{IGBT} + \frac{I_S}{\sqrt{2}\pi}V_{0,IGBT}\right) + \left(\frac{I_S^2}{4}\cdot\frac{8M}{3\pi}R_{IGBT} + \frac{I_S}{\sqrt{2}\pi}\cdot\frac{\pi M}{4}V_{0,IGBT}\right)pf \quad (19)$$

The IGBT conduction loss decreases as the *pf* decreases.

B. *Power Loss Cycling*

Since the ac current and voltage cycle periodically (60 Hz in this paper), the semiconductor losses are also typically cycling in this fundamental cycle. In addition to the average conduction loss, the power loss variation during a fundamental cycle also varies with power factor. The average losses determine the mean junction temperature (T_j). The power loss variation in a fundamental cycle determines the junction temperature variation (ΔT_j).

Eq. (17) formulates the D_2 diode current. Fig. 8 shows the D_2 diode current for one half of one fundamental cycle (from π to 2π). The D_2 diode current has less variation at unity *pf*. Compared to the current at unity power factor, the current variation during one of the two half cycles doubles when the *pf* decreases to 0.9. Other diodes in the inverter will also have similar current variation as D_2 diode.

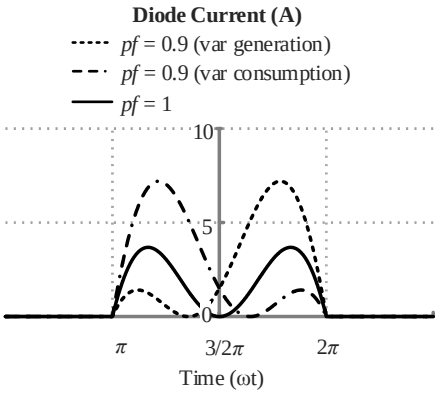


Fig. 8. Full-bridge single phase inverter diode current variation in a fundamental cycle.

C. *Effect of Filtering Inductor*

The inverter's filtering inductor is normally deemed an integral part of a PV inverter. However, from a semiconductor point of view, the filtering inductor is part of the load. Assume that the PV inverter midpoint voltage vector is $\mathbf{V}_c$. The PV inverter's midpoint voltage contains a wide spectrum of harmonics, especially the switching frequency harmonics. $\mathbf{V}_c$ denotes the fundamental component of the midpoint voltage. The voltage drop on the filtering inductor is $\mathbf{V}_L$. The grid voltage vector is $\mathbf{V}_s$. The voltages should follow

$$\mathbf{V}_c = \mathbf{V}_s + \mathbf{V}_L \quad (20)$$

The polarities of $\mathbf{V}_c$, $\mathbf{V}_s$, and $\mathbf{V}_L$ are shown in Fig. 9(a). The phase angle between $\mathbf{V}_s$ and $\mathbf{I}_s$ is θ_s. The phase angle between $\mathbf{V}_c$ and $\mathbf{I}_s$ is θ_c. The *pf* of fundamental output current is defined as $\cos\theta_s$. The *pf* of bridge circuit current is defined as $\cos\theta_c$. $\cos\theta_c$ is the actual power factor that determines the current distribution among the semiconductors.

If the output power is at unity *pf* as shown in Fig. 9(b), the bridge circuit *pf* will be lagging because of the filter inductor and has a value of $\cos\theta_c$. The inverter needs to generate a reactive power to compensate the reactive power consumed by the filtering inductor. If the output power is slightly capacitive with a *pf* of $\cos\theta_s$ as shown in Fig. 9(c), the small reactive power consumed by the filtering inductor may result in the bridge circuit *pf* being unity.

If the output power is inductive as shown in Fig. 9(d), the filtering inductor will further reduce the bridge circuit *pf*. The filtering inductors of PV inverters are typically 0.01 to 0.05 p.u. The filtering inductors do not significantly affect the bridge circuit *pf* in typical cases. However, some PV inverters may have relatively large filtering inductor/transformers that are up to 0.15 p.u. In this case, the filtering inductors will significantly affect the bridge circuit *pf* and hence the amount of current through the individual semiconductors in these cases.

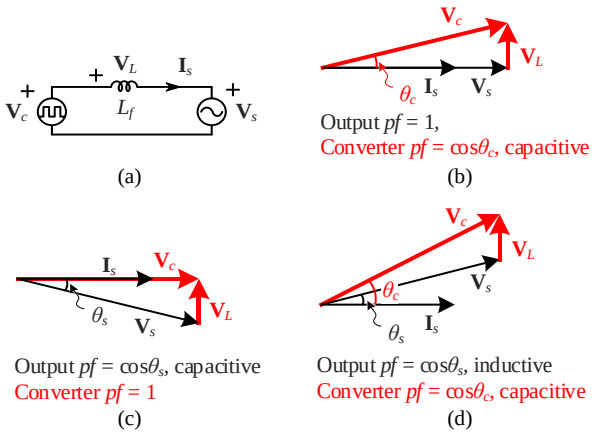


Fig. 9. (a) Equivalent circuit of PV inverter connected to the grid. Phasor diagram of PV inverter with (b)unity power factor; (c) capacitive output; and (d) inductor output.

D. *Total PV Inverter Power Loss*

The current distribution among semiconductors can be influenced by the *pf*. If the on-resistance and the built-in voltage of the IGBT and diode have significant difference, the current distribution will change the overall conduction loss of the PV inverter. For example, the majority of the current flows through IGBTs rather than diodes at unity *pf*.

If the on-resistance of the IGBT is larger than that of diode, the conduction loss of the PV inverter at unity *pf* will become larger than that at non-unity *pf*. If the on-resistance and the built-in voltage of the IGBT is similar to that of diodes in a PV inverter, the conduction loss of the PV inverter at unity *pf* will be similar to that at non-unity *pf*.

In typical PV inverter design, the selection of IGBTs and diodes often have similar conduction loss characteristics. Therefore, the total power loss of the inverter normally remains the same regardless of the *pf*. The total PV inverter power loss is typically determined by the apparent power.

Typically, the active power generation has higher priority than the reactive power generation in customer owned PV inverters. PV inverters are unlikely to sacrifice active power generation for reactive power because the compensation for active power greatly exceeds that for reactive power in today's markets. Since the active power and reactive power are in quadrature with each other, the increase of apparent power is not linearly proportional to the increase in reactive power.

Fig. 10 shows the phasor diagram of the PV inverter power with reactive power generation. When the active power generation is 0.2 p.u., the apparent power increment is 0.247 p.u. (to 0.447 p.u.) when generating 0.4 p.u. reactive power. When the active power generation is 0.8 p.u., the apparent power increment is 0.094 p.u. (to 0.894 p.u.) to generate 0.4 p.u. reactive power. In these two cases, to generate 0.4 p.u. reactive power, the additional apparent power (ΔS) of the PV inverter is quite different. In general, the ΔS of the PV inverter at larger active power generation level is less than that at smaller active power generation level. Similarly, the increment of power loss of the PV inverter at larger active power generation level is less that that at smaller active power generation level. Fig. 11 illustrates the apparent power with respect to reactive power.

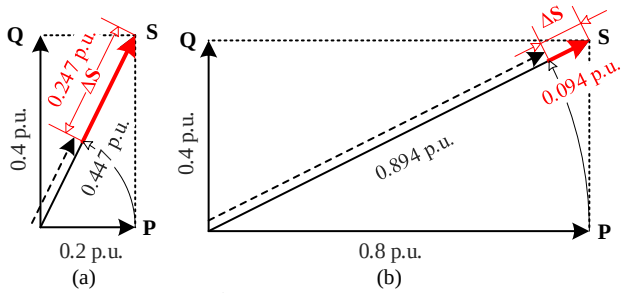


Fig. 10. Phasor diagram of PV inverters with reactive power generation.

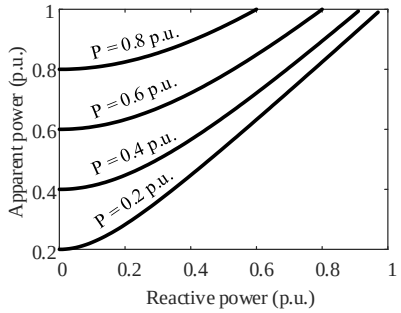


Fig. 11. Apparent power curve with respect to reactive power.

V. Simulation Results

A. Scenario Definition

The single-phase PV inverter topology shown in Fig. 4 is simulated in PLECS. The key parameters used in the simulation are summarized in Table IV. The semiconductor thermal models used in the simulation are from commercial device datasheets. The information of the devices used in this simulation is summarized in Table V. The PV inverter is connected to a 120-V ac voltage source. The output current is controlled to follow the power generation reference. The ambient temperature utilized in the simulation is 25 °C. A group of power loss simulations with different active-reactive power combinations are conducted. In this simulation study, the PV inverter is assumed to have the reactive power generation settings follow IEEE Standard 1547 [9] with maximum reactive power support to be 0.44 p.u.

Table IV. PV Inverter Key Parameters

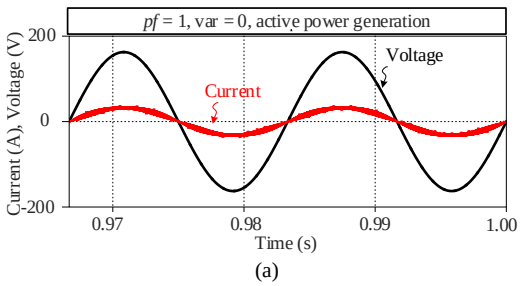
PV voltage, V_{PV}	50-70 V
DC link voltage, V_{dc}	200 V
Grid voltage, V_s	120 V
Power rating, P	2500 W
Switching frequency, f_{sw}	10 kHz
Fundamental frequency, f_0	60 Hz

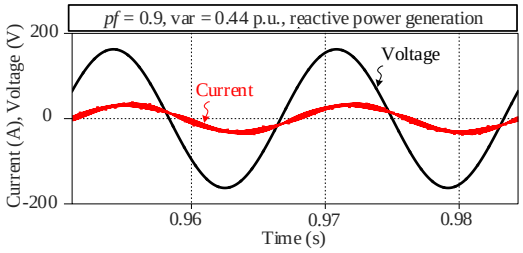
Table V. Semiconductor Device Information

Part No.	Manufacturer Part No.	Manufacturer	Package
S_1	IGP50N60T	Infineon	TO-220
D_1	C4D20120D	Wolfspeed	TO-247
S_2, S_3, S_4, S_5	IKW50N60H3	Infineon	TO-247
D_2, D_3, D_4, D_5	IKW50N60H3	Infineon	TO-247

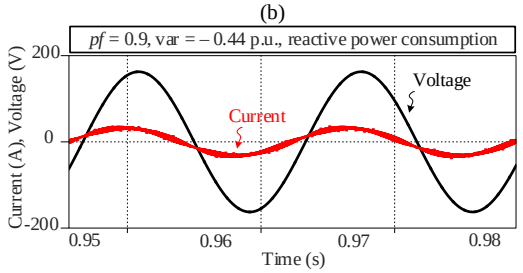
B. Basic Results

Figure 12 shows the output voltage and current waveforms from the PV inverter simulation. Fig. 12(a), (b), and (c) all have apparent power to be 2500 VA. A group of power loss simulations with different active-reactive power combination are conducted. The total power loss results are summarized in Fig. 13. Fig. 14 is the contour of Fig. 13. Fig. 13 shows the PV inverter total power loss in a 3-D plot. The *x*-axis is the active power, *y*-axis is the reactive power, and *z*-axis is the power loss. The traces in Fig. 14 are the power loss contours projected on the *xy*-plane. Fig. 14 shows that the power loss contour is in a circle. The total power loss of the PV inverter remains the same with different power factors.





(b)



(c)

Fig. 12. Sample waveforms from PV inverter simulation. (a) *pf* = 1, var =0; (b) *pf* = 0.9, var = 0.44 p.u.; and (c) *pf* = 0.9, var = – 0.44 p.u..

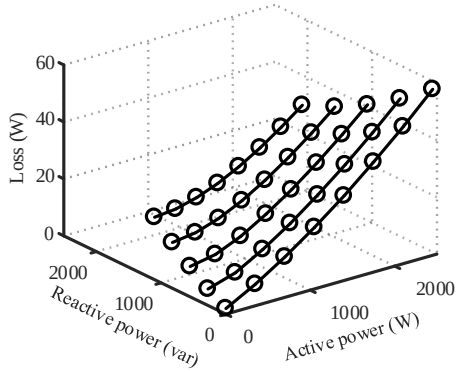


Fig. 13. PV inverter power loss results for different combinations of active and reactive power.

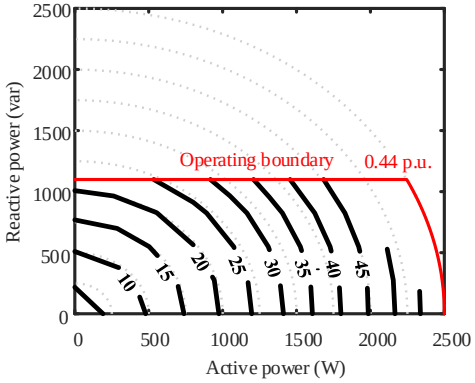
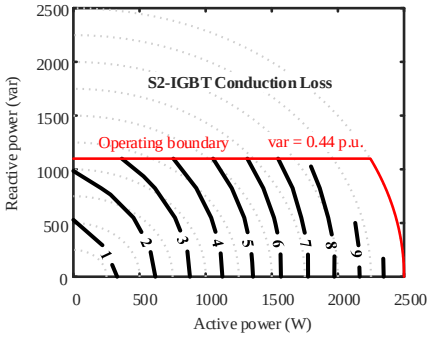


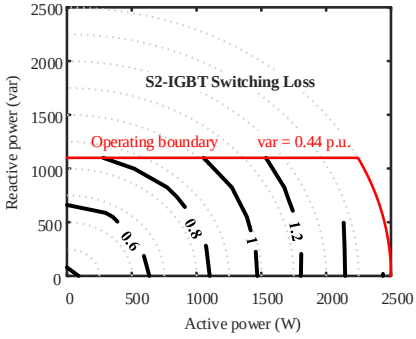
Fig. 14. Power loss contour of the PV inverter simulation.

C. *Semiconductor Power Loss*

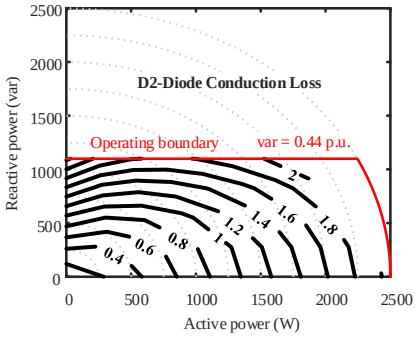
Fig. 15 shows the individual IGBT and diode power loss results. Note that the second stage of the PV inverter has four IGBTs and four diodes. Each semiconductor has power losses and switching losses. Fig. 15 selects one set of IGBTs and diodes to visualize the power loss contour so that the thermal stress of the diodes and IGBTs can be discriminated. In particular, Fig. 15(c) shows the diode conduction loss. The diode conduction loss increases as the *pf* decreases because more power flows through the diode instead of the IGBT. 2250-W active power for the converter can generate 1.8-W diode conduction loss, whereas only 1000-var reactive power generation can lead to 1.8-W diode conduction loss. From Fig. 15(a), the conduction loss of the IGBT is slightly decreased as the *pf* decreases. From Fig. 15(b) and (d), the switching loss of the IGBT and the reverse recovery loss of the diode do not have significant correlation with the power factor.



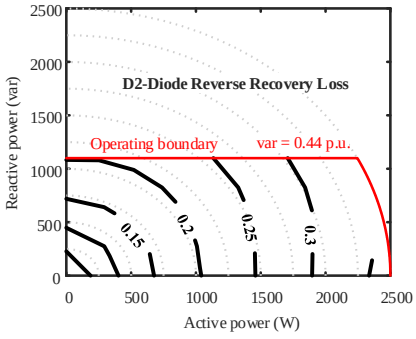
(a)



(b)



(c)



(d)

Fig. 15. Semiconductor power loss contour with respect to difference loading conditions. (a) IGBT conduction loss; (b) IGBT switching loss; (c) diode conduction loss; and (d) diode reverse recovery loss.

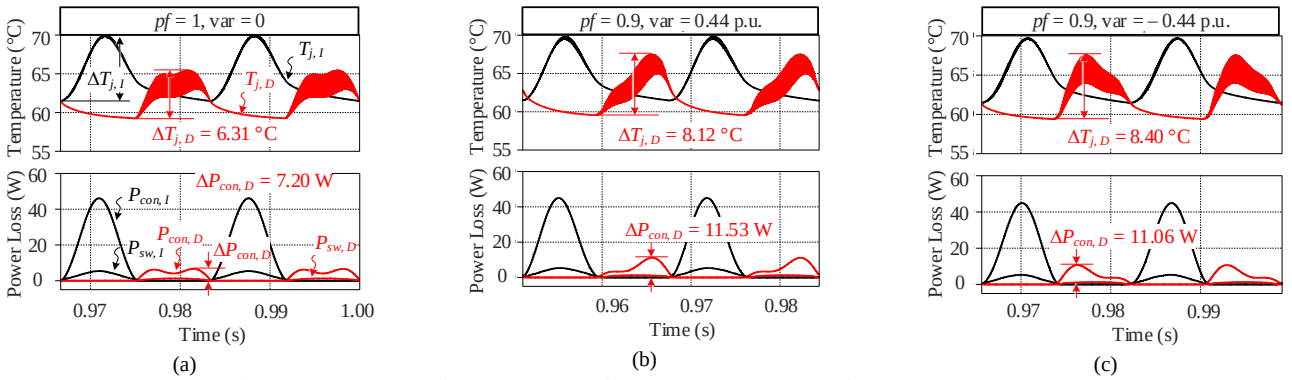


Fig. 16. Junction temperature of IGBT and diode. (a) *pf* = 1, var = 0. (b) *pf* = 0.9, var = 0.44 p.u.. (c) *pf* = 0.9, var = – 0.44 p.u..

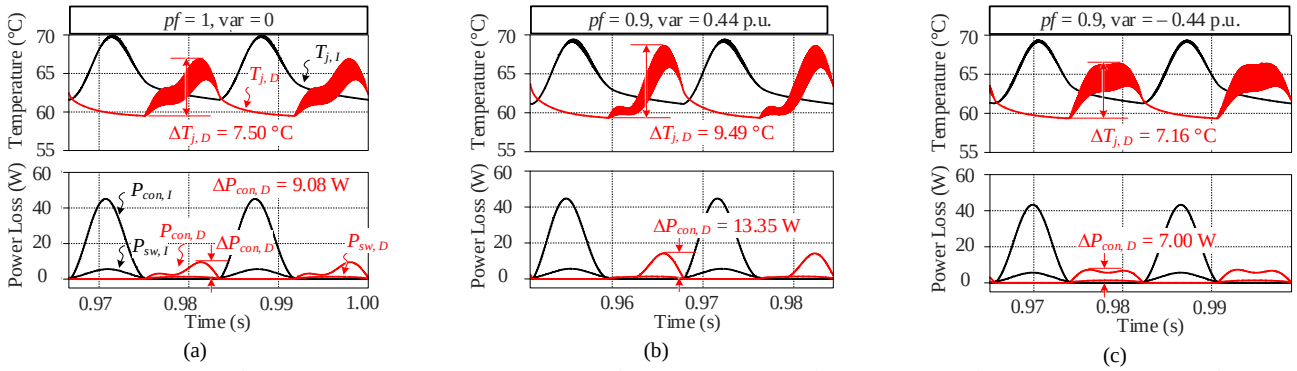


Fig. 17. Junction temperature of IGBT and diode with 50-mH (32.7% p.u.) filtering inductor. (a) *pf* = 1, var = 0. (b) *pf* = 0.9, var = 0.44 p.u.. (c) *pf* = 0.9, var = – 0.44 p.u..

D. Thermal Cycle

Fig. 16 shows the junction temperature of the IGBT and diode at the location S_2 D_2 in Fig. 4. The filtering inductor used in this simulation is 0.2 mH (1.3% p.u.). Fig. 16 presents three operating points: a) *pf* = 1, var = 0; b) *pf* = 0.9, var = 0.44 p.u.; and c) *pf* = 0.9, var = – 0.44 p.u.. The thermal model in Fig. 2 is used in this simulation study. The IGBT junction temperature ($T_{j,I}$ and $\Delta T_{j,I}$) for these three cases remains the same. On the other hand, the diode junction temperature variation ($\Delta T_{j,D}$) shows a significant difference among the three cases. As discussed in Section V-*B*, the diode current variation in a fundamental cycle may double when the *pf* = 0.9. This will lead to larger diode junction temperature variation in a fundamental cycle.

Fig. 16 (b) and (c) show that the diode junction temperature variation ($\Delta T_{j,D}$) is more than 8 °C when *pf* = 0.9, whereas Fig. 16(a) shows that the junction temperature variation ($\Delta T_{j,D}$) is 6.3 °C when *pf* = 1. A higher junction temperature will significantly influence the lifetime of the diode.

E. Filtering Inductor Effect

Fig. 17 shows the junction temperature of the PV inverter's IGBT and diode when the filtering inductor is relatively large (5 mH, 32.7% p.u.). Fig. 17 presents three operating points: a) *pf* = 1, var = 0; b) *pf* = 0.9, var = 0.44 p.u.; and c) *pf* = 0.9, var = – 0.44 p.u.. The IGBT junction temperature ($T_{j,I}$ and $\Delta T_{j,I}$) of these three cases remains the same. On the other hand, the diode junction temperature variation ($\Delta T_{j,D}$) has a significant difference for the three cases.

As discussed in Section V-*C*, the bridge circuit *pf* needs to include the filtering inductor as part of the load. When the output *pf* is 1 as shown in Fig. 17(a), the bridge circuit *pf* is slightly inductive. Hence, the diode junction temperature waveform in Fig. 17(a) is similar to that in Fig. 16(b). When the load is inductive as shown in Fig. 17(b), the bridge circuit *pf* is more inductive. This leads to even greater diode junction temperature variation. When the load is capacitive as shown in Fig. 17(c), the filtering inductor can be compensated by the load. The bridge circuit *pf* is close to unity. Therefore, the diode junction temperature variation is the least among the three cases.

F. Semiconductor Aging Analysis

To assess the aging effect of the reactive power generation, a theoretical-model-based assessment platform is established. The workflow of the theoretical-model-based assessment is shown in Fig. 18. This platform calculates the cycles to failure N_f of inverter semiconductors (IGBTs and diodes) using the theoretical models discussed in Section II and III. The PV inverter under analysis is the same as Section V-*A*. The input of the platform is the power generation of the two-stage PV inverter. The junction temperatures of inverter diodes and IGBTs are calculated accordingly.

Fig. 19 shows the junction temperature results from the theoretical models in comparison with that from the PLECS simulation. From Fig. 19, the diode junction temperature variation from the theoretical models is less than that of the PLECS simulation, whereas the IGBT junction temperature variation from the theoretical models is larger than that of the

PLECS simulation. This is because the theoretical model linearizes the semiconductor power loss model by using a built-in voltage source ($V_{0,D}$ or $V_{0,IGBT}$) and an on-resistor (R_D or R_{IGBT}). The theoretical models of the diodes and the IGBTs of this paper are linearized from the 175-ºC data from the device datasheets.

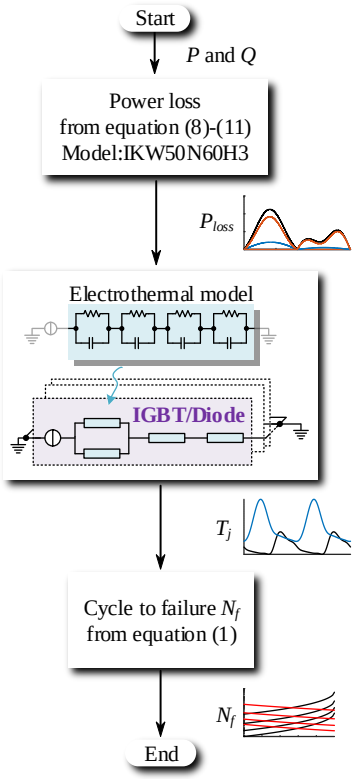


Fig. 18. Workflow of semiconductor aging effect assessment platform.

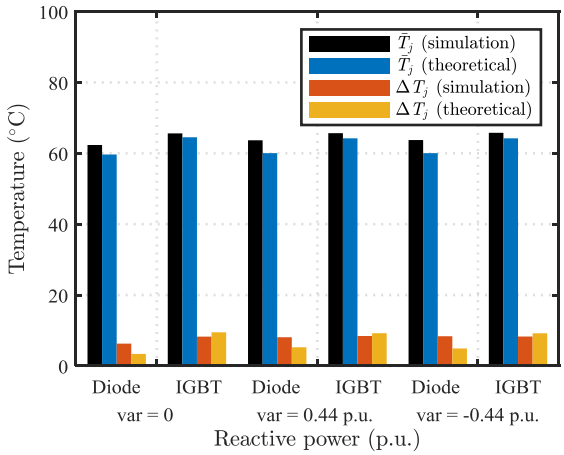
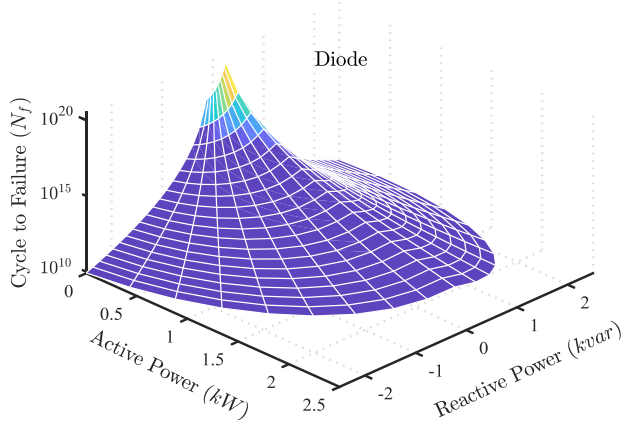


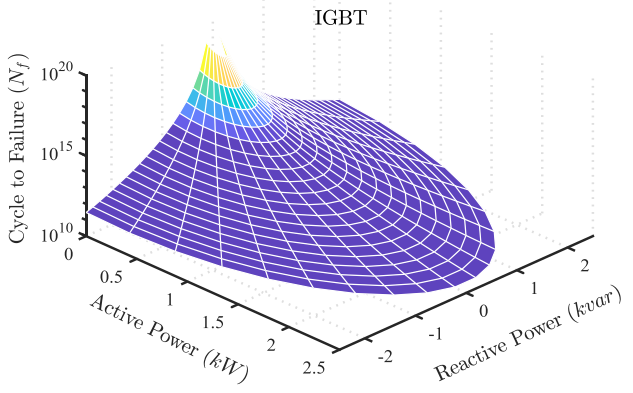
Fig. 19. Junction temperature results from the theoretical models in comparison with that from the PLECS simulation.

From Fig. 19, the average temperatures of inverter diodes and IGBTs from the theoretical model is slightly smaller than that of the PLECS simulation. The average temperature in largely determined by the sum of the IGBT and diode power losses. The overall power loss from the theoretical model is less than that of the PLECS simulation. This leads to the small differences in average junction temperatures between the theoretical model and PLECS simulation. Despite the discrepancies in absolute values between the theoretical model and the PLECS simulation, the theoretical model can properly track the trends of junction temperature given different levels of PV generation.

The junction temperature profiles of PV inverter semiconductors are used for calculating the cycle-to-failure (N_f) from (1). The aging analysis of this paper is based on the theoretical model. Fig. 20 shows the N_f of PV inverter diodes and IGBTs with respect to different PV generation. When the active power generation is small (less than 1.5 kW), a small amount of reactive power generation/absorption will drastically reduce the semiconductor N_f. When the active power generation is large (more than 1.5 kW), extra reactive power generation/absorption will only slightly reduce the semiconductor N_f. In general, the additional reactive power generation/absorption reduces the semiconductor N_f. However, the N_f reduction effect depends on the PV inverter active power production. The reduction of N_f at small active power generation levels is more than that at large active power generation levels.



(a)



(b)

Fig. 20. (a) Number of cycles to failure for the PV inverter diodes. (b) Number of cycles to failure for the PV inverter IGBTs.

Fig. 21 shows the N_f of PV inverter diodes and IGBTs with respect to different power factors. As discussed in Sections

V-*C* and *D*, the power loss of diodes increases as the *pf* decreases. Also, the junction temperature variation for diodes increases as the *pf* decreases. Larger thermal cycle will accelerate the failure of diodes. The diode N_f decreases as the *pf* decreases. This can be seen from Fig. 21. Similarly, the power loss of IGBTs decreases as the *pf* decreases. Also, the junction temperature variation for IGBTs decreases as the *pf* decreases. Smaller thermal cycle (ΔT_j) will lead to longer IGBT lifetime. The IGBT N_f increases as the *pf* decreases. Low *pf* will help extend the IGBT lifetime. This can be seen from Fig. 21.

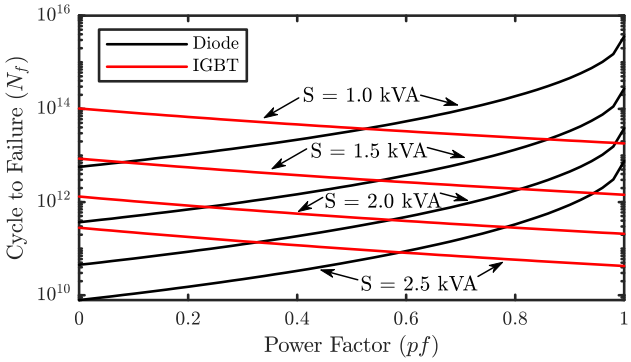


Fig. 21. N_f of PV inverter diodes and IGBTs with respect to power factors.

Fig. 22 shows the N_f of PV inverter diodes and IGBTs with respect to different reactive power generation levels. In the ancillary services market, the PV inverter is typically requested to provide reactive power in addition to the maximum active power point, thus extra reactive power generation leads to extra power loss. Both the diodes and IGBTs will suffer from the extra heat. This can be seen from Fig. 22. Both diode N_f and IGBT N_f decrease as the reactive power increases. However, the reactive power aging effects on the IGBTs and diodes are slightly different. The diode N_f is much more sensitive to the reactive power than the IGBT N_f. Diode N_f decreases more than 100 times when the reactive power increases from 0 to 0.44 p.u., whereas the IGBT N_f decreases less than 10 times when the reactive power increases from 0 to 0.44 p.u..

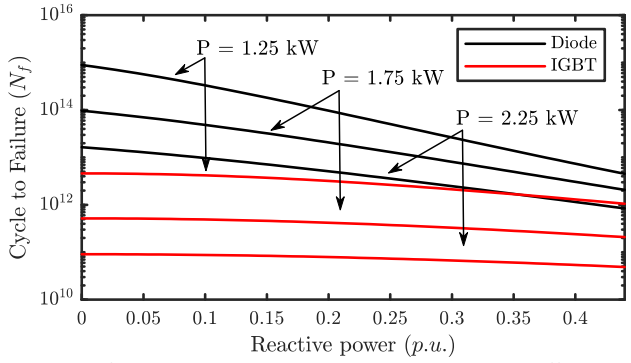


Fig. 22. N_f of PV inverter diodes and IGBTs with respect to different var generation.

Fig. 23 shows the N_f of PV inverter diodes and IGBTs with respect to different filter inductances. In general, the filtering inductor will accelerate the semiconductor aging for both diodes and IGBTs. However, the filter inductor aging effects on the IGBTs and diodes are slightly different. The diode N_f is much more sensitive to the filter inductor value than the IGBT N_f. Diode N_f decreases more than 10 times when the filter inductance increases from 0 to 0.3 p.u., whereas the IGBT N_f decreases less than 10 times when the reactive power increases from 0 to 0.3 p.u..

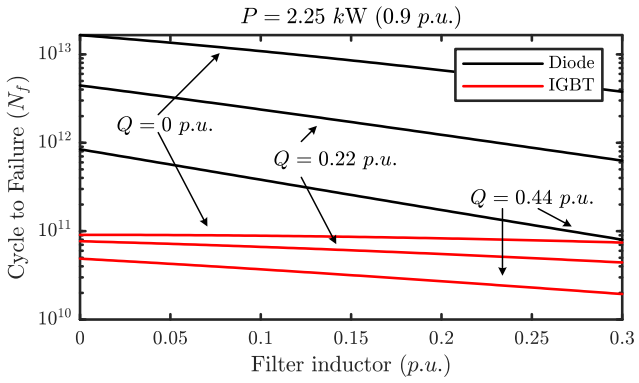


Fig. 23. N_f of PV inverter diodes and IGBTs with respect to different filter inductances.

VI. Conclusion

This paper develops the lifetime model of the semiconductors in a PV inverter by integrating the semiconductor electrothermal model and the PV inverter modulation. The lifetime model formulates the inverter semiconductors' thermal stress under the scenarios where the PV inverter is engaged in reactive power support. Both the analysis and the simulation results show that the average conduction loss of inverter diodes increases when the output current *pf* decreases. In addition to the average conduction loss of diodes, the conduction loss variation of the diodes doubles when the *pf* decreases to 0.9. The aging effect of the extra thermal stress on diodes also shows that the diodes suffer from accelerated aging during the reactive power support.

The filtering inductor impact on the semiconductor current distribution also has to be considered because of its effect on the power factor of the output current and resulting current distribution among the inverter's IGBTs and diodes. The analysis and simulation results show that the filtering inductor can increase the conduction loss variation of diodes when the load is inductive. The extra power losses in diodes lead to shorter lifetime expectation of PV inverter diodes.

PV inverter manufacturers will need to account for the provision of ancillary services, and in particular reactive power support, in the design of future products in order to ensure that provision of ancillary services does not negatively impact the lifetime of their products. This may include needing to use higher current ratings in the anti-parallel diodes and more closely examining the parasitics in their dc link capacitors and filter inductors.

Appendix

Assume that the grid voltage and current are

$$v_s = \sqrt{2}V_s \sin(\omega t + \varphi) \quad \text{(A.1)}$$

$$i_s = \sqrt{2}I_s \sin \omega t \quad \text{(A.2)}$$

where ω is the fundamental frequency, and φ is the phase difference.

$$I_{rms,MOSFET} = \frac{I_S}{2}\sqrt{1 + \frac{8M\cos\varphi}{3\pi}} \quad \text{(A.3)}$$

$$I_{rms,IGBT} = \frac{I_S}{2}\sqrt{1 + \frac{8M\cos\varphi}{3\pi}} \quad \text{(A.4)}$$

$$I_{avg,IGBT} = \frac{I_S}{\sqrt{2}\pi}\left(1 + \frac{\pi M\cos\varphi}{4}\right) \quad \text{(A.5)}$$

$$I_{rms,D} = \frac{I_S}{2}\sqrt{1 - \frac{8M\cos\varphi}{3\pi}} \quad \text{(A.6)}$$

$$I_{avg,D} = \frac{I_S}{\sqrt{2}\pi}\left(1 - \frac{\pi M\cos\varphi}{4}\right) \quad \text{(A.7)}$$

where M is the modulation index of the inverter. The MOSFET can conduct the reverse current through the main MOSFET or built-in body diode depending on the gate-to-source voltage. Typically, the reverse current is conducted through the main MOSFET rather than body diodes for PV inverters. If that is the case, the diode current (A.6) and (A.7) will also be conducted by MOSFET. The reverse voltage-current characteristics of the MOSFET is similar to the forward voltage-current characteristics of the MOSFET except for different values for reverse $R_{ds(\text{on})}$. The derivation of (A.3)-(A.7) is given in [38].

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