A High Frequency Wireless Power Transfer System for Electric Vehicle Charging Using Multi-layer Non-uniform Self-resonant Coil at MHz

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***Abstract*—A high power, high frequency wireless power transfer system for EV applications is proposed in this paper with lightweight and compact coil design. Leveraging a multi-layer non-uniform self-resonant coil, no external capacitor is needed for compensation and the high frequency conduction loss is mitigated by sharing current between multiple copper layers. Prototype coils with 200 mm radius are fabricated and tested, achieving quality factor over 450 at 3 MHz. The optimized design for both coils and a GaN-based power stage are detailed and validated experimentally. Experimental tests show 93.2% dc-dc efficiency with 2.4kW transferred across a 100 mm air gap.**

Keywords—self-resonant coil, multi-layer spiral coil, wireless power transfer, electric vehicle charging

I. Introduction on Motivations

With the increasing public awareness of the environmental impact of greenhouse gas emissions, electric vehicles (EVs) have drawn worldwide attention as the potential successor to gasoline vehicles. Wireless power transfer (WPT) allows EV battery charging without a physical, cable connection in a safe, robust and unobtrusive way in contrast to the conventional wired EV chargers. The wireless charging coils are buried underground, allowing the charging station space to be reduced. In addition, charging plugs, which can be easily damaged or cause electric safety concern without supervision, are no longer required [1].

Based on the different coupling mechanism between transmitter side and receiver side of the WPT system, there are two types of WPT techniques as candidates for high power wireless EV applications: Inductive Power Transfer (IPT) and Capacitive Power Transfer (CPT) [2]-[5]. Fig. 1 summarizes the state-of-the-art WPT systems for EV charger applications, with the power ranging from serval hundred watts to kilowatts and the switching frequency ranging from tens of kilohertz to several megahertz. The color of dot represents the WPT technique applied. Critical performance specifications are also listed in Fig. 1, including system DC-DC efficiency, coil power density, and power transfer distance. Inductive power transfer (IPT) systems have power rating up to tens of kilowatts, but most use frequencies below 250 kHz [6]-[10]. Since there is no high frequency core loss and winding loss, capacitive power transfer (CPT) systems tend to work in higher frequency range in order to increase coupling between the metal plates [11][12] but have limited power density and power rating. Work in [13] provides a concept to integrate IPT and CPT systems, but power density is still not comparable to IPT systems. Compared with IPT, CPT does not require expensive high frequency litz wires or a magnetic core, which aids the high frequency design to reduce the weight of passive components. However, CPT suffers from two major issues: low coupling capacitance and high fringing field. Capacitive coupling requires a relatively large coupling area to achieve large coupling capacitance, imposing a design challenge on high power density. For high power EV applications with a large air gap, the transmission efficiency is low due to the low coupling [14]-[17]. The high fringing field at the edge of coupled metal plate pairs is another concern because of electric field exposure limits on the human body [18][19].

IPT is a relatively mature technology for WPT systems for EV chargers with air gap up to dozens of centimeters. However, the efficiency and power rating of IPT systems are often limited by low coupling between the transmitter coil and receiver coil due to the large air gap. This issue can be addressed by using

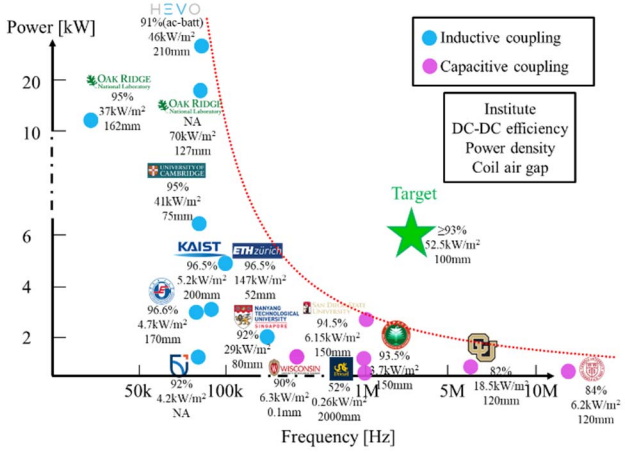


Fig. 1. State-of-the-art WPT systems for EV charger

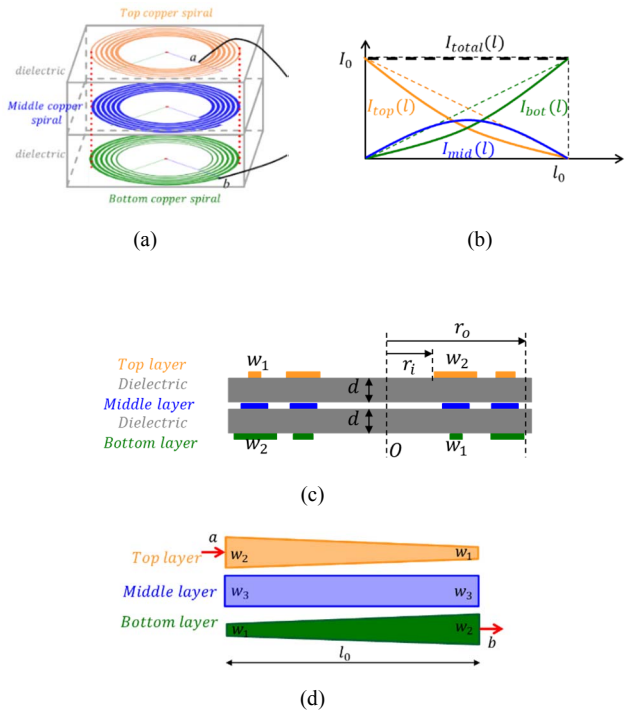


Fig. 2. Three-layer non-uniform SR coil structure (a) 3D view (b) current distribution along each copper trace (c) cross section view (d) top view of unfurled copper traces for top, middle and bottom layers

more litz wire windings or heavier magnetic cores and having larger coils up to 400 mm-500 mm in radius to gain larger inductance value and higher coupling coefficient. However, the efficiency and power density are often sacrificed, and overall manufacturing cost is inevitably increased.

In this paper, a high power, high frequency wireless EV charger is demonstrated utilizing the multi-layer non-uniform self-resonant (SR) coil in [20]. By pushing for higher frequency, smaller air-core coils with lower inductance value can be applied for the same power transfer. Litz wire is excessively expensive for strand diameters below 50 µm and may result in higher loss than solid-core copper for MHz frequencies with larger strand diameter. The multi-layer self-resonant coil structure used in this work allows high quality factor coils to be fabricated from layers of inexpensive copper foil and dielectric film. Additionally, the self-resonant coil utilizes its interlayer capacitance for resonance, eliminating the external compensation capacitor and shrinking the overall volume of passive component to increase power density.

II. Three-Layer Non-Uniform Self-Resonant Coil Review and Optimization Process

A novel three-layer non-uniform SR coil for WPT applications has been proposed in [20]. Compared to the conventional SR coil designs, it has the advantages of high inductance, high quality factor, and exhibits a series *L-C* resonant characteristic. The structure of a three-layer non-uniform SR coil is shown in Fig. 2(a). Three layers of copper spiral traces are stacked vertically, with two layers of dielectric material sandwiched between. From one end of the copper trace on top layer, terminal *a*, the current transfers gradually to the bottom layer copper trace to the other end, terminal *b*, through the middle copper layer in the form of displacement current, as shown in Fig. 2(b). To control the current sharing among the three layers, the geometry of the traces is manipulated to have non-uniform width. As shown in Fig. 2(c)-(d), the width of the top layer is linearly decreasing from w_2 to w_1, while on the bottom layer it is linearly increasing from w_1 to w_2. The width of middle layer is a constant, w_3. Due to the non-uniform copper width, the per-length capacitances formed between adjacent copper layers are varying along the trace length l_0. This variable capacitance is used to control the impedance and thereby the current distribution between the three layers.

Based on the structural analysis above, the design of both inductance and capacitance values are coupled by the geometry of the coil and the properties of the dielectric material. The coil inner radius r_i, outer radius r_o and number of turns N determine the inductance value, and these parameters also strongly affect the copper foil overlapping area and determine the total capacitance. At the same time, any change of capacitance value is limited by the available area for copper foil, which is bounded by the inductor trace design. The detailed coil *RLC* modeling process is given in [20].

With a fixed size, there is a single coil geometry which will exhibit the highest quality factor for any achievable pair of inductance and capacitance of the self-resonant coil. Between these designs, selection of the optimal (*L*,*C*) pair requires consideration of the power stages and overall converter operation, which is addressed in the following section. Initially, coil design space is narrowed by considering only the optimal quality factor designs for any (*L*,*C*) pair. To capture the optimal quality factor design considering different inductance and capacitance pairs, design parameters including coil resonant frequency f_0, inductance L, capacitance C, inner radius r_i, number of turns N, copper trace width w_1, w_2, and w_3, and dielectric material thickness d are swept to generate feasible coil design. The coil design flow chart in shown in Fig. 3.

Results of a design sweep with $f_0 = 3$ MHz are shown in Fig. 4. Larger coil outer radius r_o facilitates a higher quality factor coil design at any inductance value. Note that the abrupt Q drop at $L = 15$ µH for $r_o = 200$ mm is due to an abrupt change in N. The dielectric material properties align with the ROGERS Teflon laminates RO3003 [21], with relative dielectric constant $\varepsilon_r = 3$, maximum thickness $d = 1.52$mm, and loss tangent $D_k = 0.001$. The copper trace thickness $t = 2$ oz from electrodeposited copper foil on the dielectrics. The minimum inner radius r_i is fixed at one third of the outer radius r_o. The minimum copper trace width is set as 0.1 mm considering practical fabrication limits. In the sweeping process, N is always pre-selected as the minimum number based on the inductance L requirement, since any larger N results in larger copper trace length and will unnecessarily increase the coil loss significantly.

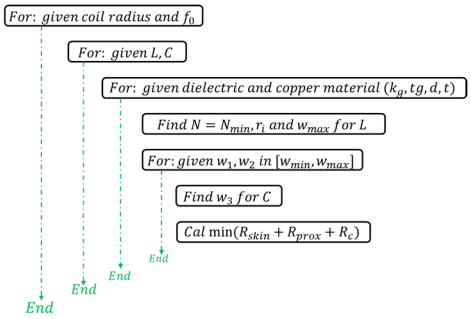


Fig. 3. Design flow chart for coil geometry

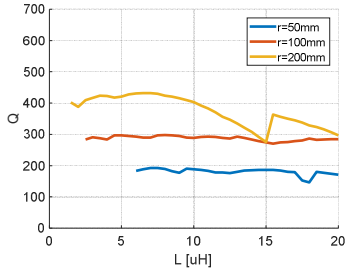


Fig. 4. Coil quality factor comparison with radius, f_0 = 3 MHz

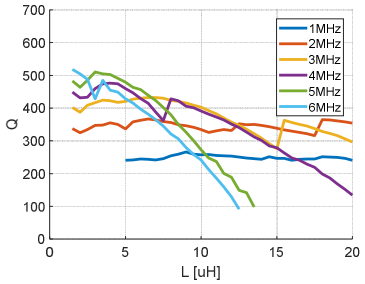


Fig. 5. Coil quality factor comparison with frequency, r_o = 200 mm

The complete coil design result is given in Fig. 5, with coil outer radius r_o = 200 mm and resonant frequency ranging from 1 MHz to 6 MHz. This plot contains the optimal coil design for a range of coil inductances. The highest quality factor coils occur with very small inductance and high frequency. These designs do not necessarily guarantee the highest system efficiency; instead, the coil design in Fig. 5 is combined with a system-level design optimization including power stages to determine the best overall system design.

III. Wireless Charging System Design Process

A. System Design Flow Chart

The integrated system design flow chart is shown in Fig. 6. For a given system power rating P_o and output voltage V_{2DC}, the system efficiency is calculated as both the transmitter and receiver coil designs are swept across all locally-optimal designs from the previous section. Note that the coupling coefficient between two coils is also a strong factor affecting the system operating point, which is determined by the coil geometries and distance between them. In the design of Fig. 6, k is calculated each iteration for a fixed coil-to-coil distance.

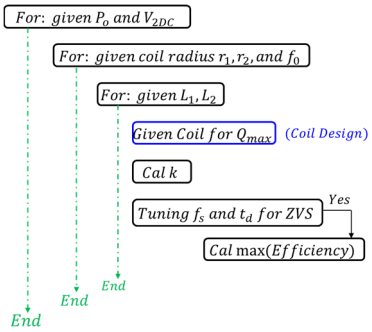


Fig. 6. Design flow chart for WPT system

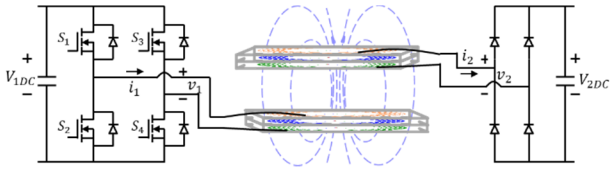


Fig. 7. Proposed WPT system diagram with SR coil

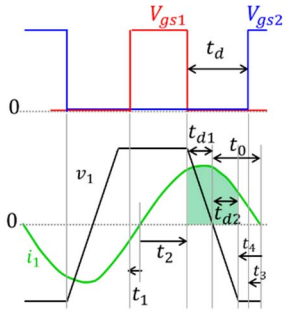


Fig. 8. Waveforms for inverter gate signals V_{gs1}, V_{gs2}, and inverter switching node voltage v_1, current i_1 within one switching cycle

In this section, the power stage loss models are based on GS66508T 650 V GaN transistors from GaN Systems and C4D08120E 1200 V SiC Schottky diodes from CREE for the high frequency inverter and rectifier, respectively. In the system modeling process, the full bridge inverter is simplified as the fundamental frequency model, while the diode bridge is accurately modeled considering the diode junction capacitance effect during the high frequency transient, as discussed in [22]. The complete system diagram is plotted in Fig. 7. The coils are designed with radius up to r_o = 200 mm and an air gap of 100 mm. Input and output voltages are allowed to vary, but constrained below voltage ratings of the selected GaNFET and Diode.

For such high power, high frequency power stage, the zero-voltage-switching (ZVS) condition should always be maintained within the wide load range to avoid any hard switching at MHz switching dynamics. As shown in Fig. 8, proper tuning of the switching frequency f_s around the coil resonant frequency f_0 gives a positive phase shift t_0 between the inverter output voltage and current for ZVS. The green shaded area is the total charge $2Q_{oss}$ during the dead-time for the completion of ZVS, with the following charge condition for time intervals t_{d1} and t_{d2},

$$Q_{oss} = \int_{t_0}^{t_0+t_{d1}} \sqrt{2} I_1 \sin(\omega_s t) dt \quad (1)$$

$$Q_{oss} = \int_{t_0-t_{d2}}^{t_0} \sqrt{2} I_1 \sin(\omega_s t) dt \quad (2)$$

And a boundary condition for the dead-time t_d is required to ensure ZVS,

$$t_{d1} + t_{d2} \le t_d \le t_{d1} + t_0 \quad (3)$$

The lower boundary of dead-time $t_{d1} + t_{d2}$ is determined by the total charge $2Q_{oss}$, and the upper boundary $t_{d1} + t_0$ prevents any re-charging of C_{oss} by the current i_1 with reversed direction. In the system optimization process, t_d is selected as the averaged value of two boundaries to avoid any accidental half-ZVS due to the modeling error.

B. System Loss Model

A detailed system loss model is provided in this part. The conduction loss is,

$$P_{con+} = 4 \times \frac{1}{T_s} \int_{t_1}^{t_2} i_1^2 R_{ds} dt$$
$$= 4 \times f_s I_1^2 \left[t_2 - \frac{\sin(2\omega_s t_2)}{2\omega_s} - t_1 + \frac{\sin(2\omega_s t_1)}{2\omega_s} \right] R_{ds} \quad (4)$$

The reverse conduction time, t_4-t_3, should be minimized especially when applying a large negative off-state gate voltage. The reverse conduction loss is,

$$P_{rev} = 4 \times \frac{1}{T_s} \int_{t_3}^{t_4} (v_{0rev} + R_{rev} i_1) i_1 dt \quad (5)$$

$$P_{rev} = 4 \times [v_{0rev} \left(-\frac{\sqrt{2} I_1}{2\pi} \right) [cos(\omega_s t_4) - \cos(\omega_s t_3)] +$$
$$f_s I_1^2 [t_4 - \frac{\sin(2\omega_s t_4)}{2\omega_s} - t_3 + \frac{\sin(2\omega_s t_3)}{2\omega_s}] R_{rev}] \quad (6)$$

where I_1 is the RMS value of i_1, R_{ds} is the conducting resistance during on-time, R_{rev} is the reverse conduction resistance, v_{0rev} is the forward voltage when reverse conducting. Adding these two parts together gives the total conduction loss,

$$P_{GaN\_con} = P_{con+} + P_{rev} \quad (7)$$

The residual turn-off loss with ZVS fulfilled is estimated by the difference between the hard switching energy E_{off} and the energy stored in C_{oss} from device datasheet.

$$P_{off} = 4 \times f_s \times (E_{off} - E_{oss}) \quad (8)$$

The total loss related to GaN switches under ZVS condition is given by,

$$P_{GaN} = P_{con+} + P_{rev} + P_{off} \quad (9)$$

Together with the diode bridge conduction loss and coil conduction loss,

$$P_D = 4 \times (v_0 I_{dave} + I_{drms}^2 R_d) \quad (10)$$

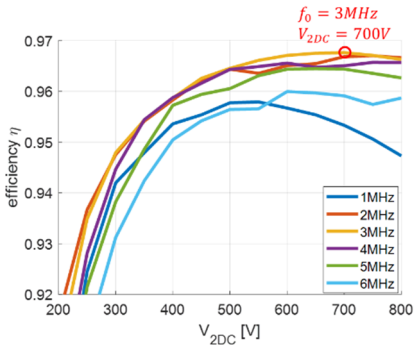


Fig. 9. Efficiency comparison with coil resonant frequency f_0 and load voltage V_{2DC}

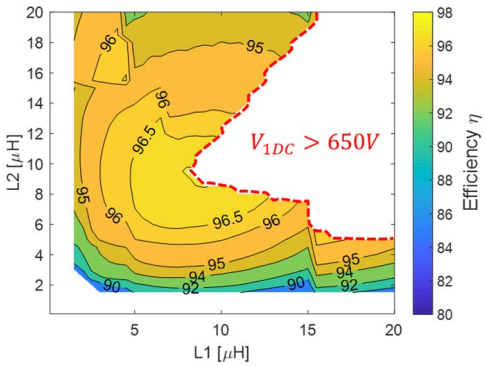


Fig. 10. System efficiency contour, V_{2DC} = 700 V, f_0 = 3 MHz

$$= 4 \times (v_0 \frac{\sqrt{2} I_2}{\pi} + \frac{I_2^2}{2} R_d)$$

$$P_{coil} = I_1^2 R_1 + I_2^2 R_2 \quad (11)$$

the final system efficiency is,

$$\eta = \frac{P_o}{P_o + P_{GaN\_con} + P_{off} + P_D + P_{coil}} \quad (12)$$

where I_2 is the RMS value of i_2, v_0 is the diode forward voltage, R_d is the diode resistance during conduction.

C. System Efficiency Contour and Analysis

After the optimization within both coil level and system level, the projected system efficiency is shown in Fig. 9 with different coil resonant frequency. The target power rating is 6.6 kW and coil radius is 200 mm. The peak modeled efficiency point is achieved when f_0 = 3 MHz and V_{2DC} = 700 V. This design point is further expanded into the efficiency contour in Fig. 10, where the inductance value of primary side and secondary coil, L_1 and L_2 are used as variables.

With different combinations of L_1 and L_2, the coil quality factor (from Fig. 5) strongly impacts the system efficiency, but low-inductance designs have degraded performance due to excessive peak currents on the primary. The right side of Fig. 10 contains a blank area where designs were eliminated due to exceeding the 650 V voltage rating of GaN devices, which is also shown in the system input voltage contour in Fig. 11.

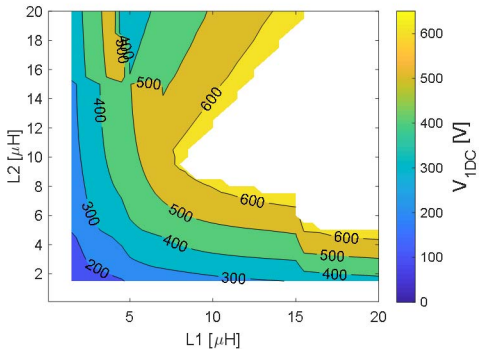


Fig. 11. System input voltage V_{1DC} contour, V_{2DC} = 700 V, f_0 = 3 MHz

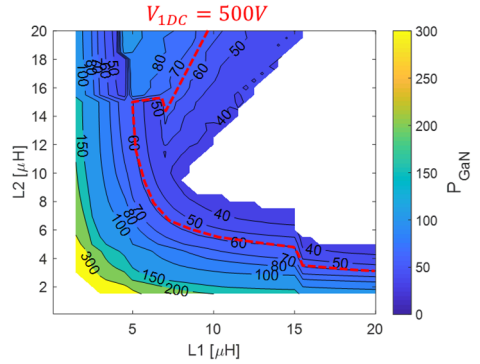


Fig. 12. GaN total loss contour, V_{2DC} = 700 V, f_0 = 3 MHz

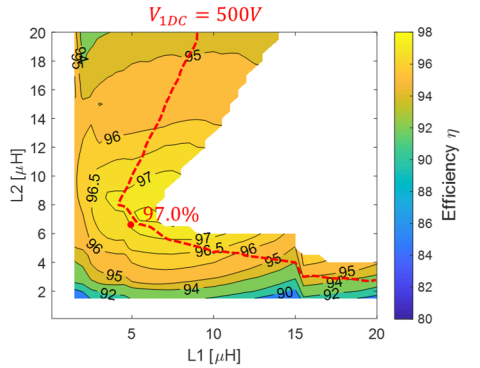


Fig. 13. Revised system efficiency contour with two GaN devices in parallel, V_{2DC} = 700 V, f_0 = 3 MHz

To evaluate the thermal stress on the high frequency switching GaN devices, the total loss in the GaN devices is plotted in Fig. 12. Note that the total loss for four devices is more than 60 W, or 15 W per device, when the input voltage is limited below 500 V as indicated by the red dash line. To mitigate heating and to further increase the system efficiency, two GaN switches are paralleled and Fig. 13 gives the revised efficiency contour. The highest efficiency design below the 500 V input voltage safety limit achieves 97.0% efficiency as marked in Fig. 13. The coil inductances are L_1 = 5 μH and L_2 = 6.5 μH, with predicted quality factor of 421 and 432, respectively. The final system at full power operates at input voltage V_{1DC} = 444 V, output voltage V_{2DC} = 700 V, and a switching frequency f_s = 3.04 MHz with coil resonant

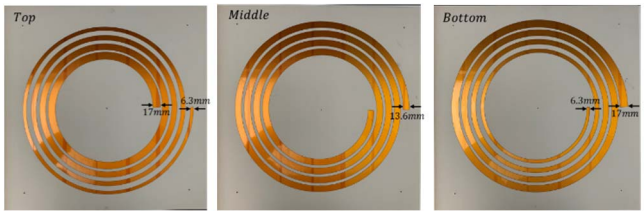


Fig. 14. Completed three copper layers for the receiver coil

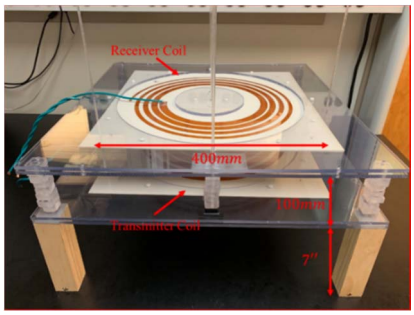


Fig. 15. Fabricated coils with mechanical setup

frequency f_0 = 3 MHz. The loss per GaN device is reduced from over 15 W to 5.4 W.

IV. Three-Layer Coil Fabrication and System Experimental Result

With the system operating point determined, two three-layer non-uniform SR coils have been fabricated with RO3003 laminates. The transmitter coil has inner radius r_i = 79.5 mm, N = 4 turns, and copper trace widths w_1 = 14.0 mm, w_2 = 19.8 mm, and w_3 = 18.0 mm. For the receiver coil, r_i = 106.7 mm, N = 4, w_1 = 6.3 mm, w_2 = 17.0 mm, and w_3 = 13.6 mm.

The coils are fabricated using laser cutting and chemical etching. Polyimide film tape from 3M is used to cover the entire copper cladding of the laminate first. The tape is dimensionally stable at the high temperature, flame retardant and chemical resistant. Then, a very low power laser is used to remove the unwanted bond tape, leaving only the spiral coil area covered to protect the copper for the acid etching. Note that the three spiral patterns on top, middle and top layers of a 3-layer coil should be center aligned for an accurate parasitic capacitance control. Ferric Chloride solution serves as the etching liquid and continuous agitation is applied for faster rate of reaction. After the spirals are fully etched, the coil is cleaned with isopropyl alcohol and deionized hot water, then baked for 1 hour in a 150 °C heat chamber. The three layers of the finished receiver coil are shown in Fig. 14.

The applied dielectric laminate RO3003 is rated for 300 V/mil. To check for degradation due to chemical exposure, a Phenix 6CP30/15-3 AC dielectric test set is used for dielectric strength measurement. The fabricated laminates sample passed the partial discharge test with less than 30 pC discharge at 4.4 kV RMS voltage, which is 2 times larger than the 1.7 kV RMS voltage on coil at full power and verifies the robustness of the laminates.

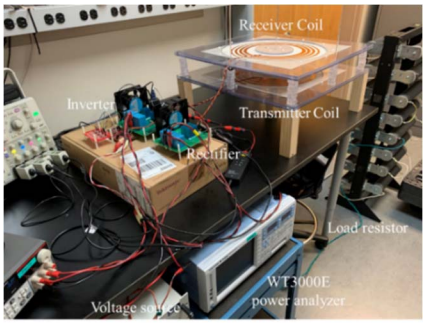


Fig. 16. System test setup with three-layer SR Coils

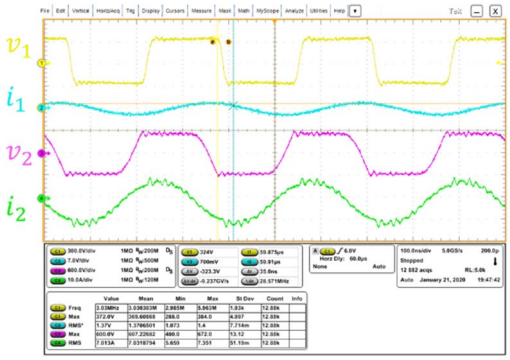


Fig. 17. Inverter output voltage v_1 current i_1, and rectifier input voltage v_2 current i_2 at 2.4 kW output

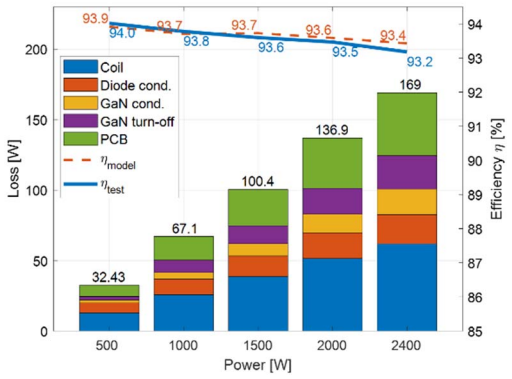
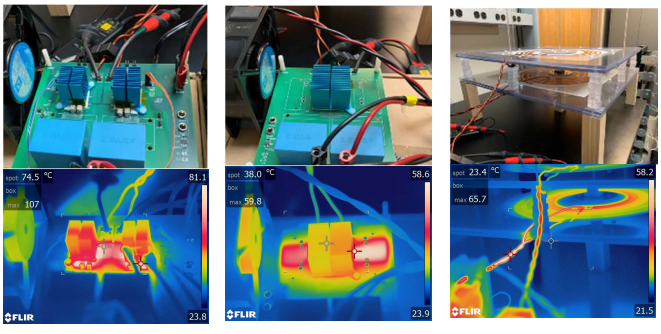


Fig. 18. System power loss breakdown for different power output



(a) (b) (c)

Fig. 19. Temperature distribution for 2.4 kW power test (a) inverter (107 °C) (b) rectifier (60 °C) (c) lead wire (66 °C) and coils (60 °C)

Fig. 15 shows the completed coils with mechanical support for testing. For each coil, the 3-later structure is held together with nylon screws. 0.25 inch polycarbonate sheets are applied for better clamping and 0.5 inch polycarbonate bars to control the air gap between two coils. A 20 mm clearance is kept from all holes in the laminates and polycarbonate parts to any copper traces to fulfill the creepage requirement from UL60950 and to avoid additional dielectric loss from the polycarbonate.

Table I shows the comparison between modeled, simulated, and measured coil parameters. The model is based on analysis supplemented with 2D magnetostatic FEA using FEMM. The HFSS simulation uses 3D electromagnetic FEA to verify resonant behavior. The fabricated coils have quality factor over 400, with less than 10% error from theoretical design point. Due to the impacts from both the strong H-field generated by the excitation source near coil and the limited meshing density, the 3D HFSS simulation gives relatively larger error for coil ESR.

TABLE I. SR coils characterization and comparison

	Model	HFSS simulation	Impedance analyzer
	Transmitter coil		
f_0 [MHz]	3	2.8	3
L [μH]	5	NA	5.2
R [Ω]	0.224	0.29	0.235
Q	421	303	417
	Receiver coil		
f_0 [MHz]	3	2.8	3.21
L [μH]	6.5	NA	6.7
R [Ω]	0.284	0.34	0.301
Q	432	336	452

The system experimental setup is shown in Fig. 16. The power stage and coils are connected via solid wires instead of stranded wires to minimize additional high frequency ac loss. Operating waveforms at 2.4 kW output are given in Fig. 17, showcasing full ZVS for the paralleled GaN switches. With 120 Ω load resistance, 3.03 MHz switching frequency, and 35 ns dead-time, the system efficiency is 93.2% measured with a Yokogawa WT3000E power analyzer. At this operating point, the input voltage is V_{1DC} = 310 V, load voltage V_{2DC} = 537 V, transmitter current I_1 = 13.5 A, and receiver current I_2 = 7.0 A.

The loss breakdown is calculated based on the tested operating condition for different output power and is shown in Fig. 18. Note that at 2.4 kW power output, more than 40 W of dielectric loss results from the parasitic capacitance of the FR4 PCB due to trace overlap between the switching mode and power ground. Additionally, this parasitic capacitance increases the primary side current required for full ZVS and causes more loss in the system. The GaN turn-off loss is over 30 W and mainly caused by the conservative gate resistor selection in the test to suppress cross-talk at high dv/dt switching. As summarized in Fig. 18, the system overall efficiency in the test is well-predicted by the system model, verifying the system design and optimization process as mentioned above.

The thermal images in Fig. 19 show the temperature distribution for inverter, rectifier, lead wire and coil. The maximum temperature point for inverter is above 100 °C due to the excessive turn-off loss and partial contribution from PCB

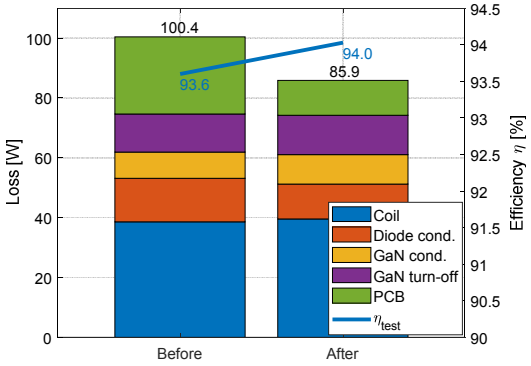
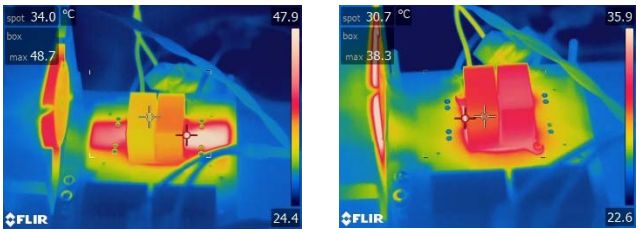


Fig. 20. System power loss breakdown comparison for before and after the PCB revision at 1.5 kW power output



(a) (b)

Fig. 21. Rectifier temperature distribution for 1.5 kW power test (a) before PCB revision (49 °C) (b) after PCB revision (38 °C)

heating. The temperature of the coils remains below 60 °C with natural convection, and the temperature distribution on the coils in Fig. 18(c) verifies the varying current distribution characteristic along the copper spiral trace in the proposed three-level SR coil.

To analyze the significance of PCB loss, a revision has been performed on the PCB board to manually cut off part of the copper area of the switching node of the diode bridge. Accordingly, the parasitic capacitance between the switching node and power ground drops from 358 pF to 96 pF based on impedance analyzer measurements. Fig. 20 provides a comparison of the loss breakdown before and after the revision at 1.5 kW power output. The PCB loss is reduced by more than half from 26 W to 12 W. The analysis is further verified by the temperature comparison in Fig. 21. The maximum temperature at diode bridge decreases from 49 °C to 38 °C due to the large drop of PCB loss while the diode conduction is only slightly reduced from 15 W to 12 W.

V. Conclusions

This work investigates the design of a high power, high frequency WPT system for EV applications. By leveraging the structural characteristics of multi-layer self-resonant coil, high quality factor coil design is possible with switching frequencies in the MHz range. The proposed air-core coil structure is low-cost, compact, and lightweight, with 200 mm radius, 3 mm thickness and only 2 oz copper traces. Both coil and system have been optimized, and there is a good alignment between the theoretical modeling and test result. A 2.4 kW power test achieving 93.2% system efficiency through a 100 mm air gap validates the concept of high frequency WPT system for EVs.

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