Small-Signal Impedance Analysis of the Impact of Grid-Forming Controllers on their DC and AC Dynamics

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***Abstract*—Grid-forming converters have recently been gaining more interest as a viable alternative to replace bulk synchronous generation for supporting and sustaining medium to low voltage grids. While the ability of grid-connected converters to support bulk generation has been thoroughly investigated, the capacity and behavior of converters that would replace bulk generation are not well defined. In an inverter-dominated system with one or more grid-forming inverters, maintaining dc-link stability is equally, if not more, important as maintaining frequency stability. To this end, and to better understand the behavior of grid-forming converters with different types of controllers, this paper derives the small-signal models for converters with nested and single-loop control structures, and compares their input and output impedance characteristics with and without synchronization. The analysis of input impedance provides insight into the impact of each grid-forming converter controller on upstream (dc) elements such as the dc-link and non-stiff dc sources, while the analysis of output impedance provides insight into the interaction of the controller with downstream (ac) elements of the grid such as the line impedance and loads. The analytical results are verified using simulation and experimental measurements.**

***Index Terms*—Grid-forming converter, impedance, small-signal, feedback loops, dc-link stability.**

I. Introduction

As it becomes more feasible to sustain an isolated grid with renewable energy sources, the role of 'grid-connected' converters will shift from that of supporting bulk generation to maintaining a stable grid voltage while feeding the loads, i.e. forming the grid. Hence, grid-forming converters have recently gained traction [1]–[4]. Many existing primary control techniques for grid-forming converters are derived from the established control methods for synchronous generators that these converters are meant to replace. However, some of these methods are not suitable for grid-forming converters.

The dc-link voltage between the renewable source or upstream dc-dc converter and the dc/ac converter is often considered analogous to the mechanical inertia of synchronous machines [5], and is utilized in various virtual inertia and frequency synchronization methods. However, in reality, the dc-link has limited reserves (unless an extremely large and expensive capacitor is used) and does not respond instantaneously to changes in frequency [6]. Moreover, the dc-link has different interactions with conventional synchronous machine controllers which can cause voltage instabilities.

Most conventional controllers for grid-forming converters use some form of voltage and frequency droop control using a nested control loop structure [7]. The outer loop regulates the voltage while the inner loop controls the current, each using feedback from the input and/or output terminals of the converter. These multiple feedback loops can destabilize the dc-link voltage, even when it is explicitly controlled. This paper analyzes the impact of the controller structure on the input impedance of a grid-forming converter to illustrate this behavior.

Several papers have been published in recent years that focus on the impedance interaction of grid-tied converters and the use of impedance-based methods to analyze the stability of converters and controller design [8]–[12]. Both input and output impedance (or admittance) studies for dc/ac converters are usually focused on the ac-side impedance, and the distinction between the two may depend on whether the converter is used in rectifying mode [11] or inverting mode [13]. Hence, dc-link dynamics are often disregarded, and the impact of any converter controller on the dc-link dynamics is rarely considered in impedance-based analyses.

This paper aims to fill that gap by representing the dc-link dynamics in the closed-loop input (dc) impedance of the converter and applying established impedance-based methods to deduce the impacts of controller feedback loops on dc-link voltage stability. Although these dynamics are commonly studied for load converters [14], [15], this paper will demonstrate similar phenomena in dc/ac source converters. While the upstream dc/dc converter or dc source also interacts with the dc link, this discussion will be focused solely on the impact of the dc/ac converter system.

A multitude of papers studying the input and output impedance of grid-connected converters attribute any instability or issues caused by the converter controller to the

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phase-locked loop (PLL) present in the controller [11], [13], [16]–[18]. However, in grid-forming inverter control, this PLL is replaced by either some form of droop control for parallel operation of multiple grid-forming inverters, or by a constant reference in the case of a single grid-forming inverter with/without multiple grid-following inverters. But even in the absence of a synchronization loop, there are certain issues caused by the use of multiple feedback loops. This will be shown by the impact of multiple feedback loops on the output admittance of a grid-forming converter.

The remainder of the paper is divided into four sections. Section II includes the derivation of the small-signal models for both dual and single feedback loop controllers both with and without droop control in grid-forming converters. These models are used to analyze the impact of the two control structures on the closed-loop input impedance and output admittance of the converter. Section III compares the results obtained from the small-signal impedance analysis of the controllers. Section IV describes the verification of the analytical results on a hardware platform. Finally, Section V concludes the paper with a summary of the observations.

II. Input and Output Impedance of Grid-Forming Converters

This section will focus on deriving the transfer functions of open-loop and closed-loop input impedance and output admittance for nested control loops and a single control loop in a grid-forming converter. Subsequently, an outer loop with droop regulation is added to both controllers to determine the impact of synchronization on these two control structures. The nested control structure consists of the same voltage control loop as that of the single control loop structure as well as an inner control loop with d-q decoupling, as shown in Fig. 1. The voltage reference can be constant for single operation or be received from the droop control loop for parallel operation of a grid-forming converter.

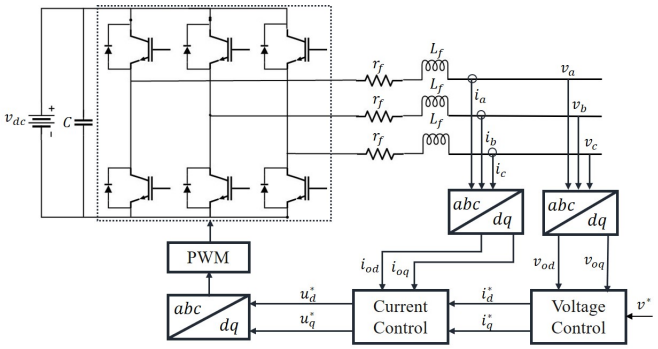


Fig. 1. Grid-forming converter with nested control loops.

A. Single grid-forming converter without droop control

In a nested controller, the output current feeds into the inner feedback loop while the output voltage is used in the outer feedback loop. In this case, the d-axis voltage reference is set to the nominal value or provided by the droop control loop, and the q-axis reference is set to zero. The equivalent circuit model of a grid-forming inverter interfaced with a limited dc source is shown in Fig. 2. Here, C is the dc-link capacitor, r_f and L_f represent the L-filter resistance and inductance, respectively, and ω_s is the nominal frequency.

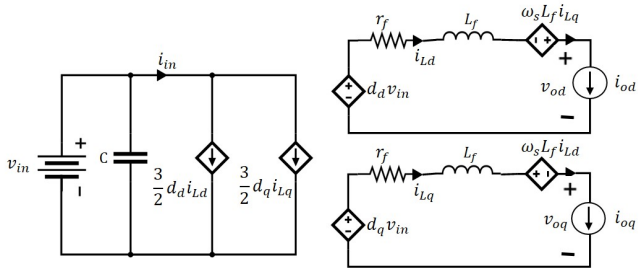


Fig. 2. Equivalent circuit model of grid-forming converter [19].

The small-signal state space model for the inverter, which will be used to analyze the impact of the controller on the input and output behavior of the inverter, is defined by the following set of transfer functions [19]:

$$\begin{bmatrix} v_{in} \\ i_o \end{bmatrix} = \begin{bmatrix} Z_{in} & T_{oi} & G_{ci} \\ G_{io} & Y_o & G_{co} \end{bmatrix} \cdot \begin{bmatrix} i_{in} \\ v_o \\ d \end{bmatrix} \tag{1}$$

where $Z_{in} = [Z_{in}]$ is the input impedance,
$T_{oi} = \begin{bmatrix} T_{oi\_d} & T_{oi\_q} \end{bmatrix}$ is the output to input (voltage) gain,

$G_{ci} = \begin{bmatrix} G_{ci\_d} & G_{ci\_q} \end{bmatrix}$ is the inner control loop gain,

$G_{io} = \begin{bmatrix} G_{io\_dd} & G_{io\_dq} \\ G_{io\_qd} & G_{io\_qq} \end{bmatrix}$ is the input to output (current) gain,

$Y_o = \begin{bmatrix} Y_{o\_dd} & Y_{o\_dq} \\ Y_{o\_qd} & Y_{o\_qq} \end{bmatrix}$ is the output admittance, and

$G_{co} = \begin{bmatrix} G_{co\_dd} & G_{co\_dq} \\ G_{co\_qd} & G_{co\_qq} \end{bmatrix}$ is the outer control loop gain.

In these functions, the input variables are dc current ($i_{in} = i_{dc}$), ac voltage ($v_o = [v_{od}\ v_{oq}]^T$), and duty cycle ($d = [d_d\ d_q]^T$). The output variables are dc voltage ($v_{in} = v_{dc}$) and ac current ($i_o = [i_{od}\ i_{oq}]^T$). Fig. 3 shows the small-signal representation for the nested-loop transfer functions when the grid voltage is regulated by the inverter and does not require droop control. The open-loop gain and impedance values of these transfer functions are calculated by setting the perturbations from the remaining inputs in the matrix to zero.

The outer control loop regulates the ac voltage as described by the following equations:

$$i_{od}^* = G_{v-PId}(v_d^* - v_{od}) \tag{2}$$

$$i_{oq}^* = G_{v-PIq}(v_q^* - v_{oq}) \tag{3}$$

where $G_{v-PI} = \begin{bmatrix} kv_p + \frac{kv_i}{s} & 0 \\ 0 & kv_p + \frac{kv_i}{s} \end{bmatrix}$ is the proportional-integral (PI) control gain for the outer control loop and $v^* = [v_d^*\ v_q^*]^T$ is the voltage reference with v_q^* set to zero.

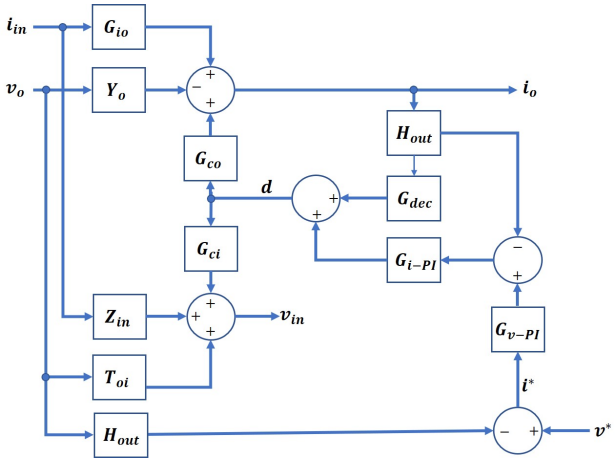


Fig. 3. Transfer function representation of input and output dynamics for nested-loop controller without droop.

The inner feedback loop uses current references from the outer feedback loop to control the PWM output as described by the following two equations:

$$u_{od}^* = G_{i-PId}(i_{od}^* - i_{od}) - \omega_s L i_{Lq} \tag{4}$$

$$u_{oq}^* = G_{i-PIq}(i_{oq}^* - i_{oq}) + \omega_s L i_{Ld} \tag{5}$$

where

$$G_{i-PI} = \begin{bmatrix} ki_p + \frac{ki_i}{s} & 0 \\ 0 & ki_p + \frac{ki_i}{s} \end{bmatrix}$$

is the PI control gain for the inner control loop and

$$G_{dec} = \begin{bmatrix} 0 & -\omega_s L_f \\ \omega_s L_f & 0 \end{bmatrix}$$

is the decoupling gain used to reduce the impact of cross-coupling caused by the output filter inductor (L_f is the filter inductance and $\omega_s = 2\pi f_s$ is the nominal frequency).

The ac (voltage and current) control delays are assumed to be the same and are calculated using the second order Padé approximation of the exponential function in the matrix:

$$H_{out} = \begin{bmatrix} e^{-0.5T_s s} & 0 \\ 0 & e^{-0.5T_s s} \end{bmatrix}.$$

From Fig. 3, the closed-loop input impedance and output admittance for a single grid-forming inverter with nested-loop controller can be derived as:

$$Z_{in\_c} = Z_{in} - G_{ci}(G_{dec} - G_{i-PI})H_{out}G_{io} \tag{6}$$

$$Y_{o\_c} = \frac{Y_o + G_{co}G_{i-PI}G_{v-PI}H_{out}}{I + G_{co}(G_{dec} - G_{i-PI})H_{out}} \tag{7}$$

On the other hand, a single-loop grid-forming converter has a single feedback loop to directly control the output voltage of the converter and does not use an inner current control loop. In this case, the control functions can be described by:

$$u_{od}^* = G_{v-PId}(v_d^* - v_{od}) \tag{8}$$

$$u_{oq}^* = G_{v-PIq}(v_q^* - v_{oq}) \tag{9}$$

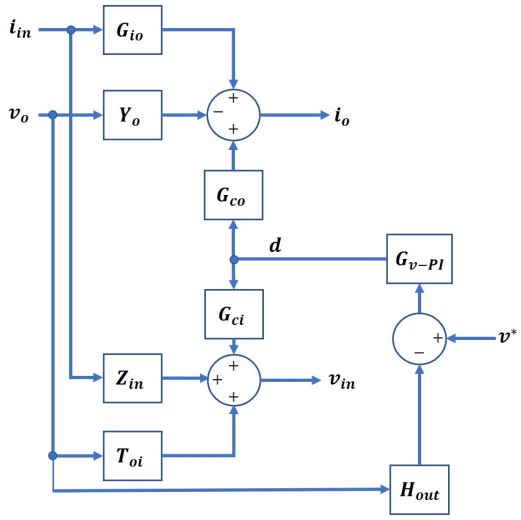


Fig. 4. Transfer function representation of input and output dynamics for single-loop controller without droop.

In the absence of a synchronization loop, the small-signal representation of the transfer functions of the single-loop grid-forming controller is shown in Fig. 4. From this model, the closed-loop input impedance and output admittance for a single grid-forming inverter with single-loop controller can be derived as:

$$Z_{in\_s} = Z_{in} \tag{10}$$

$$Y_{o\_s} = Y_o + G_{co}G_{v-PI}H_{out} \tag{11}$$

B. Parallel grid-forming converter with droop control

Droop control is ubiquitous in parallel operation of grid-forming inverters. Therefore, to study how synchronization control can alter the impact of the controller structure, the small signal model of both nested- and single-loop controllers is extended to include an outer loop with droop regulation [20]. More specifically, the active power-frequency and reactive power-voltage droop control method is incorporated into both models.

Fig. 5 shows the small-signal representation of the additional droop transfer functions along with the original model of the nested-loop controller, in which the droop control can be described as follows:

$$[\theta \; v^*]^T = G_{drp}(S_V i_o + S_I v_o) \tag{12}$$

where $G_{drp} = G_t G_m G_{lpf}$ is the droop gain,

$G_t = \begin{bmatrix} \frac{1}{s} & 0 \\ 0 & 1 \end{bmatrix}$ is the integral gain,

$G_m = \begin{bmatrix} m_p & 0 \\ 0 & m_q \end{bmatrix}$ is the droop coefficient matrix, and

$G_{lpf} = \begin{bmatrix} \frac{\omega_f}{s+\omega_f} & 0 \\ 0 & \frac{\omega_f}{s+\omega_f} \end{bmatrix}$ represents the low-pass filter for power measurements.

$S_V = \begin{bmatrix} V_d & V_q \\ V_q & -V_d \end{bmatrix}$ and $S_I = \begin{bmatrix} I_d & -I_q \\ I_q & I_d \end{bmatrix}$ are the steady-state values for d-q axis voltage and current measurements which are used to calculate the active and reactive power. In this paper, capitalized variable names indicate steady state values.

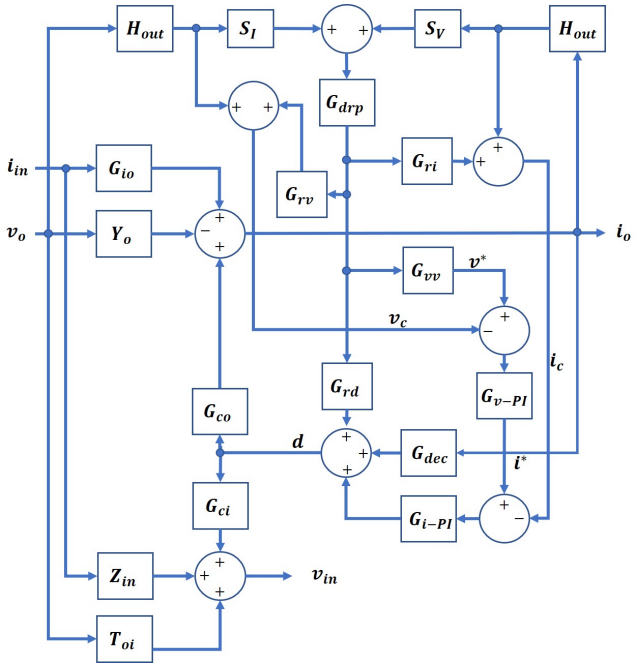


Fig. 5. Transfer function representation of input and output dynamics for nested-loop controller with droop.

In the case of parallel operation of grid-forming control, there exists a separation between the d-q axes of the grid and the converter. This shift from this synchronization-affected frame is included in the form of the following gains:

$G_{ri} = \begin{bmatrix} -I_q & 0 \\ 0 & I_d \end{bmatrix}$ for droop-affected d-q current,

$G_{rv} = \begin{bmatrix} -V_q^s & 0 \\ 0 & V_d \end{bmatrix}$ for droop-affected d-q voltage, and

$G_{rd} = \begin{bmatrix} -D_q & 0 \\ 0 & D_d \end{bmatrix}$ for droop-affected d-q duty cycle.

$G_{vv} = \begin{bmatrix} 0 & 1 \\ 0 & 0 \end{bmatrix}$ is the droop to voltage and frequency reference gain.

The closed-loop input impedance and output admittance for a nested-loop controller with droop regulation can then be derived from Fig. 5 as:

$$Z_{in\_cd} = Z_{in} - G_{ci}G_{dc}G_{io} \tag{13}$$

$$Y_{o\_cd} = \frac{Y_o + G_{co}G_{dv}}{I + G_{co}G_{dc}} \tag{14}$$

where

$G_{dc} = G_{rd}G_{drp}S_V H_{out} + (G_{dec} - G_{i-PI})G_{csi}$

$G_{dv} = G_{rd}G_{drp}S_I H_{out}$
$+ G_{i-PI}G_{v-PI}(G_{vv}G_{drp}S_I H_{out} - G_{csv})$

$G_{csv} = H_{out} + G_{rv}G_{drp}S_I H_{out}$

$G_{csi} = H_{out} + G_{ri}G_{drp}S_V H_{out}$

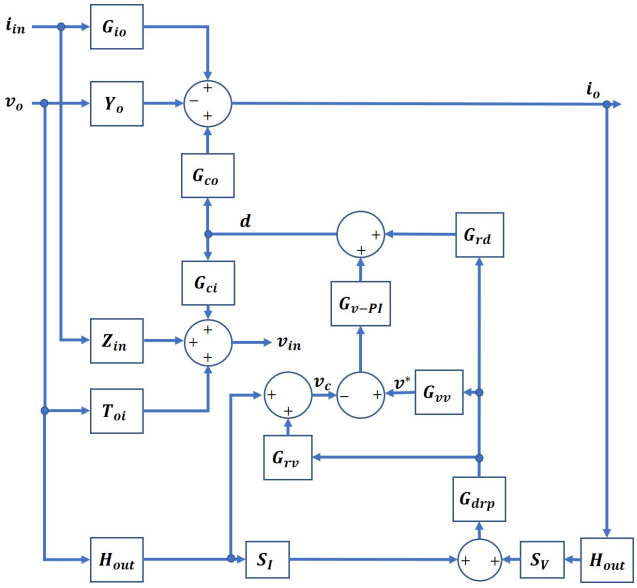


Fig. 6. Transfer function representation of input and output dynamics for single-loop controller with droop.

The closed-loop input impedance and output admittance for a single-loop controller with droop regulation can then be derived from Fig. 6 as:

$$Z_{in\_sd} = Z_{in} - G_{ci}G_{dcs}G_{io} \tag{15}$$

$$Y_{o\_sd} = \frac{Y_o + G_{co}G_{dvs}}{I + G_{co}G_{dcs}} \tag{16}$$

where

$G_{dcs} = G_{rd}G_{drp}S_V H_{out}$

$G_{dvs} = G_{rd}G_{drp}S_I H_{out} + G_{v-PI}(G_{vv}G_{drp}S_I H_{out} - G_{csv})$

III. Analytical Results

The transfer functions derived in the previous section were analyzed in Matlab using the converter and controller parameters shown in Table I. All the plots are wrapped within $\pm 180°$.

A. Single grid-forming converter without droop control

Fig. 7 presents the Bode plots for the input impedance of the single grid-forming inverter, with Zin_o being the open-loop input impedance, Zin_c being the closed-loop impedance for a converter with nested controls, and Zin_s being the closed-loop impedance for a converter with a single feedback loop. The open-loop input impedance is determined by the dc-link capacitor. In the absence of the ac current feedback loop, the single-loop controller has no impact on the input impedance.

The nested-loop controller with voltage and current feedback loops renders a capacitive effect on the dc impedance

TABLE I. Converter and Controller Parameters

Steady-state Converter Parameters	
Nominal ac voltage: V_{ac}	294 V (peak)
Nominal ac current: I_{od}, I_{oq}	26.7 A, 0 A
Nominal dc voltage: V_{dc}	400 V
Nominal dc current: I_{dc}	15 A
dc-link capacitor: C	5 mF
L-filter inductance: L_f	0.575 mH
L-filter resistance: r_f	0.2 Ω
Nominal frequency: f_s	60 Hz
Duty cycle: D_d, D_q	0.337, 0.059
Controller Gains	
Sampling period: T_s	100 μs
Switching frequency: ω_{sw}	10 kHz
Inner controller gains: ki_p, ki_i	0.105, 35
Outer controller gains: kv_p, kv_i	0.008, 40
Filter frequency: ω_f	1500 Hz
Droop coefficients: m_p, m_q	0.001, 0.001

at lower and higher frequencies but has a negative resistance effect around the controller bandwidth. As described in [21], this negative resistance behavior of dc/ac converters leads to dc voltage instability in upstream dc/dc converters because the converter decreases the voltage when current increases in trying to keep the load constant. Ref. [22] explains how tight closed-loop controllers exacerbate this phenomenon. However, the single closed-loop does not create the same negative resistance effect or the increased dc impedance at lower frequencies.

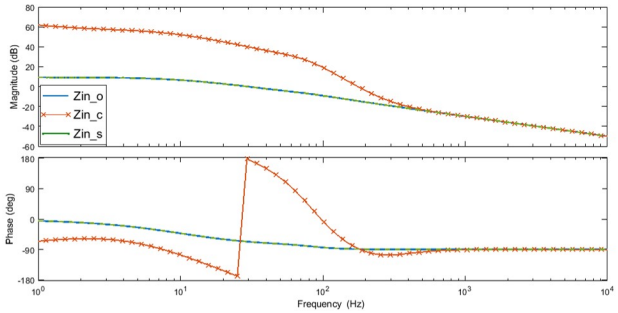


Fig. 7. Open loop and closed-loop Bode plots of converter input impedance.

Fig. 8 presents the inverter output admittance, with Yo_o being the open-loop admittance, Yo_c being the closed-loop admittance with nested control loops, and Yo_s being the closed-loop admittance with a single control loop. The open-loop admittance is determined by the filter inductor. The nested-loop control has an increasing negative admittance (reducing negative impedance) with increasing frequency and is non-passive at all frequencies. The closed-loop admittances along both axes lie in the negative resistance region around the controller bandwidth.

Nested-loop d-q coupling also increases at higher frequencies. The single-loop controller has higher positive admittance at lower frequencies which is passive. It reduces and becomes

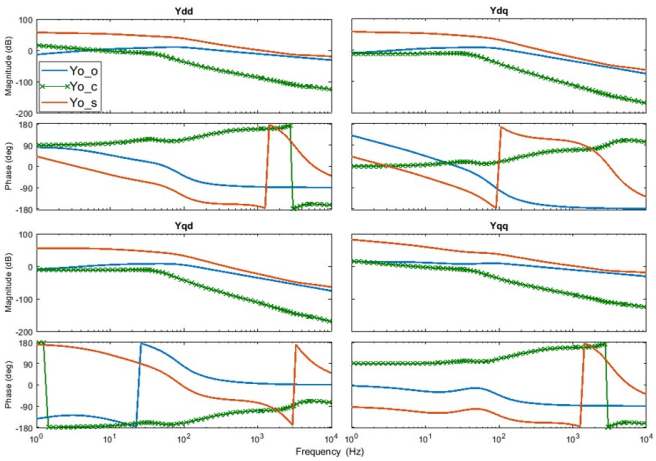


Fig. 8. Open loop and closed-loop Bode plots of converter output admittance.

non-passive in the control bandwidth region. These non-passive regions show that the control delay from the feedback loops reduces the system passivity even when the output filter is designed to be passive. The control delay from the single feedback loop impacts the higher frequency region while the control delays from the double feedback loops affect the lower frequency region. This non-passivity can lead to unstable system oscillations under weak grid conditions [23].

B. Parallel grid-forming converter with droop control

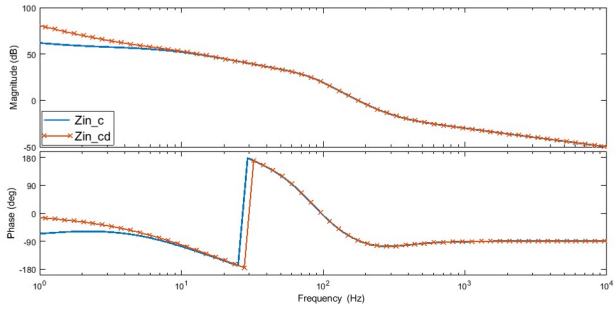


Fig. 9. Bode plots comparing converter input impedance for nested-loop controller with and without droop.

From the input impedance results for nested-loop controller in Fig. 9, it is clear that the outer droop loop only has an impact at lower frequencies, closer to the droop control loop bandwidth. The droop control loop increases the input impedance at lower frequencies but does not reduce the negative resistance behavior of the nested-loop controller. The results in Fig. 10 show that droop control has little to no impact on the output admittance, especially for the d-d and q-q axes.

Fig. 11 shows that the droop control loop only has an impact at the lower frequencies for the single-loop controller, rendering an overall capacitive effect while increasing the input impedance. Fig. 12 shows that droop control has a more significant impact on the output admittance, making it more

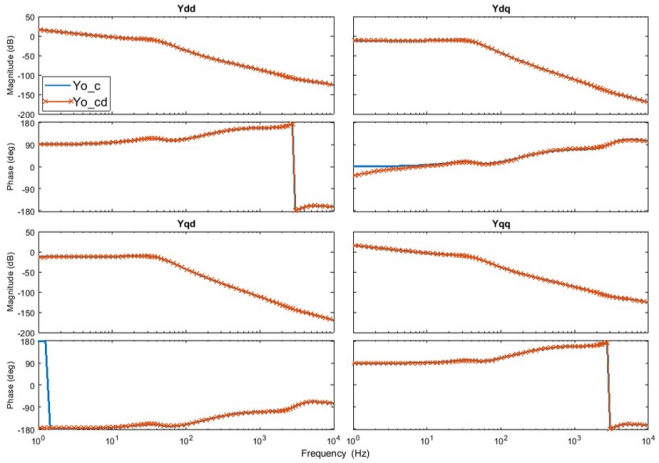


Fig. 10. Bode plots comparing converter output admittance nested-loop controller with and without droop.

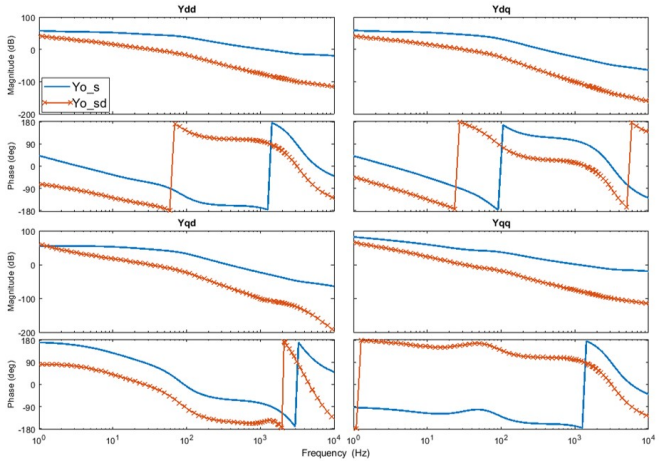


Fig. 12. Bode plots comparing converter output admittance single-loop controller with and without droop.

negative and non-passive. The power measurements used in droop control also increases coupling between the d- and q-axes at lower frequencies.

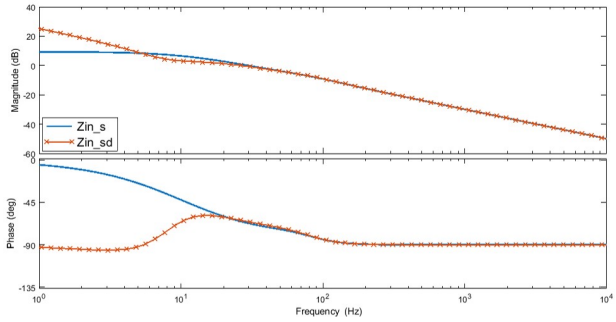


Fig. 11. Bode plots comparing converter input impedance for single-loop controller with and without droop.

Although the passivity-reducing effect of current control has been previously studied in grid-connected inverters [24], this analysis demonstrates similar behavior for grid-forming inverters as well. It is clear from both cases with and without droop control that using the current feedback loop significantly reduces the passivity of the system and can be detrimental to the system stability in inverter-dominated weak grids.

IV. Simulation and Experimental Verification

A single grid-forming inverter is simulated in MATLAB/Simulink using both single- and nested-loop controllers with an average model-based voltage source converter, connected to an impedance load. The system and control parameters used for the simulation are the same as those used in the baseline analysis (Table I). The dc-link voltage is measured during a step load change from 5 kW to 7 kW at 1 s, and shown in Fig. 13.

These results show that for the same change in load, the dc-link voltage for the nested-loop controller experiences a larger drop after the load change than the single-loop controller. This

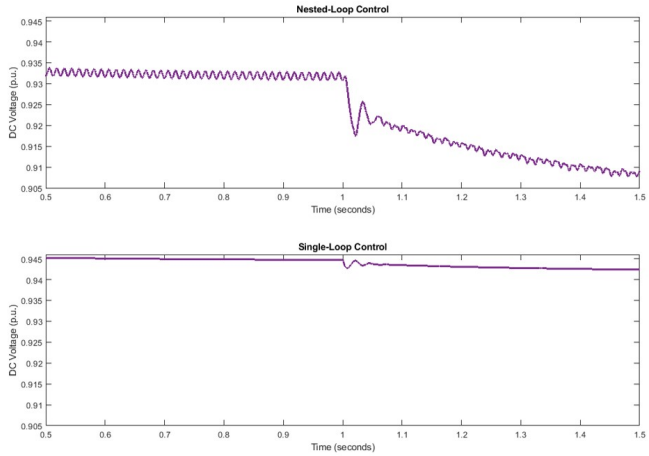


Fig. 13. DC-link voltages for nested- and single-loop controllers during step load change.

indicates that the dc-link behind the nested-loop controller is more susceptible to disturbances as a result of changing load or grid conditions.

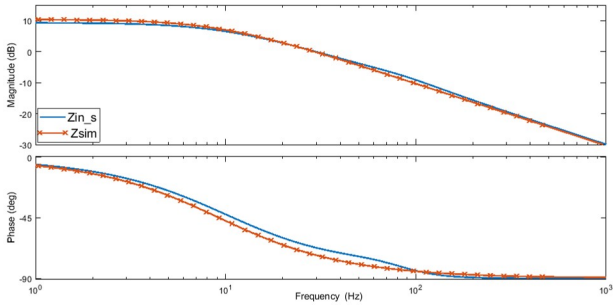
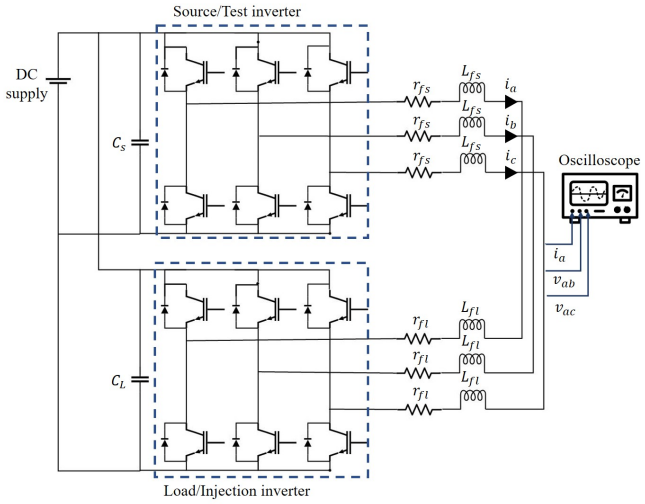


Fig. 14. Bode plots of closed-loop input impedance from analytical model and simulation measurements.

The input impedance for the single-loop controller is also measured using Simulink's Impedance Measurement function

and compared with the analytical results. Fig. 14 shows that the analytical and simulation results match very well.

Experimental tests are performed to validate the analysis results for a single-loop controller with a single grid-forming inverter. A small-signal voltage injection method is used to measure the closed-loop output impedance of a grid-forming converter with single-loop control in the CURENT hardware testbed [25], [26], shown in Fig. 15b. In Fig. 15a, the top converter is the grid-forming (source) inverter being tested while the bottom converter serves as the current-controlled load which also injects high-frequency voltage perturbations. The two identical converters have common dc and ac sides (by nature of the testbed design), as well as the same L-filters on the ac side. The ac currents and voltages are measured using an oscilloscope. To match the testbed hardware settings, the single-loop analysis results in this section are derived using the values in Table II.



(a)

(b)

Fig. 15. Experimental setup for inverter impedance measurement: (a) Experimental setup schematic (b) CURENT Hardware Testbed converter cabinet with inverters and filters.

To solve the 2-by-2 matrix of the output ac admittance in the d-q axes, two sets of d-q voltage and current measurements (v_d, v_q and i_d, i_q) are used as shown in (17) [27]. One set of measurements is acquired for high-frequency injections in the d-axis voltage, and the second set is from high-frequency injections in the q-axis voltage. To reduce the number of measurements as well as data processing, the primary phase (A) is aligned along the d-axis to obtain v_d and i_d measurements, and then along the q-axis to obtain v_q and i_q measurements for each set of injections. This eliminates the need for sensing the other phases and using Park transformations.

$$\begin{bmatrix} Y_{odd} & Y_{odq} \\ Y_{oqd} & Y_{oqq} \end{bmatrix} = \begin{bmatrix} i_{d1} & i_{d2} \\ i_{q1} & i_{q2} \end{bmatrix} \begin{bmatrix} v_{d1} & v_{d2} \\ v_{q1} & v_{q2} \end{bmatrix}^{-1} \tag{17}$$

TABLE II. Experimental Setup Parameters

Nominal ac voltage: V_{ac}	40 V (peak)
Nominal ac current: I_{od}, I_{oq}	27.44 A, 0 A
Nominal dc voltage: V_{dc}	100 V
Nominal dc current: I_{dc}	13.9 A
dc-link capacitor: C	500 mF
L-filter inductance: L_f	0.575 mH
L-filter resistance: r_f	0.2 Ω

The measurements collected from the oscilloscope are processed through a Fast Fourier Transform in Matlab to obtain the complex admittance values for the range of injected frequencies (100 to 2000 Hz in intervals of 50 Hz). These values are then used to estimate the transfer functions of the measured output admittance matrix, and to draw the Bode plots for comparison.

The results shown in Fig. 16 depict the measured impedance as Y_meas and the analytically derived impedance as Yo_s. The phase values are wrapped between $-180°$ and $+180°$ to show and compare the results more clearly. The results from the experimental measurement match the analytical values very well.

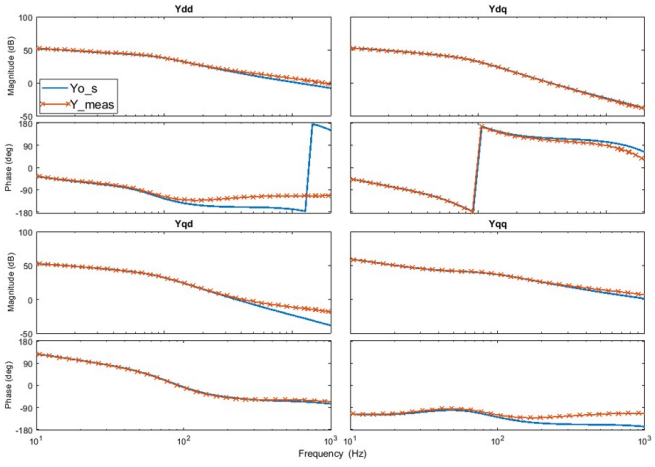


Fig. 16. Bode plots of closed-loop output admittance from the analytical model and experimental measurements.

V. Conclusion

Small-signal impedance analysis is used in this paper to compare the behavior of multiple feedback loops to a single feedback loop in a grid-forming converter controller. Small-signal models are derived for each type of controller to analyze the closed-loop input impedance and output admittance of the converter. The analytical results are also verified using simulation and hardware measurements.

This study demonstrates the existence of negative resistance behavior in both the input impedance and output admittance of the commonly-used cascaded-loop controller in grid-forming inverters. The negative resistance behavior on the input side can lead to dc-link voltage instability, and the non-passive output admittance can jeopardize the ac system stability under weak grid conditions. While the single-loop controller does not impact the dc impedance, the control delay inevitably creates a non-passive region in the output admittance. The addition of the droop control loop does not exacerbate or alleviate the issues caused by the nested-loop controller, but it does make the single-loop output admittance less passive.

Hence, even though inner current control loops are suitable for grid-following inverters and useful in current limiting during transients, their feedback loop ultimately weakens both the dc and ac side stability for grid-forming applications. Ultimately, eliminating the inner current control loop can improve dc-link stability and increase ac output passivity while also enhancing the speed of the controller response.

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