A Closed-Loop Modulation Scheme for Duty Cycle Compensation of PWM Voltage Distortion at High Switching Frequency Inverter

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***Abstract*—Wide bandgap semiconductors with fast switching speed capability are becoming an enabler to achieve the higher power density design. However, the further increase of switching frequency cannot continuously improve the power quality of ac-side waveforms in dc–ac/ac–dc application. The main reason is the distortion of pulsewidth modulation (PWM) voltage at switching point under high switching frequency. In general, there are two contributors causing PWM voltage distortions in bridge-based topologies. One is the deadtime, which occupies higher ratio in the small duty cycle case under high switching frequency and induces the voltage errors. The other one is the turn-OFF transient in the small load current or around the zero-crossing point of the ac-side current, because the relatively slow rising slope of the drain–source voltage will affect the right duty cycle. To solve this issue, this paper proposes a closed-loop modulation scheme to compensate the duty cycle distortion of PWM voltage based on one-cycle control or charge control. Compared to the traditional feedforward type of compensation, the proposed scheme does not need online calculation and instantaneous inductor current sampling, and it shows potential to be a general scheme for variety of topologies and modulations. Simulations and experiments are carried out on a 400-kHz single-phase full-bridge inverter with 400-Hz fundamental frequency to demonstrate the performance of the proposed approach.**

***Index Terms*—Closed-loop modulation, duty cycle distortion, high switching frequency, one-cycle control (OCC) or charge control, power quality.**

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I. Introduction

EMERGING from the latest generation of wide bandgap semiconductors, the Gallium Nitride (GaN) heterojunction field-effect transistor is a highly promising device for achieving high power density. The switching frequency in a single-phase hard-switching inverter with the power rating from 1 to 3 kW are boosted to 200–500 kHz [1]–[3] by adopting GaN HEMTs, compared to 10–100 kHz with Si devices. Nonetheless, in the meantime, the design of high switching frequency converter imposes several new challenges. One of known challenges in high switching frequency ac–dc/dc–ac converters is the power quality of ac-side waveforms. For voltage-source inverters or rectifiers, the power quality of ac-side waveforms is directly related with pulsewidth modulation (PWM) voltage at switching terminals. Indeed, the essence of PWM voltage distortion is the duty cycle difference between the ideal duty cycle from the controller and the actual duty cycle of PWM voltage, which is mainly caused by the deadtime and slow turn-OFF transient under low load current conditions [4].

Initial research work on duty cycle compensation was summarized in textbook [5], which mainly focused on the deadtime compensation in dc-fed motor drive application. Two common applied schemes were given in [5], and they are output closed-loop control and deadtime feedforward control based on the current direction, and most follow-on compensation research was based on these two basic approaches for different topologies and applications. However, two approaches were developed for low switching frequency application, and both have limitations and difficulties to implement at high switching frequency converters.

The first approach directly depends on the closed-loop control design of the output waveform. Since PWM voltage distortions caused by duty cycle loss can be reflected as third, fifth, seventh, and even higher order harmonics of ac-side waveforms, authors in [6] and [7] attempted to regulate induced harmonics

by the feedback controller. However, those methods demand a high control bandwidth and control gain under these specific harmonics especially for a 400-Hz ac system in the airplane and must be achieved through a superfast digital controller with enough low computation delay. Therefore, the feedback control compensation schemes are more applicable when the switching frequency and the fundamental frequency are relatively low, e.g., several kilohertz for switching frequency and 60 Hz for fundamental frequency. Considering the limited main frequency and computation speed of popular digital signal processors (DSP) controllers in power electronics applications, it is more practical to choose feedforward-type compensation schemes.

There is a lot of research work based on the second approach focusing on feedforward-type duty cycle compensation [8]–[13]. Authors in [8]–[12] concentrated on duty cycle compensation in voltage-fed motor drives or on the overlap effect in current-fed rectifiers [13]. The basic idea for duty cycle compensation in these papers is to treat deadtime distortion as a voltage error depending on the amplitude and polarity of load current; however, only dead-time-oriented duty cycle error is considered in their scheme rather than both the deadtime and the turn-OFF transient under small load current. Li *et al.* [14] further derived equations of voltage loss caused both by the deadtime and the turn-OFF transient in a single-phase full bridge inverter. Zhang and Xu [15] took snubber circuits effects into consideration on the deadtime compensation in the motor drive application, and the deadtime is compensated based on the voltage differences between the actual PWM voltage and ideal voltage. However, all these compensation methods need online calculation and the sampling of the instantaneous inductor current or the switching point voltage, which is not realistic for a hundred kilohertz converter design.

Other than the deadtime compensation, authors in [4] and [16] addressed the PWM voltage distortion caused by the nonlinear output capacitance of devices in Vienna-type topology. Hartmann *et al.* [16] mitigated the input current distortion caused by the long turn-OFF delay time owing to the particularly nonlinear output capacitance of Si super junction MOSFET. Liu *et al.* [4] pointed out that the slow slope of falling edge of switching point voltage also introduces PWM voltage distortion especially for Vienna-type topology, whose commutation loop involves multiple devices including the diode bridge and active devices. Both of their methods can get rid of the instantaneous sampling of inductor current or switching voltage, but they are only suitable for the specific topology, modulation schemes, operation conditions (PF $= 1$), or devices. Once these factors change, the equations of feedforward duty cycle compensation have to be rederived.

Literature [17]–[20] developed and implemented closed-loop PWM or PWM feedback loop in class D power amplifier in audio systems to improve power supply rejection (PSR) and total harmonic distortion (THD). An analog PWM negative feedback loop including switching node voltage sampling and a first-order or second-order compensator is employed and designed to correct output voltage error, which can achieve a good PSR capability and very low THD as low as 0.003%. However, the design of compensators in PWM feedback loop at class D amplifier is more like a traditional proportional integral (PI) or proportional differential (PD) controller design, whose compensation capability of harmonics mainly depends on the bandwidth and gain of the compensator. Like other closed-loop control schemes, the compensator needs to be designed with a high bandwidth and enough control gain at high-order harmonics frequencies, and this can be easily implemented in class D amplifier since it has a low radiated and conducted noise because of adopting of low-voltage-rating power semiconductors with nearly ideal switching and low parasitics. Nonetheless, it is not the case in the relatively high-voltage (e.g., 650-V rating) and high-power inverters. High-bandwidth compensator will induce the stability and noise immunity issue for relatively high-power and high-voltage converters.

In this paper, a closed-loop modulation scheme based on one-cycle control (OCC) or charge control [21], [22] is proposed for mitigating the PWM voltage distortion. The proposed scheme does not require instantaneous inductor current feedback and can be regarded as a separate control loop, which is independent of the original converter control loops (voltage/current loop), control strategies, and modulations. Instead, the proposed scheme applies the OCC/charge control onto the modulator to correct the duty cycle so that the PWM voltage distortion introduced by deadtime and slow switching transition can be compensated, and the actual duty cycle of PWM voltage will automatically track the ideal reference duty cycle from the controller.

Some modified OCC schemes [23]–[27] reconstructed the reference signals of OCC control such as adding an additional control loop [23]–[25] (e.g., voltage control loop with PI controller) or other feedback signals [26], [27] (phase current, neutral point voltage) to improve the control performance (e.g., dc-link voltage ripple, output current harmonics) or to add new control capability (e.g., neutral voltage balance). However, they are still designed for relatively low switching frequency and were also not designed to target the distortion issue due to deadtime and slow switching transition or for duty cycle compensation purpose. In comparison, the circuit design for OCC has been improved in this paper to adapt to duty cycle compensation at high-frequency application up to 400 kHz. The size of the implemented circuits for the proposed closed-loop modulation is also small enough to be integrated into the gate driver board with relatively low cost and tiny space, and it also has a potential to be applied in different topologies, devices, and even different modulation schemes to compensate the duty cycle error of PWM voltage.

This paper is structured as follows. Section II briefly introduces the distortion mechanism of PWM voltage caused by the deadtime and the slow turn-OFF transient. The principle of the proposed closed-loop modulation scheme is given in Section III, and the necessary modifications to the traditional charge control and related issues are presented. Section IV shows the implementation of the proposed closed-loop modulation scheme based on the analysis in Section III. The time delay of logic circuits is a key factor on the accuracy of the proposed scheme. In Section V, experimental waveforms obtained from a single-phase inverter with 400-Hz fundamental frequency and 400-kHz switching frequency are provided to verify the analysis and the proposed control scheme. Finally, Section VI concludes this paper.

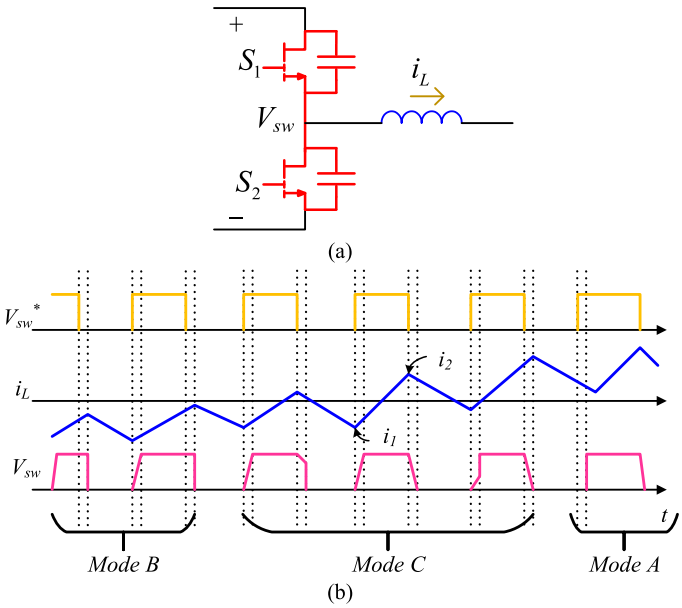


Fig. 1. Basic configuration block in a bridge-based voltage-source inverter or rectifier and its key waveforms. (a) Half-bridge configuration. (b) Key waveforms and three modes.

II. Duty Cycle Distortion Mechanism of PWM Voltage

For a bridge-based voltage-source inverter or rectifier, the basic configuration block is shown in Fig. 1(a), which is a typical half bridge with an ac inductor. Fig. 1(b) shows the key waveforms around the zero-crossing point of the inductor current. In Fig. 1(b), $V_{\rm sw}^*$ is the ideal duty cycle produced by the controller, which is also the reference duty cycle of PWM voltage at the switching point. However, the real output duty cycle of PWM voltage $V_{\rm sw}$ shown in Fig. 1(b) is much different from ideal one due to the existence of the deadtime and the turn-OFF transients. Based on the understanding of the circuit operation, the PWM voltage distortion in half bridge can be classified into three categories by judging the polarity of the ac inductor current.

Mode A) Inductor current is positive. The active switch is S_1 operating in hard switching, and the synchronous switch is S_2 operating under zero voltage switching (ZVS) condition. In this mode, the rising edge of PWM voltage is decided by the turn-ON transient of active switch S_1 while the falling edge of PWM voltage is decided by the turn-OFF transient of active switch S_1. Specifically, the turn-ON speed is only determined by gate driver for GaN HEMT [28]; thus, the rising edge of PWM voltage is generally steep and has no contribution to the voltage error of PWM voltage. However, before S_1 turn-ON, S_2 is continuously ON during the deadtime through behavior-like body diode which forces PWM voltage to zero volts and introduces voltage loss compared to the ideal case. For falling edge of PWM voltage, it is determined by turn-OFF speed of active switch S_1. Since turn-OFF speed is decided by the load current around zero crossing or low load current condition [23], the nonideal switch action of S_1 also induces the extra voltage error during turn-OFF transient.

Mode B) Inductor current is negative. Contrary to Mode A, the active switch is changed to S_2, and the synchronous switch is S_1. In this mode, the rising edge of PWM voltage is decided by the turn-OFF transient of active switch S_2 while the falling edge of PWM voltage is decided by the turn-ON transient of active switch S_2. Similar to the analysis in Mode A, the rising edge voltage distortion is caused both by the turn-OFF transient of active switch S_2 and the deadtime, while the falling edge voltage distortion is induced only by the deadtime.

Mode C) Inductor current has multiple zero crossings in one switching cycle, and the rising edge and the falling edge of PWM voltage align to the different polarities of the inductor current. For this particular case, both two edges of PWM voltage are affected by the turn-OFF transients and the deadtime. Apart from the deadtime, the edge aligning to positive current is affected by the turn-OFF transient of switch S_1, and the edge aligning to negative current is affected by the turn-OFF transient of switch S_2.

TABLE I
Symbols for Deriving the Duty Cycle Distortion

Symbol	Physical significance
t_r	Rising time of PWM voltage at switching point
t_f	Falling time of PWM voltage at the switching point
T_d	Dead time
V_e	Voltage error caused by duty cycle distortion
C_{oss}	Charge-based equivalent output capacitance
V_{sw}	PWM voltage at the switching point
V_{sw}^*	PWM voltage formed by the ideal duty cycle information from the controller
i_f	The instantaneous inductor current at the start moment of falling edge of PWM voltage
i_r	The instantaneous inductor current at the start moment of rising edge of PWM voltage
V_{dc}	Dc bus voltage
T_s	Switching period of the device

Before going to the detailed derivation of duty cycle loss, Table I gives all the variables used in the following quantitative analysis. The rising time t_r of PWM voltage under Mode A is derived as

$$t_r = \frac{2C_{oss}V_{\rm dc}}{|i_r|}. \tag{1}$$

The falling time t_f of PWM voltage under Mode B is

$$t_f = \frac{2C_{oss}V_{\rm dc}}{|i_f|}. \tag{2}$$

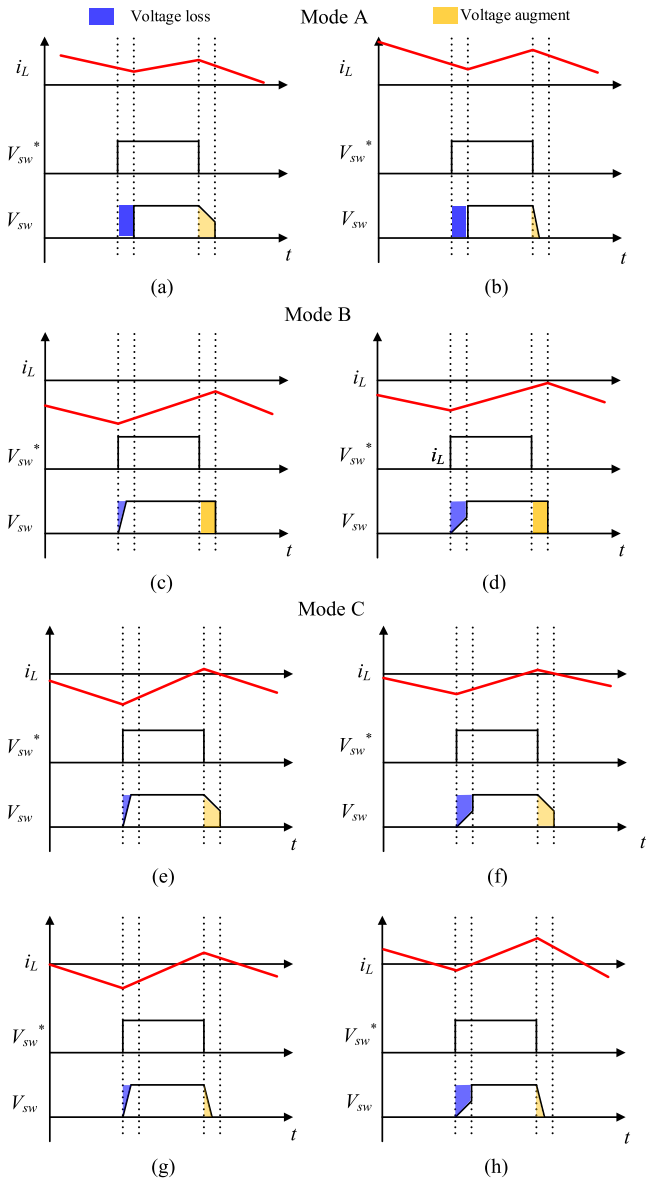


Fig. 2. All possible cases for duty cycle distortion of PWM voltage.

On account of the above analysis, all possible duty cycle distortion cases of PWM voltage are shown in Fig. 2. Each mode is further subdivided into several cases depending on the longest duration time among t_r, t_f, and T_d. In Fig. 2, the blue shadow area is the voltage loss of PWM voltage at the switching point, and the yellow shadow area is the voltage augment of the PWM voltage at the switching point. Hence, the voltage errors for each case can be derived by calculating the area of the shadow region. Here gives one calculation example for Fig. 2(a) in Mode A.

For the blue shadow area, the voltage loss caused by the deadtime can be derived from the rectangle shape and it is obtained as

$$v_{e\_\mathrm{loss}} = \frac{V_{\mathrm{dc}} T_d}{T_s}. \tag{3}$$

TABLE II
EXPRESSION OF VOLTAGE ERROR UNDER DIFFERENT MODES

Mode A	**Case a**	$v_e = -\dfrac{T_d^2 i_f}{4C_{oss}T_s}$
	Case b	$v_e = \dfrac{V_{dc}t_f}{2T_s} - \dfrac{V_{dc}T_d}{T_s}$
Mode B	Case c	$v_e = -\dfrac{V_{dc}t_r}{2T_s} + \dfrac{V_{dc}T_d}{T_s}$
	Case d	$v_e = -\dfrac{T_d^2 i_r}{4C_{oss}T_s}$
Mode C	Case e	$v_e = -\dfrac{T_d^2 i_r}{4C_{oss}T_s} - \dfrac{V_{dc}t_r}{2T_s} + \dfrac{V_{dc}T_d}{T_s}$
	Case f	$v_e = \dfrac{T_d^2 (i_r - i_f)}{4C_{oss}T_s}$
	Case g	$v_e = \dfrac{V_{dc}t_f - V_{dc}t_r}{2T_s}$
	Case h	$v_e = \dfrac{V_{dc}t_f}{2T_s} - \dfrac{V_{dc}T_d}{T_s} + \dfrac{T_d^2 i_r}{4C_{oss}T_s}$

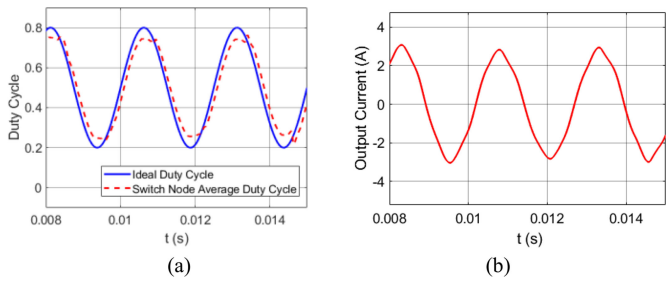


Fig. 3. PWM voltage distortion illustration. (a) Ideal duty cycle versus real PWM voltage duty cycle. (b) Output ac current.

The voltage augments in Fig. 2(a) caused by the turn-OFF transient is calculated from the trapezoid shape and it is derived as

$$v_{e\_\mathrm{aug}} = \frac{[V_{\mathrm{dc}} + (V_{\mathrm{dc}} - T_d i_f / 2C_{oss})]T_d}{2 \cdot T_s}. \tag{4}$$

Combining (3) and (4), the total duty cycle distortion of PWM voltage is characterized from the sum of the two terms

$$v_e = v_{e\_\mathrm{aug}} - v_{e\_\mathrm{loss}} = -\frac{T_d^2 i_f}{4C_{oss}T_s}. \tag{5}$$

Similarly, the PWM voltage distortions under all other cases are obtained, as given in Table II. Simulation in a single-phase voltage-source inverter when considering C_{oss} and T_d is also conducted to verify the PWM voltage distortion. Fig. 3(a) gives the difference between the ideal duty cycle of the controller and the filtered actual PWM voltage duty cycle. It demonstrates that

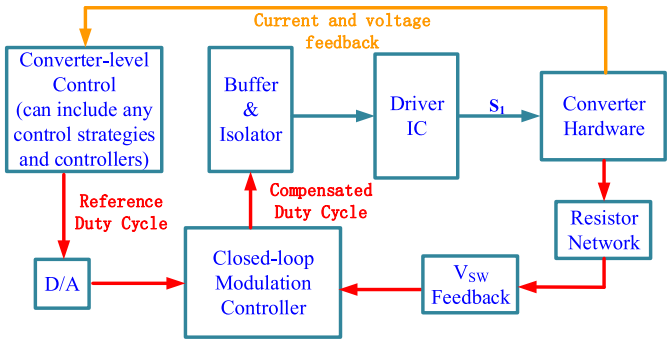


Fig. 4. Proposed duty cycle compensation scheme with a closed-loop modulation controller.

the actual PWM voltage duty cycle cannot track the ideal duty cycle from the controller if there is no compensation scheme. In addition, based on the compensation expression of the PWM voltage error in Table II, both instantaneous samplings of the inductor current and dc-bus voltage are required for the on-line calculation of the compensation terms. This feedforward compensation increases the design complexity of the controller and computation burden of the control software for a hundreds kilohertz inverter. In order to avoid instantaneous inductor current sampling, a charge control-based closed-loop modulation is proposed in this paper.

III. Principle of Modulation Closed-Loop Scheme

A. Compensation Principle Based on Charge Control

The traditional feedforward compensation scheme is a case study under one specific topology combined with a fixed modulation and specific devices. The general way to realize compensation for all potential applications should be a feedback control. However, the feedback control has two major barriers to overcome. First, it is very difficult to sample and feedback the high switching frequency PWM voltage, especially for the rising and falling edges of PWM voltage. Second, it requires a high-bandwidth controller to provide enough control gain under equivalent harmonics.

To avoid these issues in feedback control, a closed-loop modulation-based compensation scheme is proposed and shown in Fig. 4. For this proposed scheme, the duty cycle will not be directly given by the converter controller but from the closed-loop modulation controller. The converter controller is only responsible for producing the reference duty cycle with any control strategies and modulation schemes. In addition, the reference duty cycle does not need to be discretized through the PWM module in the DSP controller, whereas it is a continuous signal in the time-domain output by a built-in D/A in DSP. For example, for space vector modulation, the reference duty cycle is saddle shaped, while for sinusoidal PWM (SPWM), the reference duty cycle is the sinusoidal shape with a dc bias. The discretization is achieved by closed-loop modulation controller with PWM voltage feedback. The goal of the proposed compensation scheme is let the actual duty cycle of PWM voltage track the reference duty cycle output by converter controllers, and it is independent of converter control. Hence, any control methods, strategies, or modulations can be utilized to improve converter-level control performance.

To track the reference duty cycle, the basic idea is to adopt charge control to obtain the average voltage of the scaled PWM voltage in one switching cycle, and this average voltage can be treated as an equivalent duty cycle of the actual PWM voltage. Then, let the equivalent duty cycle of PWM voltage $D_{\rm eq}$ equal to the reference duty cycle $D_{\rm ref}$. As a result, all the PWM voltage distortion will be compensated.

The following gives the mathematical illustration for the proposed scheme. Assuming bipolar SPWM is used for a single-phase full-bridge inverter, $D_{\rm ref}$ under the rated input voltage is written as

$$D_{\rm ref} = 0.5 + m\sin\omega t \text{ where } 0 \le m \le 0.5 \tag{6}$$

where m is modulation index, and ω is the angular frequency of the ac fundamental voltage.

Generally, $D_{\rm ref}$ represents the final output of any control strategies and structures with dc bias injection. Since the real duty cycle of the switch cannot be a negative value, a dc bias 0.5 needs to be added in (6) for the correct duty cycle reference of a full-bridge inverter.

Also, assuming the sampled $V_{\rm sw}$ is scaled down by the rated input voltage $V_{\rm input\_rated}$, which means that the steady-state voltage of the sampled $V_{\rm sw}$ is 1 V at the rated input voltage case, so the equivalent duty cycle can be derived as

$$D_{\rm eq} = \frac{\int_0^{T_s} v_{\rm sw}(t)/V_{\rm input\_rated}\,dt}{T_s}. \tag{7}$$

To make $D_{\rm eq}$ equal $D_{\rm ref}$ in one switching cycle, charge control becomes the perfect choice. A mixed signal implementation utilizing both analog circuits and digital control is proposed in Fig. 5(a), where $D_{\rm eq}$ is obtained by a resettable op-amp-based integrator and the reference duty cycle $D_{\rm ref}$ is output by a DSP controller with a built-in D/A with a scaling ratio. As shown in Fig. 5(a), a resistor sampling network is connected to the switching point (the midpoint of one switching bridge), then the sampling voltage of the resistor divider is sent to an analog integrator, so the charging path includes the resistor sampling network and the analog integrator.

It is clear that the same scaling ratio should be designed for $V_{\rm sw}$ normalization through the resistance voltage divider to properly produce the final $D_{\rm comp}$ at the rated input voltage. One issue in setting up $D_{\rm ref}$ is how to scale the reference output under nonrated dc input voltage since the sensing ratio of $V_{\rm sw}$ is a fixed value only designed for the rated dc bus voltage $V_{\rm input\_rated}$. When the bus voltage changes, the normalized $V_{\rm sw}$ will not be 1 V, leading to different scaling ratios between the analog path and the digital path, which $V_{\rm sw}$ does not have the same scaling ratio with $D_{\rm ref}$.

To match the scaling ratio of $V_{\rm sw}$ under different input voltages, $D_{\rm ref}$ should be scaled under different input voltages before it is output by D/A port. Assuming the $D_{\rm ref\_rated}$ is the output amplitude under the rated input voltage and m in (6) is decided

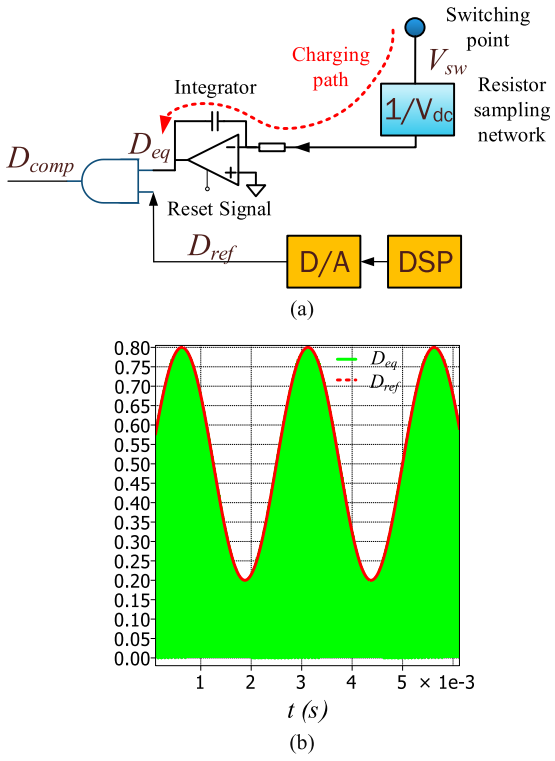


Fig. 5. Charge-control-based compensation and its key waveforms. (a) Integrator to obtain $D_{\rm eq}$. (b) Key waveforms.

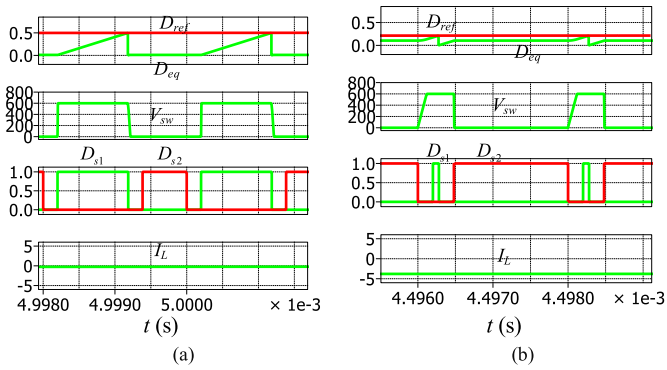


Fig. 6. Zoom-in simulation waveform of charge control. (a) Mode C compensation. (b) Mode B compensation.

by the output voltage control, the corrected $D_{\rm ref}$ under other input voltage $v_{\rm in}$ is given in

$$D_{\rm ref} = \frac{D_{\rm ref\_rated} v_{\rm in}}{V_{\rm input\_rated}} = \frac{0.5 + m \sin \omega t}{V_{\rm input\_rated}} v_{\rm in} \tag{8}$$

where $V_{\rm input\_rated}$ is the rated input voltage.

The simulation waveforms of $D_{\rm eq}$ and $D_{\rm ref}$ from MATLAB are shown in Fig. 5(b). The red envelope curve is the reference duty cycle and the green shadow area is the output voltage of integrator. From Fig. 5(b), it is evident that $D_{\rm eq}$ can track $D_{\rm ref}$ with charge control.

Fig. 6 further gives the zoom-in simulation waveforms under different PWM voltage distortion cases. According to these waveforms, the closed-loop modulation can guarantee that $D_{\rm eq}$ always equal $D_{\rm ref}$ at one switching cycle under different

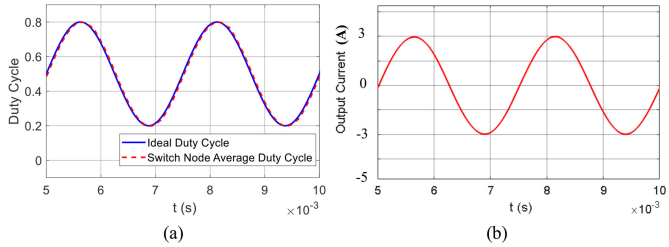


Fig. 7. Simulation waveform after compensation. (a) Ideal duty cycle versus real PWM voltage duty cycle. (b) Output ac current.

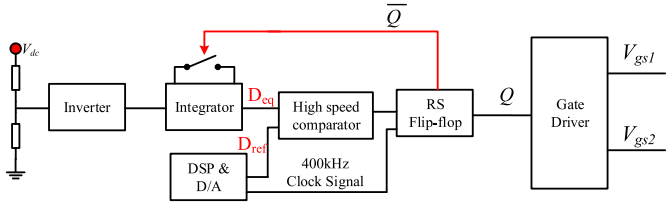


Fig. 8. Original modulation closed-loop scheme.

distortion cases. Fig. 7(a) demonstrates that the equivalent duty cycle of PWM voltage equals to reference duty cycle after compensation, and compared to Fig. 3(b), the output current at ac side in Fig. 7(b) becomes much less distorted.

B. Modifications to Charge Control to Improve the Accuracy of Compensation

In the previous section, the principle of closed-loop modulation has been analyzed and a concept-proof simulation has been conducted in MATLAB with the program-based charge control. However, the circuits-based charge control may not achieve the same perfect performance as the program-based charge control. To further verify the practical feasibility and understand the potential challenge of this scheme, a circuit-model-based closed-loop modulation as shown in Fig. 8 is implemented in SABER.

The simulation adopts the same main circuit parameters as the hardware prototype of a single-phase full-bridge inverter with 400-kHz switching frequency and 400-Hz fundamental frequency. The deadtime is set to 200 ns and junction capacitance of each device is set as 284 pF based on the charge-based equivalent output capacitance from the datasheet. The closed-loop modulation scheme is equipped with switch S_1 in Fig. 1(a). From the simulation, three issues are observed and discussed, respectively.

1) Reset Time of the Integrator: The first issue is related to the reset signal of the integrator. Since the duration time of the reset signal of the conventional charge control covers the entire OFF-state time of switch S_1, PWM voltage will not be integrated during this turn-OFF region and the following deadtime. As a result, the closed-loop modulation only compensates the rising edge of the PWM voltage corresponding to Mode B rather than both of two edges, causing compensation errors. One of the possible schemes is to equip the closed-loop modulation circuits to switch S_2 as well and enable its function on Mode A. Then, two

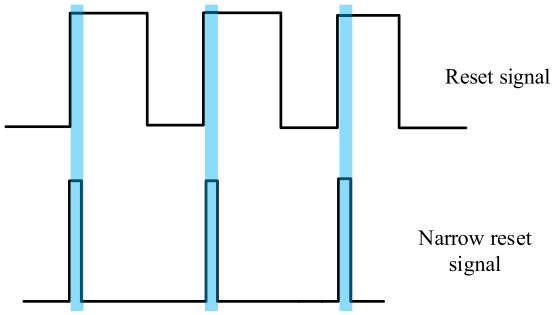


Fig. 9. Using the monostable trigger to narrow down reset signal pulse.

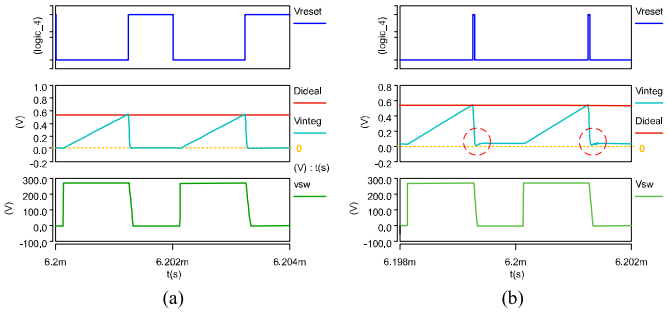


Fig. 10. Simulation waveforms with circuits models. (a) Without monostable trigger. (b) With monostable trigger.

closed-loop modulation controllers alternate between Modes A and B. However, it introduces extra cost and design complexity.

To address this issue, a simpler scheme is proposed by inserting a monostable trigger between the reset switch and the RS flip–flop. The illustration of this circuit is given in Fig. 9. By shaping the varying duration of the long reset pulse to a narrow pulse with a fixed duration through a monostable trigger, the capacitor of the integrator is only reset to zero for a short time, and then it can be swiftly charged to a voltage level due to the integration of $V_{\rm ds}$ during the falling transient and the deadtime. From simulation results in Fig. 10, it is clear that this voltage becomes the initial value of the integrator for next switching cycle and compensate the error in the turn-OFF and deadtime regions in the new cycle.

The duration time of narrow pulse also has impacts on the power quality of ac waveforms and it can be modified by changing *RC* values in the monostable trigger circuits. The power quality comparisons of output current under two different duration times of narrow pulse are conducted in the simulation. When the duration time of the narrow pulse is set as 300 ns, the THD of the output current is 5.8%. As it drops to 100 ns, the THD of output current also drops to 0.5%. As a result, the duration time of the shaped narrow pulse in real circuits design should not exceed 100 ns.

2) Maximum Duty Cycle Limitation: The second issue is the maximum duty cycle limitation. Under the high switching frequency and the maximum duty cycle point, the fully compensated duty cycle may exceed one, as clearly illustrated in Fig. 11 based on the theoretical derivation in Section II. This could cause abnormal operation of the closed-loop modulation controller since it means that the output voltage of integrator

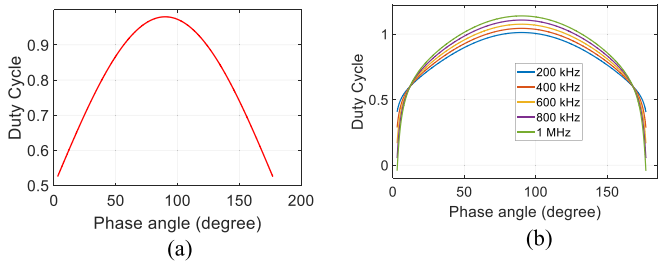


Fig. 11. Maximum duty cycle illustration. (a) Uncompensated duty cycle for gate drive. (b) Compensated duty cycle for gate driver.

cannot be accumulated to $D_{\rm ref}$ even if the duty cycle is adjusted to the maximum one, leading to the failure of the reset event. To solve this problem, another reset signal $D_{\rm reset}$ shown in Fig. 14 is added to control the reset signal of RS flip–flop from the DSP controller when the duty cycle is close to one. With this extra control of the reset signal, RS flip–flop will be forced to reset to zero level and the voltage of integrator capacitor will be also discharged to 0 V if the duty cycle arrives at the preset of the maximum duty cycle.

3) Time Delay of Logic Circuits: The third issue is the time delay of the logic circuits in the closed-loop modulation controller. In general, the closed-loop modulation controller has the capability to compensate any voltage errors induced by the time delay between control signals and gate signals (including the errors of the propagation time and the delay time of the digital ICs) even though the delay does not necessarily cause the distortion. The real concern here is still when the duty cycle is close to one, the time delay of the logic circuits including the comparator and logic gates causes a delay to the reset signal of RS flip–flop so that the reset signal may be even later than the next cycle set signal of RS flip-flop from DSP. It results of race hazard of the RS flip–flop at the maximum duty cycle and causes the uncertain or wrong logic outputs of the RS flip–flop and chaos in the final switching signal outputs. Specifically, this will lead to the turn-ON failure of the switch and the losing of switching action for next switching cycle since the reset signal is still at the effective logic level after the set signal goes to the low logic level, and the output of RS flip–flop maintains the low logic level during entire next switching period.

To investigate the effects of the time delay on the controller, a time delay unit is adopted in SABER to perform the different time delays of the logic circuits. Fig. 12 gives one simulation example to illustrate the problem. The reset signal keeps effective logic level even after the holding time of the set signal of RS flip–flop when this issue happened. Fig. 13 shows the output current waveform under the half load when the maximum duty cycle $D_{\rm max}$ equals 0.9. When the time delay is set as 80 ns in Fig. 13(a), the output current is a normal sinusoidal waveform. When it is increased to 200 ns in Fig. 13(b), the closed-loop modulation controller cannot work normally, and the output current waveform performs weird behavior around the maximum duty cycle. Therefore, the selection of logic circuits should be very careful to maintain a relatively low time delay for high-frequency operation.

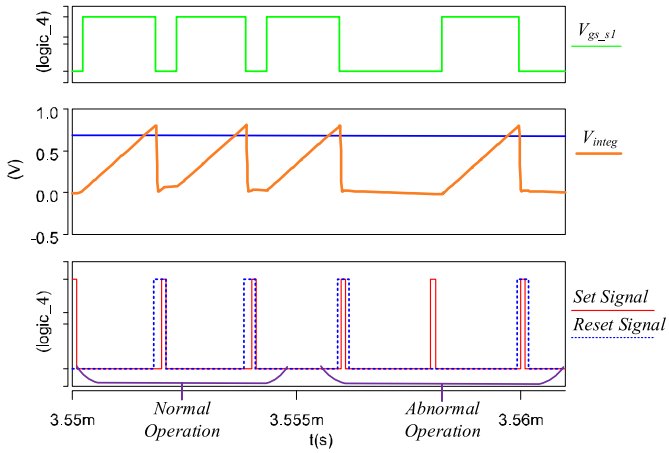


Fig. 12. Abnormal waveform with a large delay time of logic circuits.

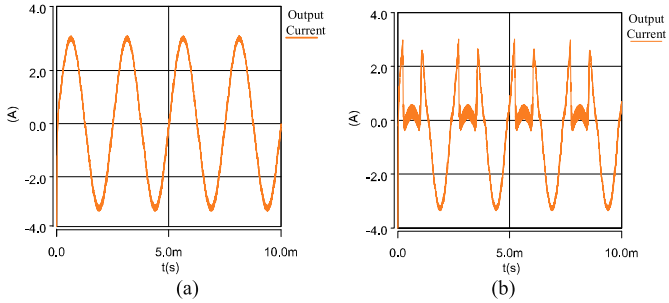


Fig. 13. Output current waveform under $D_{\max} = 0.9$. (a) Time delay is 80 ns. (b) Time delay is 200 ns.

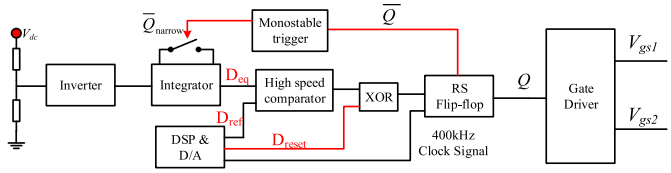


Fig. 14. Updated closed-loop modulation scheme.

TABLE III
COMPARATOR RESPONSE TIME COMPARISON

Parameter	Test conditions	LM311	TLV3501A	Unit
Response time, low to high	Rc= 500 Ω to 5 V, C_L=5 pF	115	4.5	ns
Response time, high to low		165	7	ns

IV. IMPLEMENTATION OF PROPOSED MODULATION CLOSED-LOOP SCHEME

The final closed-loop modulation scheme is given in Fig. 14. This section will illustrate the implementation of key components in a closed-loop modulation controller. Based on discovered issues in last section, one of important criteria to select logic devices is to keep the delay or response time low. Table III shows the comparison of the response time of two comparators.

TABLE IV
DEVICE SELECTION RESULTS FOR A CLOSED-LOOP MODULATION CONTROLLER

Part number	Function
ADI 817	PWM voltage inverter
OPA 192	High precision integrator
TLV3501A	High-speed comparator
CD54AC74	High-speed RS flip-flop
SN54AHCT123A	Monostable trigger
Si8274	Complementary gate driver IC with high common mode transient immunity

LM311 is one of most commonly used comparators supplied by bipolar voltages, and the merit of this comparator is allowance of negative voltage as inputs. However, its response time around 115 ns is relatively long for this high-frequency application. Hence, TLV3501A is chosen for its extremely short response time (5–7 ns), but the inconvenience is this comparator only allows positive voltage as inputs.

The transfer function of the integrator is given in (9). Considering a negative sign exists in the transfer function, the output of the integrator voltage is negative when the scaled positive PWM voltage is connected as an input. Thus, an inverter needs to be inserted to guarantee that the input voltage of the comparator is positive

$$V_o(s)/V_{\text{in}}(s) = -\frac{1}{sR_iC_f}. \tag{9}$$

Two possible positions can be selected for the insertion of an inverter: before the integrator or after the integrator. The better position is after the integrator since the integrator functions as a low-pass filter, and it is easier to achieve high accuracy compared to directly invert scaled the PWM voltage before the integrator. Nevertheless, the high-speed analog switches also only accept positive voltage for inputs, so the voltage of the capacitor inside the integrator circuits cannot be negative, which means the inverter must be inserted before the integrator. Hence, a high-bandwidth amplifier (50 MHz) from analog devices (ADI) is chosen for the inverter and its part number is ADI 817. One critical parameter for the inverter is slew rate of the output voltage, and ADI 817 can provide 350 V/μs. The highest dv/dt under 270 V dc bus for GaN HEMT is around 50 V/ns, which is much higher than the voltage slew rate of the amplifier. However, after scaling down the PWM voltage, the dv/dt is also scaled to 185 V/μs when assuming the voltage sampling ratio is 1/270. This guarantee the accuracy of the inversion of the scaled PWM voltage. The integrator is selected from TI OPA 192, which is a high precision operational amplifier with the ultra-low input bias current (20 pA max). The analog switch is also selected from TI TS5A1066 with a very low turn-OFF and turn-ON time around 5 ns.

The implementations of left circuits are not difficult and just choose the low delay time logic IC for better performance. Table IV gives overall device selection results for a closed-loop modulation controller. These circuits are placed in the gate driver board in the prototype.

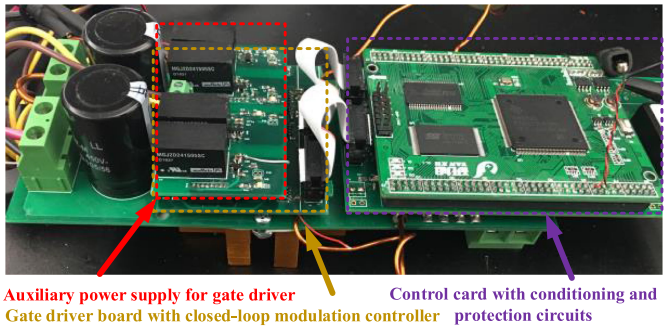
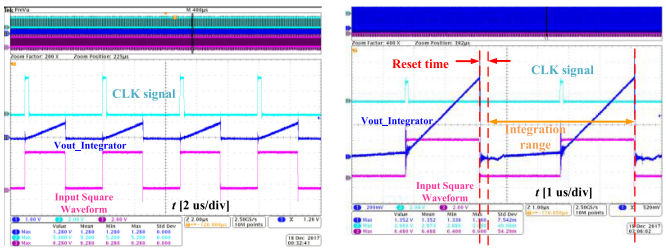


Fig. 15. Prototype picture.

TABLE V
PROTOTYPE PARAMETERS

Parameters	*Value*	*Parameters*	*Value*
Input voltage V_{DC}	270 V	Output capacitance C_{out}	8 μF
Output voltage V_{out}	115 V AC	GaN HEMT	GS66502B from GaN Systems
Output frequency f_o	400 Hz	DSP controller	TMS320F28379D
Nominal power P_o	1200 W	Dead time	200 ns
Switching frequency f_s	400 kHz	Gate resistance	20 Ω
Filter inductance L_f	40 μH		



(a) (b)

Fig. 16. Charge control function verification under signal level. (a) Integrator testing waveform. (b) Monostable testing waveform.

V. EXPERIMENTAL VERIFICATION

A full-bridge inverter was built for the verification of the proposed scheme as shown in Fig. 15. The prototype parameters are given in Table V. The basic function of charge control under high frequency is verified under signal level. A 400-kHz square wave produced from the signal generator is used as an input signal to emulate the scaled PWM voltage. The testing waveforms are shown in Fig. 16. clock signal (CLK) is the set signal of RS flip–flop to enable the switch to turn ON, and when it becomes to the high level, the square wave also turns to high and begins to integrate. When the output voltage of integrator touches the threshold voltage of the comparator, the comparator turns the gate signal to low, then the analog switch will turn ON to reset the voltage of integrator to zero. The difference of this circuits is the duration time of the reset signal shown in Fig. 16(b) compared to the traditional charge control. The duration time of the rest signal only holds 100 ns instead of the whole OFF-state time of the switch. After the reset time, the integrator starts to work again, and the voltage error caused by a falling edge and the deadtime during turn-OFF can be accumulated for compensation in the next switching cycle.

Fig. 17 illustrates the different mechanisms of PWM voltage distortions. To observe the deadtime-induced voltage error more easily, the PWM voltage at the switching point is measured under 50-V dc-bus voltage. Since the forward voltage of behavior-like body diode of GaN HEMT is around 5 V for a given –3 V gate voltage under OFF-state, it is easier to distinguish the freewheeling conduction time during the deadtime. The plateau during the deadtime is 10-V above dc bus voltage because of the forward voltage of two GaN HEMTs in series during the deadtime.

Based on the analysis on Section I and the classification in Fig. 2, voltage error shown in Fig. 17(a) is because of the deadtime and the slow turn-OFF transients of S_2 in Mode B when S_2 is the active switch; voltage error shown in Fig. 17(b) is because of the deadtime and the slow turn-OFF transients of S_1 in Mode A when S_1 is the active switch; voltage error shown in Fig. 17(c) is due to the deadtime and the slow turn-OFF transients both of S_2 and S_1 in Mode C when the inductor current is around zero crossing point.

To prominent PWM voltage distortion and verify the effectiveness of the proposed scheme, the deadtime is chosen as 200 ns. Fig. 18 displays output current waveforms of the inverter under full load. Without closed-loop modulation control, the output current waveform shown in Fig. 18(a) has the obvious distortion, and its harmonics spread out on third, fifth, seventh, and ninth harmonics. After enabling the closed-loop modulation, the output current waveform shown in Fig. 18(b) becomes less distorted. From Fig. 18(d), the THD of output current waveform with a closed-loop modulation controller was reduced from 6.11 to 1.89%. Also, the third, fifth, seventh, and ninth harmonics are decreased a bit compared to the results shown in Fig. 18(c).

Fig. 19 illustrates the compensation effects by comparing the switching signal of switch S_1 with and without compensation scheme. Fig. 19(a) shows the switching signal without compensation scheme, while Fig. 19(b) shows the switching signal with the compensation scheme. Through comparison, around the load current peak, the duty cycle of the compensated switching signal is a little bit larger than one of the uncompensated switching signal, and no obvious duty cycle difference exists since only the deadtime-induced PWM voltage error needs to be compensated. However, around the zero-crossing point, the duty cycle of the compensated switching signal is obviously smaller than one of the uncompensated switching signal since both the deadtime and the slow turn-OFF transient-induced PWM voltage errors needed to be compensated. The trends of the difference between the duty cycle with and without compensation at experimental results agreed with the theoretical prediction in Fig. 11.

Fig. 20 gives the soft start waveforms with closed-loop modulation. With a smooth increase of the reference duty cycle output D_{ref} by D/A from DSP, the integration signal of

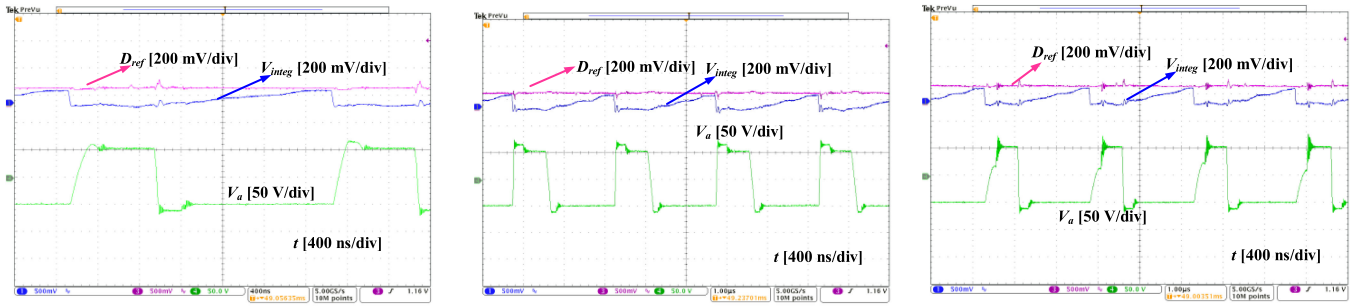


Fig. 17. Illustration of PWM voltage distortion at $V_{\rm dc} = 50$ V. (a) Voltage error caused by rising edge and deadtime in Mode B-[c]. (b) Voltage error caused by falling edge and deadtime in Mode A-[b]. (c) Voltage error caused by rising edge and deadtime in Mode c-[h].

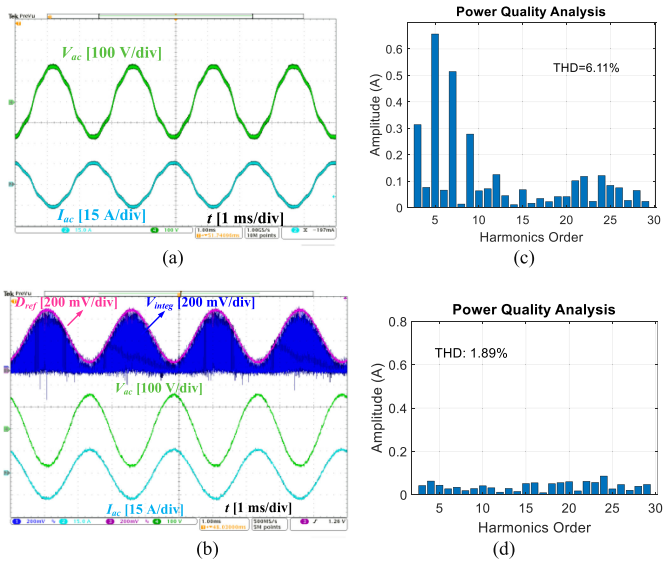


Fig. 18. Comparison of power quality of output current waveforms under full-load condition. (a) Testing waveform without closed-loop modulation. (b) Testing waveform with closed-loop modulation. (c) Harmonics analysis without closed-loop modulation. (d) Harmonics analysis with closed-loop modulation.

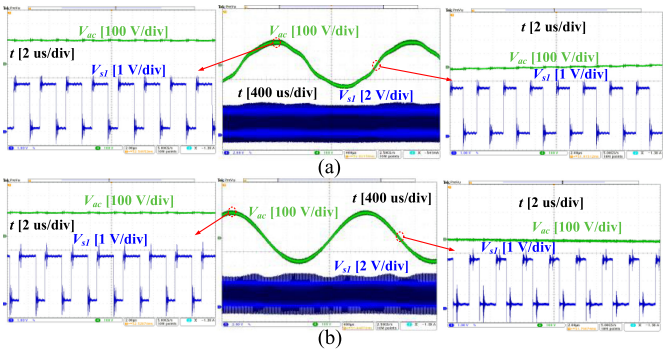


Fig. 19. Switching signal comparisons at peak current and zero-crossing points. (a) Without compensation. (b) With compensation.

PWM voltage also increased smoothly by keeping tracking the envelope of the reference duty cycle. It demonstrates that the compensation scheme can work well during the dynamic procedure.

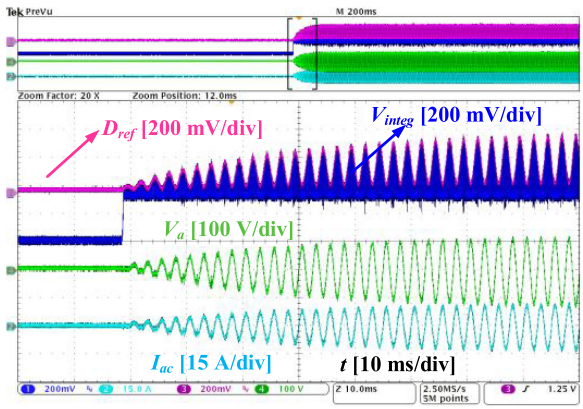


Fig. 20. Start-up waveforms with closed-loop modulation.

VI. Conclusion

To obtain a practical feedback control of duty cycle compensation, this paper proposed a charge control-based closed-loop modulation scheme. The proposed control does not need instantaneous inductor current sampling and online calculation compared to the feedforward type compensation. Moreover, there were several advantages for this scheme. One was to enhance noise immunity by introducing the integrator to integrate instantaneous PWM voltage. The integrator could function as a low-pass filter providing the attenuation for the high-frequency ringing and noise during the switching transients. The other was that this scheme was easy to implement on the gate driver board with the tiny space and simple hardware.

Compared to the traditional charge control, monostable trigger and maximum duty cycle limitation were implemented to improve the accuracy of the duty cycle compensation. The circuits to realize the closed-loop modulation were designed carefully, and suitable low delay-time devices were selected for high-frequency application. The experiment was carried out to demonstrate the proposed scheme. The THD of output current waveform could be reduced from 6.11 to 1.89% with closed-loop modulation.

The major limitation to implement the proposed closed-loop modulation for even higher switching frequencies (above 400 kHz) was the time delay of the logic circuits. One

future work is to utilize low-cost field-programmable gate array/complex programmable logic device to replace discrete logic ICs and to shrink the time delay, which can enable the proposed scheme to adapt to the application with even higher switching frequency.

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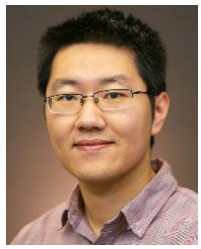

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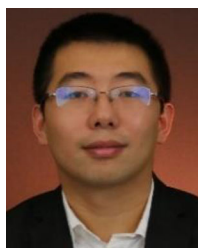

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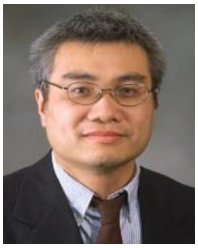

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