

# Bridging Gaps in Paper Design Considering Impacts of Switching Speed and Power-loop Layout

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**Abstract**— In power electronics design, the selection of power semiconductors mainly considers the voltage and current ratings, power loss, and operating frequency capability. However, in the paper design stage, the impacts of switching speed and busbar or PCB layouts related geometries design on the converter system are not considered comprehensively, which may introduce a trial-and-error procedure of selecting the gate resistance in the implementations due to overvoltage and cooling capability issues. To shrink the design gaps between the paper design and implementations, with advanced modeling methods and design automation programs, this paper proposes a systematic design approach for power semiconductors selection and cooling system design considering the impacts of switching speed and power-loop layout. The discrete-time switching behavior model for the switching speed prediction and automatic geometry creation program for the power-loop layout are developed to determine the gate resistance in the paper design stage, and the partial element equivalent circuits (PEEC) numerical modeling method is adopted to extract the parasitic inductance for the created geometries. After the determination of gate resistances for the selected device and topology, a multi-variable switching loss scaling method with the discrete-time switching behavior model is used to get the more accurate device losses for the cooling design. A complete design iteration and related verifications are also given in this paper.

**Keywords**—paper design, gate resistance selection, power loop layout, modeling

## I. INTRODUCTION

Power semiconductor selection, the corresponding cooling design, and gate resistance selection play very important roles in the power electronics design, affecting the converter performance in different aspects like efficiency, safe operation, and power density. In the conventional design approach, the switching loss model, cooling design, and PCB layout are closely related to this topic, and much research has been done.

For the switching loss model, one widely applied analytical model in [1] has a linear assumption on the switching waveforms. Then, with this assumption, the switching loss can be derived by calculating the overlap area of voltage and current waveforms during switching intervals. However, the analytical model in [1] often cannot achieve a satisfying accuracy compared with experimental results since switching waveforms are varied with different types of power switches, and the model

is also too simplified without considering the parasitics and layout. Some research [2-4] develops advanced switch behavior models to predict the switching waveforms considering the gate resistance and parasitics, and the switching loss is calculated with the integral of the derived voltage and current waveforms. However, it requires the inputs of the layout parasitic inductance and gate resistance, which is unknown in the paper design stage. Another way to estimate the switching loss is to use the measured data from a double pulse test (DPT) or calorimetric measurements, but it is not time efficient and requires a similar layout with the final implemented converter. Also, when the paper design is required to evaluate numerous candidates of power devices, the linear scaling method with one measured data from the device's datasheet is the most common way to calculate switching loss in the conventional converter design. However, the measured switching loss data is only effective for one specific testing condition while the gate resistance and operating conditions are usually different in practical cases compared with the testing condition in the datasheet, leading to uncertain errors. E.g.,  $E_{on}$  and  $E_{off}$  given at 400 V 10 A with a 10  $\Omega$  gate resistance in the datasheet are applied in the paper design for the switching loss calculation when using a 650 V 20 A rated SiC device, but the practical gate drive adopts a 5  $\Omega$  gate resistance and the switches operate at 500 V with different current levels.

For the PCB layout, a general concept called the magnetic field cancellation is applied to reduce the power loop parasitic inductance [5]. With the help of the internal layer of power plane, a minimized vertical power loop area can be achieved for the parasitics inductance reduction. Similar to PCB layout, a planar laminated busbar structure is the most common structure to minimize the power loop inductance [6]. To extract the stray inductance more accurately, numerical analysis methods are applied, such as finite element analysis (FEA) [7-9], and partial element equivalent circuit (PEEC) [10-11]. However, all those methods demand manual drawing of geometries after confirming the selection of switches and dc-link capacitors, which cannot enable the evaluations of switching behavior considering the package dimensions and geometry limitations in the paper design stage. Once the gate resistance is adjusted due to the overvoltage issue in the debug or testing stage, the switching loss is also changed with the gate resistance that

causes insufficient cooling capability of the designed cooling system.

As a result, it is a common experience that a trial-and-error procedure may be required in the testing and debug stage. The missing links in the conventional paper design approach are the selection of the gate resistance (evaluation of the switching speed) and power-loop layout who significantly influence the overvoltage containment, cooling design, and even EMI bare noise.

In this paper, to shrink above gaps in the paper design of power electronics converters, an automatic busbar or power loop creation method is developed using an open-source geometry description scripting language [12]. Then, the PEEC method is applied to extract the parasitics inductance as the input variable to the discrete-time switching behavior model. With those models, an iteration is conducted to determine the proper gate resistances to avoid an overvoltage issue and a malfunction of gate drive. Then, the switching loss can be calculated with the proposed multi-variable scaling method, and the whole design iteration is also given including the gate resistance determination and cooling design.

## II. AUTOMATIC CREATION AND NUMERICAL MODELING OF LAYOUT RELATED GEOMETRIES

In most cases, geometry structures in busbar design and PCB layout are not complex. They are made of traces, holes, and planes. Also, a general rule of magnetic field cancellation is followed to design the busbar structure and PCB layout. Specifically, for a busbar, a laminated structure with the overlap of the positive and negative busbar is generally applied. For PCB layouts, a vertical power loop similar to the laminated busbar is always adopted to reduce the parasitic inductance. To reduce the power loop area, the dc-link capacitors or the decoupling capacitors should be placed as close as possible to the power devices. With such rules, the basic geometry of busbars and PCB layouts and components arrangement for different topologies can be predefined, and the dc-link capacitors and power devices will be fitted into the geometry design based on the dimensions of packages. One example of the predefined geometry of a two-level converter is given in Fig. 1, the dimensions of the layout will be adjusted based on the selected device and dc-link capacitor.

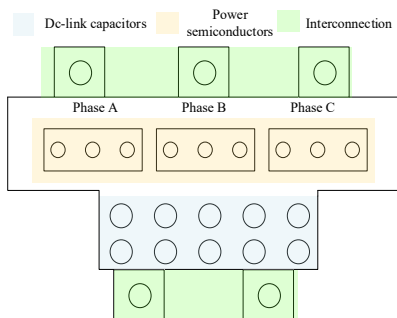


Fig. 1. One example of predefined two-level voltage source inverter layouts.

To automatically create the predefined geometries with the selected devices and capacitors, an open-source geometry

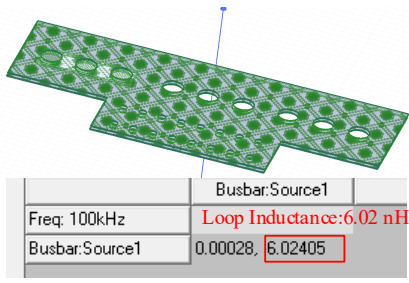
description scripting language originally developed by Mattan Kamon at M.I.T. is chosen [12]. It was developed for describing the geometries in interconnect problems for IC package design. In this scripting language, all geometries are defined in an x-y-z coordinate and it can easily define holes, traces, and planes, which is good enough to describe the geometries in power electronics design.

Moreover, an automatic script generation function is developed in MATLAB to create the geometry scripting file for the parasitics extraction. The required inputs for the automatic script generation are the dimension information of the selected power device and dc-link capacitor, operating frequency, the thickness of the busbar and insulation material. Specifically, the device packages (discrete type, surface mount or power module), the number of pins, pin pitch and diameter of holes are necessary to create the geometries for the busbar or power loop layout. Similarly, the detailed information of terminals (pins) of dc-link capacitors is required for geometry creations. Hence, the impacts of holes on the power-loop parasitic inductance are covered. With required input parameters, the automatic geometry creation program will first calculate the coordinate values for traces, holes, and planes which form the power-loop based on the selected topology. Second, based on the analysis frequency, the segment arrangement of the geometry and equipotential points for different layers are defined in the program. At last, all definitions and configurations of geometry, segment arrangement, and equipotential points are generated based on the syntax rules of the geometry description scripting language in [12] with the built-in “fprintf” function in MATLAB. The created new file has an extension as “.inp”, which can be recognized by the fast field solver FastHenry2 with PEEC numerical method.

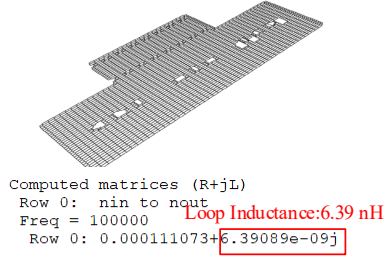
One automatic geometry creation example of the two-level VSC is given in Fig. 2 with the SiC power module CAS120M12BM2 from Wolfspeed and dc-link capacitors B25620B1197K983 from EPCOS. The busbar design with manual drawing in SolidWorks based on the predefined structure in Fig. 1 is given in Fig. 2(a) while the automatically created geometry with the geometry description scripting language is given in Fig. 2(b). The holes in Fig. 2(b) have low display resolution because of the low number of segments, and the developed visualization program cannot handle the display with a large number of segments due to heavy memory utilization.

To verify the effectiveness of the implemented PEEC method, two geometry examples are used for parasitic inductance extractions through FEM software Q3D and PEEC algorithm. The first geometry example is created automatically for a busbar design for a two-level converter. As Fig. 2 shows, the inductance values from FEM and PEEC are close, and the difference is 6.17%.

The second example is from the practical PCB layout of one 10 kW ANPC converter shown in Fig. 3. For the PEEC method, planes are used to model the power loop layout while, for the FEM method by Q3D, PCB layout in Altium Designer can be directly imported into the software for the simulation. Also, the thickness of the cooper is set as 2oz. Fig. 3(a) and (b) gives two parasitic inductance results for the short commutation loop in



(a) FEM result



(b) PEEC result

Fig. 2. Geometry comparison and extracted inductance value comparison of the laminated busbar between FEM and PEEC.

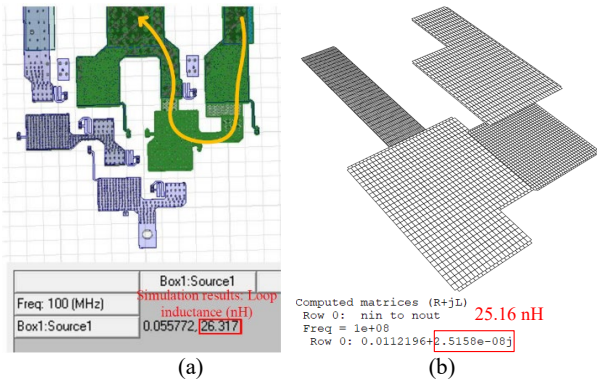


Fig. 3. Extracted inductance value comparison of ANPC layout between FEM and PEEC: (a) FEM result for short commutation loop, (b) PEEC result for short commutation loop.

the ANPC converter with FEM and PEEC methods and the difference is 4.45 %. This comparison demonstrates that the PEEC method can achieve similar accuracy of parasitic inductance calculation compared with the FEM method.

### III. GATE RESISTANCE SELECTION WITH SWITCHING SPEED OPTIMIZATION

#### A. General Constraints

Before giving the gate resistance constraints limited by the switching speed, some general gate resistance selection criteria are given in this subsection. For gate drive circuits during turn-on and turn-off transients, it was formed of an LCR resonant circuit, which is a classical second-order system. To avoid the oscillations of the gate voltage and current, it was necessary to avoid the system as an underdamped state. To make the damping ratio larger than 1, the oscillation of the gate voltage and current can be avoided, which gives a gate resistance lower limit as:

$$R_G \geq 2\sqrt{\frac{L_G}{C_{GS}}} \quad (1)$$

where  $R_G$  is the gate resistance including the internal and external gate resistance,  $C_{GS}$  and  $L_G$  are the parasitic capacitance between gate and source and gate loop parasitic inductance, respectively.

The second constraint is to select the proper gate resistance to limit the initial gate current not to exceed the maximum source and sink current, which is only required when perfering a specified gate drive. The purpose of this is to let the totem pole circuit inside the gate drive IC not work in the saturation region. The reason is that the switching behavior model in this paper did not consider the gate drive modeling in the saturation region so that limiting the maximum gate current can help improve the modeling accuracy of the switching behavior.

$$R_G \geq \frac{V_{cc} - V_{ee}}{I_{gmax}} \quad (2)$$

where  $V_{cc}$  and  $V_{ee}$  are the steady-state gate voltages for turn-on and turn-off,  $I_{gmax}$  is the maximum gate current determined by the peak sink and source current capability of gate drive IC.

#### B. Gate Resistance Selection with Switching Speed Limitation

For the turn-off gate resistance, combined with Eq. (1) and Eq. (2), an initial gate resistance can be decided. Nonetheless, this initial gate resistance generally has a very low value to cause an unaccepted voltage spike due to the drain-source voltage oscillation. The diagram of the determination of the turn-off gate resistance to avoid the overvoltage issue is given in Fig. 4(a). Once a device is selected from the database, the power loop layout will be automatically created by the program presented in Section II, and the corresponding parasitic inductance is evaluated with the PEEC algorithm. Then a discrete-time switching behavior model is applied with device parameters to predict switching speed  $dv/dt$  and the voltage spike during turn-off. If the voltage spike exceeds the target limit during turn-off, the turn-off gate resistance will be increased until the voltage spike is lower than the preset limit.

For the turn-on gate resistance selection, another lower limit can be decided to prevent the malfunction of gate drive at off-state during the high  $dv/dt$  event created by the complementary switch, which is shown in Fig. 4(b). The voltage across the gate to source during  $dv/dt$  cannot exceed the threshold voltage  $V_{th}$  for preventing the switch from false turn-on. The expression of  $v_{gs}$  during  $dv/dt$  can be derived as

$$C_{gd} \cdot \frac{dv}{dt} \cdot (R_{G\_off} + R_{sink}) \cdot \left( 1 - e^{-\frac{\Delta t}{(R_{G\_off} + R_{sink})(C_{gd} + C_{gs})}} \right) \leq 0.8V_{th} \quad (3)$$

where  $dv/dt$  value and the turn-on time  $\Delta t$  are determined by  $R_{G\_on}$  of the complementary switch. A 20% margin is given for the threshold voltage judgment.

Since the turn-off resistance is determined to avoid the voltage spike of  $v_{ds}$ ,  $R_{G\_off}$  cannot be adjusted to reduce the gate voltage during  $dv/dt$  caused by the turn-on of the complementary

switch. As Fig. 4(b) shows, the turn-on resistance  $R_{G, on}$  will be increased to reduce  $dv/dt$  value until Eq. (3) is satisfied.

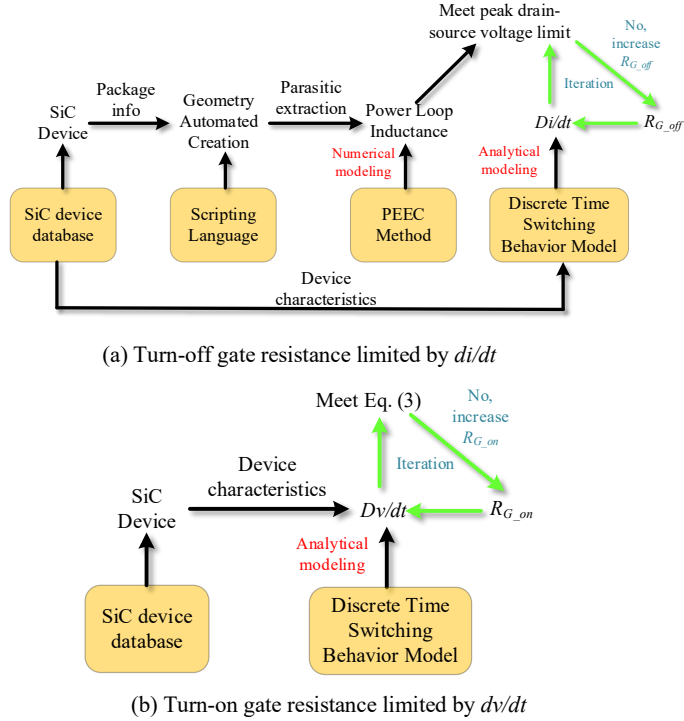


Fig. 4. Diagram of the determination of gate resistances considering switching speed.

### C. Switching Behavior Model and Verifications

In the proposed design approach, the switching behavior model of power semiconductors is critical to predicting the switching speed and voltage spike accurately. Here, a discrete-time modeling method with state-space matrices are applied, which is similar to the work in the literature [2,4]. The turn-on and turn-off processes are divided into four intervals with the corresponding state-transition matrix [2].

Compared with previous modeling work, this paper incorporates more non-linear parameters of devices. Hence, the impacts of junction temperature on the switching behavior are considered. First, the transconductance  $g_m$  is a function of the junction temperature  $T_j$  and the voltage difference ( $v_{gs}-V_{th}$ ), and the transconductance curves can be obtained from the transfer characteristic curves in Fig.5(a), and the fourth-order polynomial equation is used to fit the transconductance curves as a function of the junction temperature and the voltage difference ( $v_{gs}-V_{th}$ ). The fitting results are shown in Fig.5(b). Second, the threshold voltage  $V_{th}$  is also a function of the junction temperature which impacts the switching behavior, and a linear interpretation method is used for curve fitting shown in Fig.6. With those fitting functions, the variations of transconductance and threshold voltage with temperature are added to the discrete-time modeling for higher accuracy.

Moreover, based on [4], the non-linear characteristic of  $C_{gs}$  as a function of  $v_{gs}$  should also be considered. However,

generally, the characteristic of  $C_{gs}$  with  $v_{gs}$  is not given in the datasheet, requiring extra efforts to characterize  $C_{gs}$  curve with a curve tracer. Fig. 7 shows one measuring example through the curve tracer, and the fitting function is established for discrete-time modeling.

To compare the developed model with real switching behavior performance, a DPT is conducted with the SiC MOSFET C3M0065090J with a D<sup>2</sup>park package, and the prototype is shown in Fig. 8. With testing results, two cases with the different gate resistances are used for the comparison and study. For a fair comparison, the developed switching model applies the same parasitics of the DPT board and the same gate drive parameters.

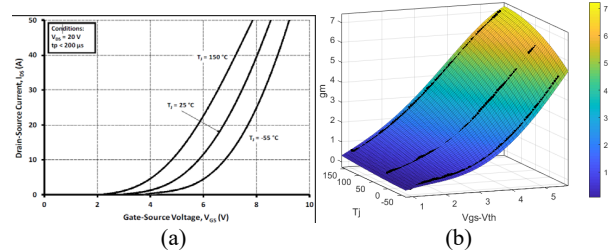


Fig. 5. Curve fitting results of transconductance as a function of junction temperature, (a) example of transfer characteristics at different temperatures, (b) curve fitting of transconductance.

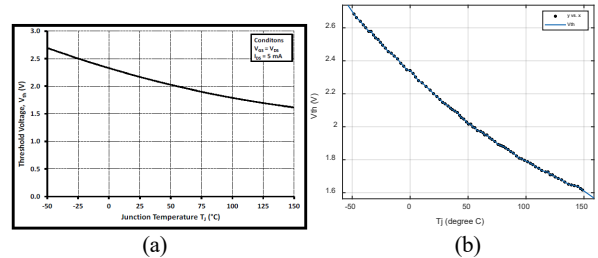


Fig. 6. Curve fitting results of threshold voltage as a function of junction temperature, (a) example of threshold voltage at different temperatures, (b) curve fitting of threshold voltage.

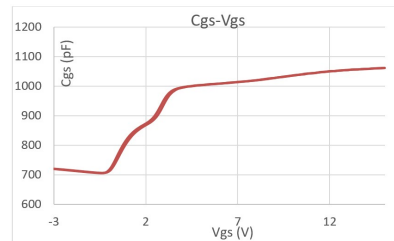


Fig. 7. The characterization results of  $C_{gs}$  as a function of  $v_{gs}$ .

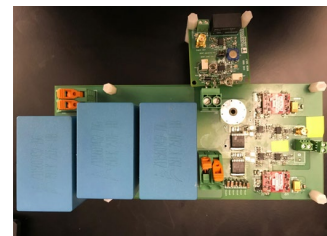
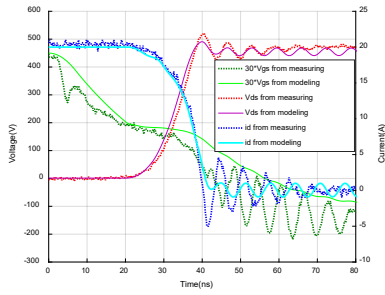
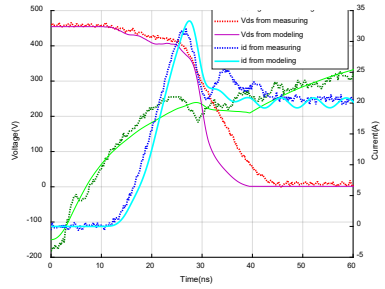


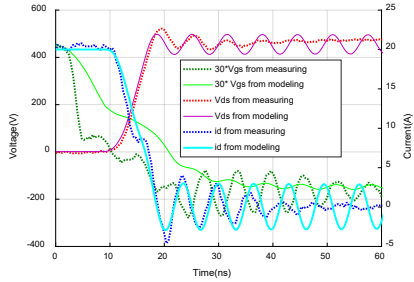
Fig. 8. The prototype of DPT platform for SiC MOSFET C3M0065090J.



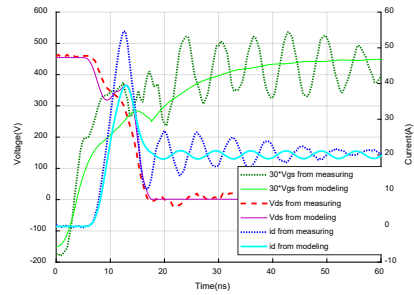
(a) Turn-off waveforms comparison @  $R_g=20 \Omega$



(b) Turn-on waveforms comparison @  $R_g=20 \Omega$



(c) Turn-off waveforms comparison @  $R_g=2.5 \Omega$



(d) Turn-on waveforms comparison @  $R_g=2.5 \Omega$

Fig. 9. Waveform comparison at the testing condition of 450 V and 20 A with different gate resistances.

Thus, a waveform comparison was conducted at the testing condition of 450 V dc-link and 20 A load current. In Fig. 9, turn-on and turn-off waveforms are compared when the gate resistances are 20  $\Omega$  and 2.5  $\Omega$  respectively. For turn-off waveforms comparison, from Fig. 9(a) and (c), the waveforms of  $v_{ds}$  and  $i_d$  from the developed model match the testing waveforms well no matter what the gate resistance is used, but the  $v_{gs}$  modeling waveforms have some discrepancies compared with testing waveforms. The possible reason is the measured  $v_{gs}$  waveform is not a real  $v_{gs}$  waveform due to the parasitics of

interconnection and wire bonding compared with the developed model. For turn-on waveforms comparison, from Fig. 9(b), the  $i_d$  waveforms are close but the  $v_{ds}$  waveforms have the obvious discrepancy when the gate resistance is 20  $\Omega$ . However, when the gate resistance changes to 2.5  $\Omega$ , the discrepancy of  $v_{ds}$  waveforms becomes smaller but the resonant amplitudes of  $i_d$  waveforms have an obvious difference. The possible reason is the gate drive of the high-side switch is not modeled, and the switch current contributing by the cross-talk is not modeled and included.

Table 1 further gives some key parameter comparison between the predicted results and the testing results. In terms of switching speed prediction, the errors of predicted results are acceptable to evaluate the overvoltage or  $dv/dt$ ,  $di/dt$  value. The overvoltage estimation error is within 5%, and the error of  $dv/dt$  and  $di/dt$  is below 15%. However, for the switching loss estimation, especially for turn-on with a 20  $\Omega$  gate resistance, the error can be up to 25.3%.

Since the switching speed and overvoltage prediction are the main objectives here, even though the developed model cannot achieve very high accuracy of the switching loss prediction, it is still good enough to use the developed model to estimate the switching speed and to select the proper gate resistance.

Table 1. Key parameter comparison between the predicted results and the testing results.

Parameters	2.5 $\Omega$		20 $\Omega$	
	Measured	Predicted	Measured	Predicted
Dv/dt during turn-on	115 V/ns	134.1 V/ns	68.1 V/ns	85.4 V/ns
Di/dt during turn-off	3.89 A/ns	3.66 A/ns	2.62 A/ns	2.48 A/ns
$V_{dsmax}$	522 V	497.6 V	512 V	487.3 V
$E_{off}$	13.4 $\mu$ J	14.83 $\mu$ J	39 $\mu$ J	41.7 $\mu$ J
$E_{on}$	80.7 $\mu$ J	72.8 $\mu$ J	165.5 $\mu$ J	122.7 $\mu$ J

#### D. Complete Design Example for Gate Resistance Selection

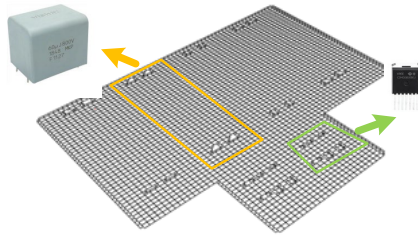
A 900 V SiC MOSFET C3M0065090J is used for a two-level VSC as a design example and four film capacitors MKP1848712924Y5 from Vishay are chosen as the dc-link capacitors. The corresponding layout has been created given in Fig. 10(a) and the parasitic inductance is calculated as 9.1 nH considering the power loop and parasitic inductance of the dc-link capacitors. Other parameters and parasitics are summarized in Table. 2.

With the parameters in Table 2 and the discrete-time switching behavior model, the gate resistance selection results based on the iterations presented in part A and part B in this section are given in Table 3. The predicted turn-off switching waveforms are also given in Fig. 10(b) and (c), and the maximum  $v_{ds}$  with the 5.6  $\Omega$  gate resistance during the turn-off is 887.7 V while the one with the 7.7  $\Omega$  gate resistance is 863.2 V.

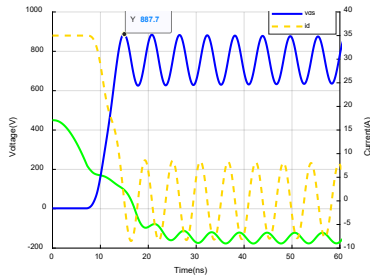
In summary, with the design iterations of the gate resistance selection considering switching speed, the turn-on resistance is selected as 5.8  $\Omega$  and the turn-off resistance is selected as 7.7  $\Omega$  for this design example.

Table 2. Parameters of design example with C3M0065090J.

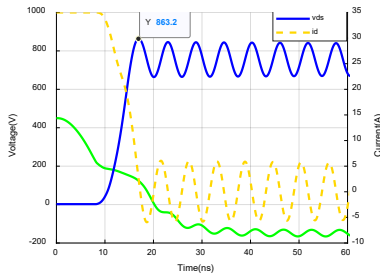
Parameters	Values
Dc-link voltage: $V_{dc}$	750 V
Maximum load current: $I_{acmax}$	35 A
Power loop inductance: $L_d$	7.9 nH
Parasitic capacitance: $C_{gs}$	980 pF
Gate drive voltage: $V_{dr}$	15 V/ -5 V
Required maximum $V_{ds}$ : $V_{dsmax}$	862 V (750*1.15)
Gate loop inductance: $L_g$	2 nH
Common source inductance: $L_{ss}$	0.5 nH



(a) Automatically created geometry



(b)  $R_{G\_off}=5.6 \Omega$



(b)  $R_{G\_off}=7.7 \Omega$

Fig. 10. Automatically created power loop layout and switching waveforms for design example with C3M0065090J.

Table 3. Gate resistance selection constraints summary.

Parameters	Values
Gate voltage damping: Eq. (1)	$\geq 5.6 \Omega$
Gate drive current limitation: Eq. (2)	$\geq 3.3 \Omega$
Design iteration for $R_{G\_off}$ to suppress peak voltage	$\geq 7.7 \Omega$
Design iteration for $R_{G\_on}$ to avoid cross-talk	$\geq 5.8 \Omega$

#### IV. MULTI-VARIABLE SWITCHING LOSS SCALING AND COMPLETE DESIGN ITERATION

The conventional linear scaling method uses the measured switching loss data provided by the datasheet to scale the switching energy loss at arbitrary current and voltage levels, but this method has three limitations. First, the switching loss includes the non-linear part associated with the non-linear junction capacitance as a function with  $v_{ds}$ . Only using the linear scaling method will cause relatively large errors at the low current level and high switching frequency. Second, The switching loss calculation does not reflect the selected or practical gate resistance in the linear scaling method. Third, the impacts of temperature on the transconductance and threshold voltage are not included in the linear scaling method.

To overcome those disadvantages and improve the switching loss calculation accuracy, a multi-variable switching loss scaling method based on the developed discrete-time switching behavior model is proposed. Compared with the linear scaling method, except the operating voltage and current, the selected gate resistance  $R_G$  and the operating junction temperature  $T_j$  are also required as the input variables for the loss scaling. Also, the separation of the non-linear loss related to the junction capacitance and the overlap loss during switching transients has been conducted for higher accuracy.

The non-linear part switching loss is caused by charging or discharging of the junction capacitance, and two losses are associated with this process. During the charging process of a non-linear junction capacitance,  $E_{oss}$  represents the energy stored in the junction capacitance and  $E_r$  represents the energy consumed by the resistive component in the circuits. Because of the existence of non-linear junction capacitance,  $E_{oss}$  and  $E_r$  are not equal like the linear capacitance, and the expression of each part can be expressed as:

$$E_{oss}(V) = \int_0^V C_{oss}(v_c) v_c dv \quad (4)$$

$$E_r(V) = Q(V)V - E_{oss} = \int_0^V V C_{oss}(v_c) dv - \int_0^V C_{oss}(v_c) v_c dv \quad (5)$$

The separation of the switching loss has been summarized in Table 4. The loss distributions of DPT measured data and theoretical data are different since the current sensor cannot directly measure the channel current of power devices. The function  $E_{oss}$  and  $E_r$  at any voltages can be calculated with  $C_{oss}$  fitting function, and the overlap loss  $E_{V1on}$  and  $E_{V1off}$  are obtained by using the  $E_{on}$  and  $E_{off}$  in the datasheet based on the loss distribution in Table 4. Then, the overlap loss  $E_{V1on}$  and  $E_{V1off}$  part will be scaled with the discrete-time switching behavior model by the applied gate resistance  $R_G$ , the assumed junction temperature  $T_j$ , the operating voltage and current.

Table 4. Summary of switching loss separation.

Switching loss	Loss distribution	
	DPT Measured	Theoretical
Turn-on loss $E_{on}$	$E_{V1on} + E_r$	$E_{V1on} + E_r + E_{oss}$
Turn-off loss $E_{off}$	$E_{V1off} + E_{oss}$	$E_{V1off}$

First, the scaling ratio is obtained by using the discrete-time switching behavior model to calculate the overlap loss ratios between the required operating condition and the reference operating condition in the datasheet:

$$\begin{cases} r_{loss\_on} = \frac{E_{V_{ton\_cal}}(R_G, T_j, V, I)}{E_{V_{ton\_cal}}(R_{G\_ref}, T_{j\_ref}, V_{ref}, I_{ref})} \\ r_{loss\_off} = \frac{E_{V_{toff\_cal}}(R_G, T_j, V, I)}{E_{V_{toff\_cal}}(R_{G\_ref}, T_{j\_ref}, V_{ref}, I_{ref})} \end{cases} \quad (6)$$

where  $E_{V_{ton\_cal}}$  and  $E_{V_{toff\_cal}}$  are the calculated values with the discrete-time switching behavior model,  $R_G$ ,  $T_j$ ,  $V$  and  $I$  are the real operating condition in the paper design, and  $R_{G\_ref}$ ,  $T_{j\_ref}$ ,  $V_{ref}$ , and  $I_{ref}$  are the reference operating condition for the measured switching loss data.

Second, the reference turn-on and turn-off energy loss  $E_{on\_ref}$  and  $E_{off\_ref}$  from the datasheet are used to get the updated  $E_{on\_upd}$  and  $E_{off\_upd}$  with the overlap loss ratios:

$$\begin{cases} E_{on\_upd} = r_{loss\_on} \cdot E_{V_{ton\_ref}} + E_r(V) \\ = r_{loss\_on} \cdot (E_{on\_ref} - E_r(V)) + E_r(V) \\ E_{off\_upd} = r_{loss\_off} \cdot E_{V_{toff\_ref}} + E_{oss}(V) \\ = r_{loss\_off} \cdot (E_{off\_ref} - E_{oss}(V)) + E_{oss}(V) \end{cases} \quad (7)$$

To verify the effectiveness of the proposed switching loss scaling method, DPT testing set up for SiC MOSFET C3M0065090J shown in Fig. 8 is used to measure the switching loss data at different gate resistances, testing voltages and currents. The comparison results are shown in Fig. 11(a), (b) and (c) respectively. Also, a group of switching data at different junction temperatures from the datasheet of SiC MOSFET C3M0065090J is used for study and comparison, which is given in Fig. 11 (d).

In Fig. 11(a), the loss data at 150 V and 35 A is used as the reference values, and both the linear scaling method and the proposed scaling scheme are applied to get the switching loss data at 300 V and 450 V. The comparison shows that the scaling results of  $E_{on}$  with the linear scaling method diverge greatly from the measured results of  $E_{on}$ . Although the results from the proposed scheme have a maximum error of 12.1%, they are much more accurate than the results with the linear scaling method for  $E_{on}$ . For Fig. 11(b), the loss data at 450 V and 20 A is used as the reference values, and both methods are applied to get the switching loss data at 5 A and 35 A. Through comparison, unlike the voltage variable scaling, the results of  $E_{on}$  from the linear scaling method does not diverge from the measured data that much. Nonetheless, the results of  $E_{on}$  from the proposed scheme still achieve a smaller error than the ones of the linear scaling method. The maximum error of  $E_{on}$  with the proposed scheme is 26.2 % at 5 A.

For Fig. 11(c) and (d), the loss data are scaled with the gate resistance and the junction temperatures. Although the scaled loss results did not show very high accuracy, it makes the loss results closer to the measured data. E.g., in Fig. 11(c), the scaled  $E_{on}$  for the 20  $\Omega$  gate resistance has a 20.9% error compared with the measured data with 20  $\Omega$  gate resistance, but it is still better

than only using one switching loss data to calculate the switching loss for different gate resistances.

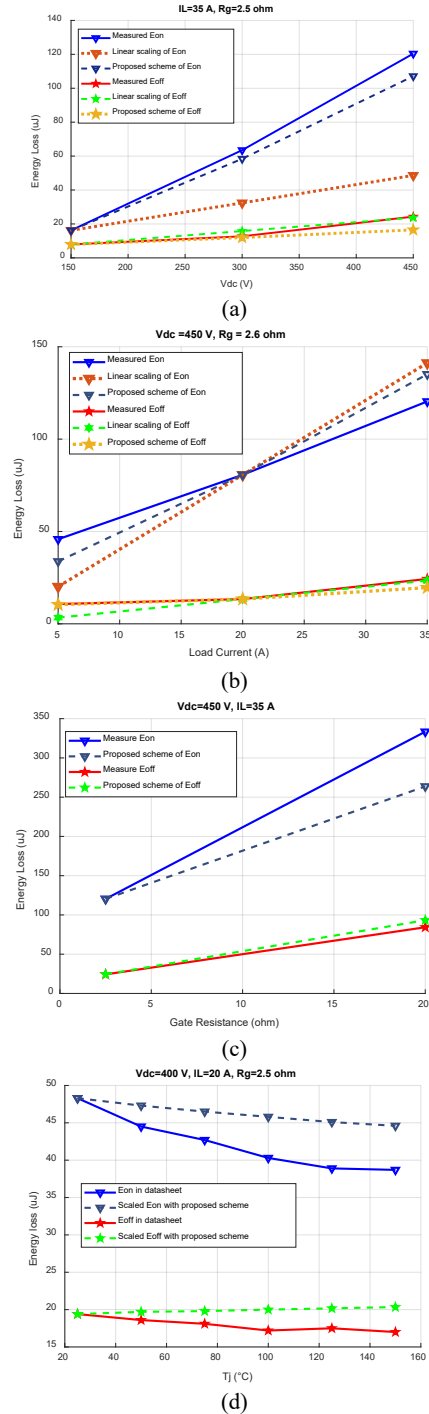


Fig. 11. Switching loss scaling comparison at (a) different testing voltages, (b) different testing currents, (c) different gate resistance, (d) different junction temperatures

Moreover, a complete design iteration combined with the device selection and cooling design is given in Fig. 12. After the initialization of the device database, each device will be

evaluated through the device selection iteration. Also, for each device, the corresponding layout is automatically created based on the package information, and the gate resistance selection iterations are conducted with the parasitics extraction. Then, with the selected gate resistance, the switching loss will be calculated with the multi-variable scaling method considering the gate resistance, operating junction temperature, and voltage and current levels. At final, the cooling design will be done with the calculated device losses. The detailed cooling design procedure will not be given in this paper while the paper [13] is a good reference for the whole cooling design iteration.

### V. CONCLUSIONS

This paper presents a comprehensive paper design approach for the device selection and cooling design combined with advanced analytical and numerical modeling methods. Compared with the conventional approach, the power loop layouts and gate drive resistance selection are incorporated. The power loop layout can be automatically created based on the selected device package and dc-link capacitor dimensions. Then the switching speed for the turn-on ( $dv/dt$  value) and turn-off ( $di/dt$  value) can be determined by the extracted parasitic inductance and reliability constraints. At last, to scale loss data with the selected gate resistance and operation conditions, a proposed multi-variable switching loss scaling method is adopted to improve the accuracy of the loss calculation, and accordingly, a complete design iteration combined with the device selection and cooling design is given.

### ACKNOWLEDGMENT

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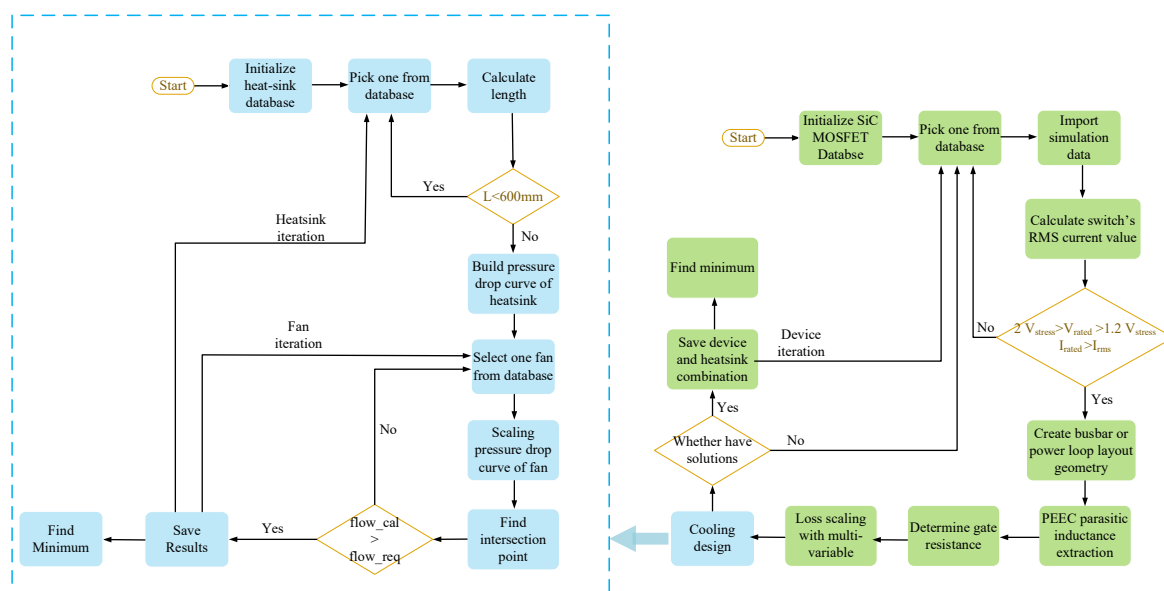


Fig. 12. Complete diagram for the device selection and cooling design.