# Characterization and Failure Analysis of 650-V Enhancement-Mode GaN HEMT for Cryogenically Cooled Power Electronics

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***Abstract*— In order to evaluate the feasibility of newly developed gallium nitride (GaN) devices in a cryogenically cooled converter, this article characterizes a 650-V enhancement-mode GaN high-electron mobility transistor (GaN HEMT) at cryogenic temperatures. The characterization includes both static and dynamic behaviors. The results show that this GaN HEMT is an excellent device candidate to be applied in cryogenic-cooled applications. For example, transconductance at cryogenic temperature (93 K) is 2.5 times higher than one at room temperature (298 K), and accordingly, peak *di*/*dt* during turn-on transients at cryogenic temperature is around 2 times of that at room temperature. Moreover, the ON-resistance of the channel at the cryogenic temperature is only one-fifth of that at room temperature. The corresponding explanations of performance trends at cryogenic temperatures are also given from the view of semiconductor physics. In addition, several device failures were observed during the dynamic characterization of GaN HEMTs at cryogenic temperatures. The ultrafast switching speed-induced high *di*/*dt* and *dv*/*dt* at cryogenic temperatures amplify the negative effects of parasitics inside the switching loop. Based on failure waveforms, two failure modes were classified, and detailed failure mechanisms caused by ultrafast switching speed are given in this article.**

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***Index Terms*— Cryogenically cooled power electronics, gallium nitride high-electron mobility transistors (GaN HEMTs), failure analysis, static and dynamic characterizations, ultrafast switching speed.**

## I. Introduction

IN CERTAIN special applications, e.g., superconducting system, the power electronics system can utilize the available coolant like liquid nitrogen to cool the converter at cryogenic temperatures, which may have a potential for efficiency and power density improvement. In this case, it is necessary to conduct investigation, characterization, and verification of components applied in power electronics systems at cryogenic temperatures. One of the key components in power electronics is power semiconductor devices.

In the previous literature, the main candidates for power devices in motor-drive systems at cryogenic temperatures were Si MOSFETs, SiC MOSFETs, and Si insulated-gate bipolar transistors (IGBTs). Based on [1] and [2], cryogenically, the SiC MOSFET suffers an obvious increase in ON-resistance of the channel, a slight decrease in breakdown voltage, and much slower switching times than that at room temperature. However, in [3] and [4], 1200-V new generation SiC MOSFET (C3M0075120K) from CREE shows a different switching loss trend with temperatures. With the temperature decreasing to 93 K, the switching loss decreases around 18.8% compared with the loss at room temperature. In comparison, the Si MOSFET shows a good trend in ON-resistance of the channel and switching performance at cryogenic temperatures [5], but the breakdown voltage of a Si MOSFET is only 60%–80% of that at room temperature [6].

GaN device is another wide bandgap power device with appealing features at room temperature. Endoh *et al.* [12] and Dogmus *et al.* [13] investigated the effects of temperature on cryogenic characteristics of gallium nitride high-electron mobility transistors (GaN HEMTs) from the point of solid-state physics. Several physics characteristics of AlGaN/GaN materials were measured from 16 to 300 K, and the strong improvement in dc and radio frequency (RF) characteristics

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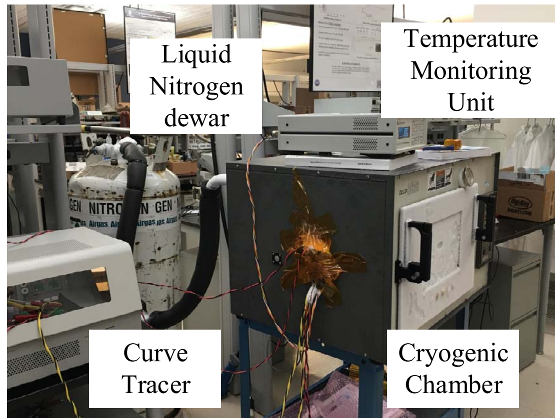


Fig. 1. Testbed setup of static characterization at cryogenic temperatures.

was observed at cryogenic temperatures, indicating the high electron mobility of two-dimensional electron gas (2DEG) and very low ON-resistance. Recently, Colmenares *et al.* [7] conducted a characterization of an Efficient Power Conversion (EPC) 200-V GaN HEMT device, and it exhibits a decreasing trend of ON-resistance at cryogenic temperatures. The conduction resistance of GaN HEMT at 70 K from EPC becomes around one-fifth of that at room temperature. The breakdown mechanism of the GaN HEMT is different from that of the Si MOSFET and is more complicated because of its lateral structure [8]–[10]. The breakdown voltage of the GaN HEMT is mainly determined by the vertical leakage current of the substrate, and therefore, it does not change at different junction temperatures. Nonetheless, the performance of higher voltage GaN devices at 650 V, which are more suitable for high-power applications, is not reported for cryogenically cooled power electronics.

This article selects a 650-V enhancement GaN HEMT GS66516T from GaN Systems for characterization. The test setup for cryogenic temperature testing, and static and dynamic characterization results are presented. The $V$–$I$ alignment method is given for data processing of the dynamic characterization since the GaN HEMT has a much faster switching speed at cryogenic temperature. Furthermore, the failure issues observed during the dynamic characterization are analyzed, and two failure modes are also classified and their related failure mechanisms are given.

This article is structured as follows. Section II introduces the testing setup for both static and dynamic characterizations at cryogenic temperatures. Also, the key points affecting the measuring accuracy in static characterization are stressed. Static characterization results are discussed in Section III, and the relevant semiconductor physics explanations are given. Section IV shows and discusses the dynamic characterization results, and the $V$–$I$ alignment, which is a key procedure of data processing, is given in detail. Section V provides the failure-mode analysis for the dynamic characterization with ultrafast switching speed. Finally, the conclusions for this article are drawn in Section VI.

This article is revised and expanded from its original form [11]. Compared with [11], this article added more details for the testing setup of static characterizations at cryogenic temperatures, and gate–source waveform's comparison with different testing wire constructions is given to illustrate its impacts on measuring accuracy. Also, $I$–$V$ curves of GaN HEMTs at different temperatures are supplemented for static characterization results. For the dynamic characterization, this article adds the illustration on how to adjust the deskew of testing voltage and current waveforms at ultrafast switching speed to achieve the accurate switching loss calculation.

## II. Test Setup for Cryogenic Temperature Characterization

The main methodology for the characterization of power devices at cryogenic temperatures is based on [5]. The test setup of static characterization is shown in Fig. 1. The chamber combined with liquid nitrogen (LN2) dewar is utilized to control the junction temperature of the device under test (DUT). DUT is not directly immersed into the liquid nitrogen in this article, and it was put inside a cryogenic chamber, and the temperature can be controlled from 298 K (room temperature) to 93 K (cryogenic temperature) with a liquid nitrogen dewar. However, if even lower testing temperature is required, DUT can be directly immersed into liquid nitrogen, reported in [4], which is 77 K. For static characterization, a curve tracer B1505A from Keysight is used to measure the output and transfer characteristics. The diagram of the detailed testing configuration is illustrated in Fig. 2(b).

Fig. 3(a) shows the test setup of dynamic characterization. For dynamic characterization, a double-pulse test (DPT) circuit is used for measuring switching loss data. The DPT circuit is placed inside the cryogenic chamber, as shown in Fig. 3(b). The gate drive, capacitor, and resistor are selected and tested for functioning properly at cryogenic temperatures for normal operation, but the load inductor and auxiliary power supply are located outside of the cryogenic chamber since they may not work properly at cryogenic temperatures. The diagram of the testing configuration for dynamic characterization is shown in Fig. 4.

One important remark in the static characterization setup is the coupling of testing wires. The curve tracer only provides Kelvin measurement for drain and source terminals, while gate–source voltage only is measured in the curve tracer side rather than the device side. Hence, wire construction with five wires, as shown in Fig. 2(a), is commonly applied for static characterization, and source sense and gate signal return share one cable. It does not cause any issue when the device is placed inside the curve tracer tank, and the cable length is short. Nonetheless, once the long cable has to be used to interconnect between the curve tracer and DUT in the chamber in this case and testing wire of the drain sense and gate terminal is twisted together, the real gate–source terminal will induce a voltage spike during the $dv/dt$ transient because of coupling effects between drain and gate wires. This can easily damage the gate–source structure of the GaN device even though a good waveform quality in the curve tracer side is displayed. In order to keep the device operation safe and for higher accuracy under a certain gate voltage, two source wires should be used for testing, as shown in Fig. 2(b). One is twisted with drain sense

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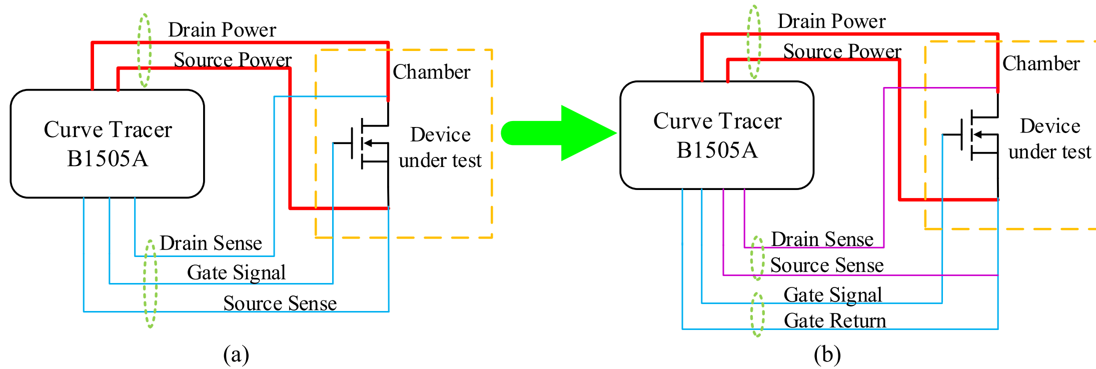


Fig. 2. Illustration of testing wires construction for static characterization. (a) Original wires construction. (b) Improved wires construction with the extra gate signal return wire.

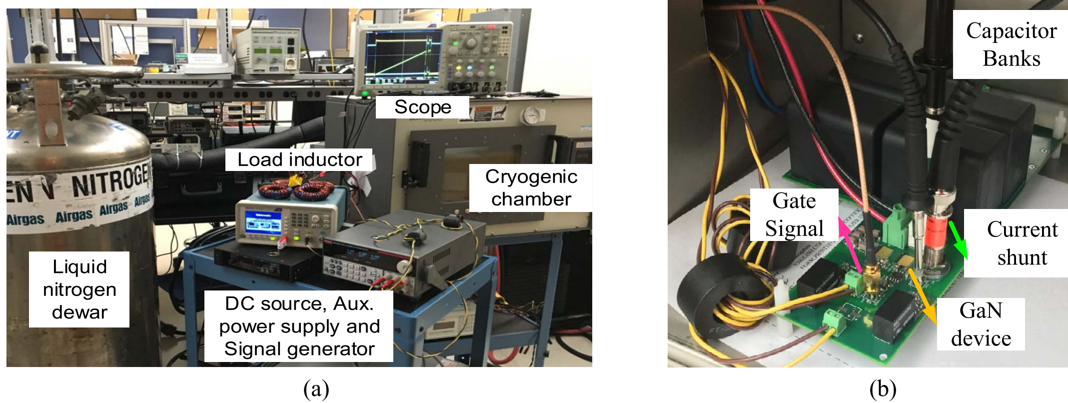


Fig. 3. Testbed setup of dynamic characterization at cryogenic temperatures. (a) Whole testbed. (b) Double-pulse testing circuits inside the cryogenic chamber.

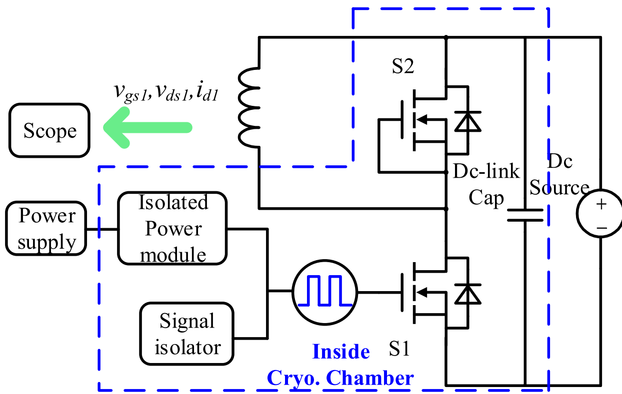


Fig. 4. Testing configuration for dynamic characterization.

wire and the other one is twisted with gate signal wire. It is similar to the printed circuit board (PCB) layout and keeps the power loop and gate loop separate. In addition, even if the gate structure is not damaged by the voltage spike, the measured transconductance will also have nonnegligible variation that can be up to 17% lower compared to the wire construction, as shown in Fig. 2(b).

Fig. 5(a) shows the real gate–source waveform of the GaN device if the testing wire of the drain and gate is twisted together, as shown in Fig. 2(a). $V_{gs}$ obviously has the voltage variation caused by the coupling during the *dv*/*dt* transient. When the testing configuration was changed to that in Fig. 2(b), $V_{gs}$ waveform is shown in Fig. 5(b). Compared with $V_{gs}$ shown in Fig. 5(a), $V_{gs}$ voltage variation has been much reduced without the coupling during the *dv*/*dt* transient.

## III. Static Characterization Results

Fig. 6 shows the transfer characteristics of the GaN HEMT at different temperatures. It can be seen in Fig. 6 that the slope of the transfer curve increases when the temperature decreases. The slope of this curve, i.e., the transconductance of the GaN HEMT shown in Fig. 7, ascends with the decrease in junction temperature. In addition, the transconductance at 93 K is 2.5 times higher than that at room temperature (296 K). This feature allows the GaN HEMT to have a much faster switching speed under cryogenic temperatures. In fact, Endoh *et al.* [12] pointed out the obvious increase in the electron velocity caused by an improvement in 2DEG mobility beneath the gate leads to the improved transfer characteristics at cryogenic temperatures.

According to Fig. 8, the conduction resistance of the device gradually decreases when the junction temperature declines. However, the speed of reduction in conduction resistance is rapid at the beginning of temperature drop, but it becomes slow around 133 K. Overall, the conduction resistance at 97 K is 5.4 mΩ, which is only around one-fifth of that at room temperature (24.8 mΩ). The reason for this trend is the increased carrier density in the 2DEG at cryogenic

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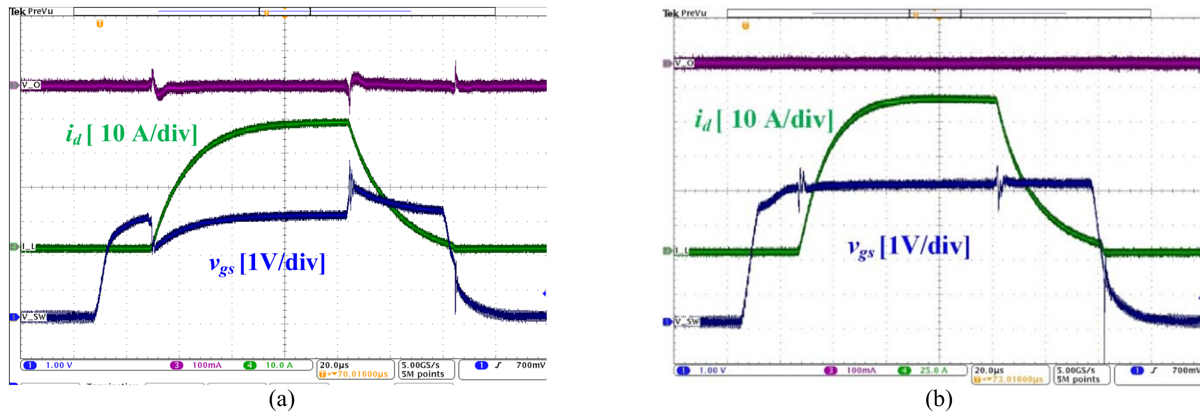


Fig. 5. Experimental gate–source waveform of 650-V GaN HEMT under static characterization (a) with the testing configuration in Fig. 2(a) and (b) with the testing configuration in Fig. 2(b).

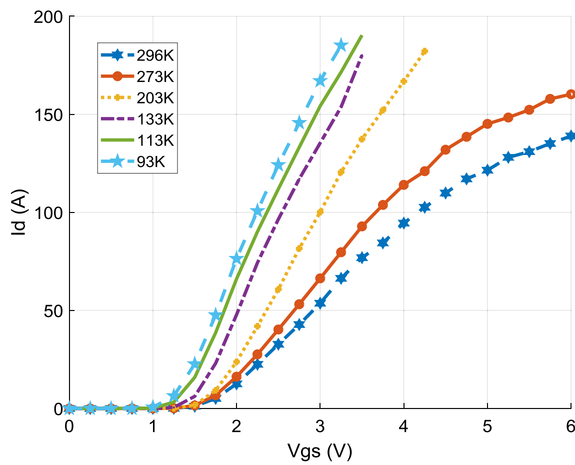


Fig. 6. Transfer characteristics of 650-V GaN HEMT at different temperatures.

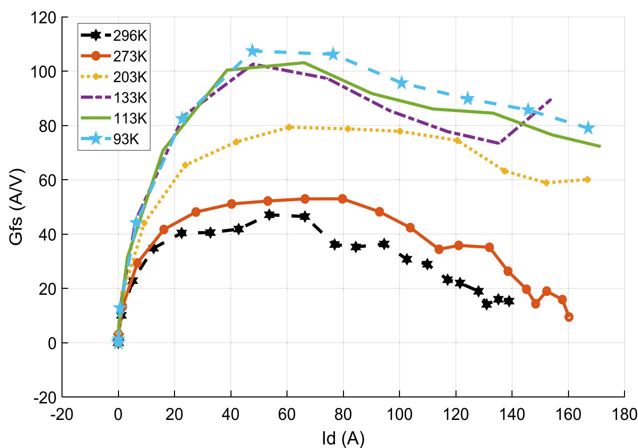


Fig. 7. Transconductance of 650-V GaN HEMT as a function of current at different temperatures.

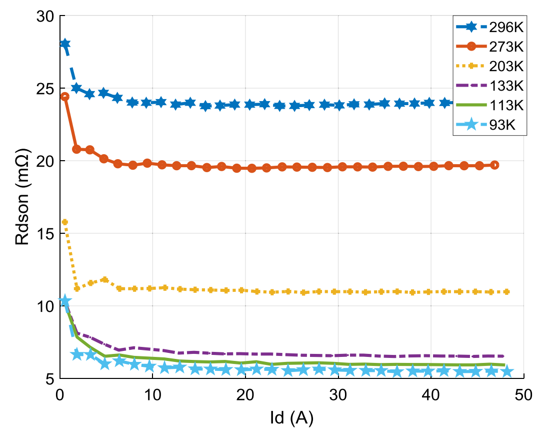


Fig. 8. ON-resistance of the channel at different temperatures.

temperatures [13]. Unlike SiC MOSFET, there is no carrier freezeout phenomenon presented in [6].

Based on [13], the higher transconductance and the lower conduction resistance at cryogenic temperatures can be attributed to the excellent combination of electron mobility and a high 2DEG carrier density below 200 K. Low interface roughness, optimized quaternary alloy barrier thickness, and high drift velocity are the reasons to get such good 2DEG properties at cryogenic temperatures, while the optical and acoustical phonon scattering are the ruling factors to determine the carrier mobility above 200 K.

As shown in Fig. 9, different from Si and SiC devices, the threshold voltage of this GaN HEMT has a positive temperature coefficient. This feature can benefit current-sharing capability among paralleled devices. For example, the device with a higher loss will result in a higher junction temperature to lead to a higher threshold voltage. As a result, the higher threshold voltage's slowing down the turn-on switching speed and increasing the turn-on delay time helps paralleled devices balance the loss.

Fig. 10 shows the output characteristics at different temperatures. The saturation current at the same gate voltage increases with the decreasing temperature. Also, the slope of drain current in ohmic-region obviously increases with the decreasing temperature, indicating a much smaller ON-resistance of GaN HEMTs' channel.

Fig. 11 shows the reverse conduction characteristics for the GaN HEMT. Even though the GaN HEMT does not have

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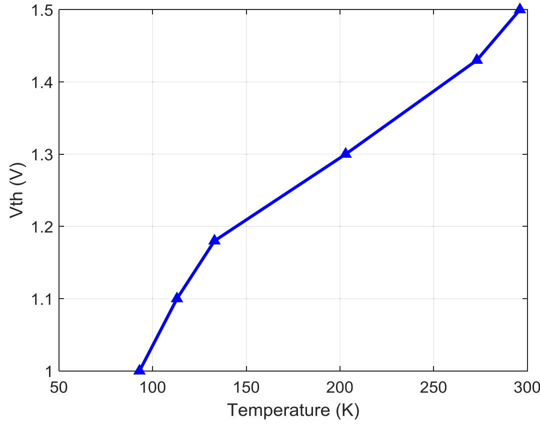


Fig. 9. Threshold voltage of the 650-V GaN HEMT as a function of temperature.

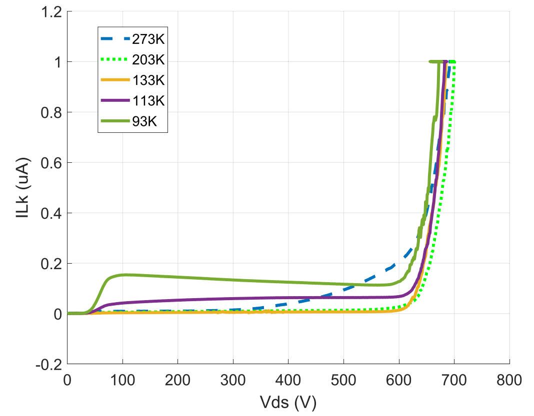


Fig. 12. Breakdown voltage the 650-V GaN HEMT as a function of temperature.

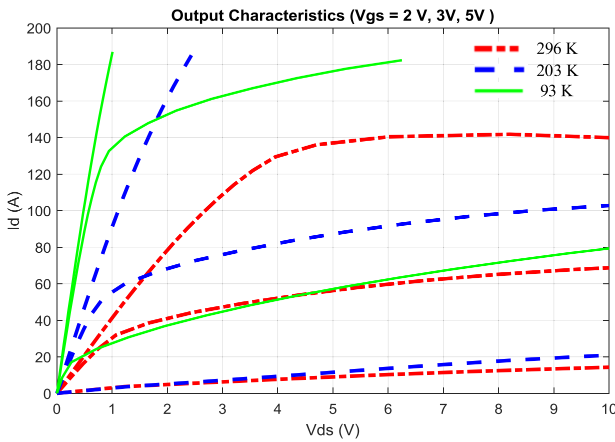


Fig. 10. Output characteristics of the 650-V GaN HEMT at different temperatures (when $v_{gs} = 2$, 3, and 5 V).

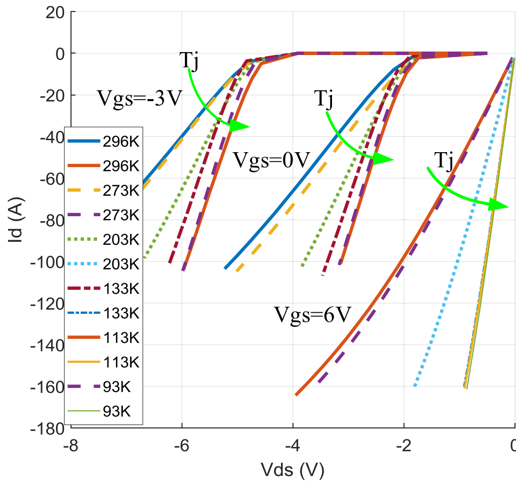


Fig. 11. Reverse conduction characteristics of the 650-V GaN HEMT at different temperatures.

a real-body diode considering the physical structure of the device, it still has a diodelike behavior (DLB) during the reverse conduction. In Fig. 11, under different temperatures, the forward voltage of the DLB is nearly the same, while the equivalent series resistance becomes lower as junction temperature decreases. For the bridge configuration, this feature will help to reduce freewheeling loss during the dead time at cryogenic temperatures.

As shown in Fig. 12, different from Si-based devices, the breakdown voltage is nearly constant under different junction temperatures, and having no degradation for breakdown voltage can help the device block rated voltage rating at cryogenic temperatures. Meneghesso *et al.* [8] identified that the GaN-to-Si substrate vertical leakage current, independent of temperature, limits the maximum breakdown of the AlGaN/GaN HEMTs on Si.

## IV. Dynamic Characterization Results

At cryogenic temperatures, the switching speed of the GaN HEMT becomes much faster than that at room temperature. As discussed before, the transconductance at 133K is 2.5 times as large as that at room temperature. Fig. 13 shows the comparison of measured results of *di/dt* at room temperature and cryogenic temperature. The *di/dt* at 133 K is 21 A/ns, which is two times higher than that at 279 K. In addition, *dv/dt* during switching at 133 K is 83.3 V/ns, which is also around twice larger than one at room temperature.

Such a high switching speed causes two issues. The first one is how to conduct $V$–$I$ alignment or deskew adjustment between measured $v_{ds}$ and $i_d$, which is the key procedure to realize accurate switching loss data evaluation. According to [14], even if the timing misalignment is as small as 2 ns, it causes a 50% error compared with the correct one. To relieve this issue, a $V$–$I$ alignment method for switching waveforms is applied based on [15]. The basic idea is to utilize the initial transient voltage dip of $v_{ds}$ for $V$–$I$ alignment during the current rise up (*di/dt* period). Before the device's arriving in the ohmic region from the saturation region shown in Fig. 14, the drain–source voltage can be expressed as

$$v_{ds} = V_{dc} - i_d R_{shunt} - L_{loop} \frac{di_d}{dt} \qquad (1)$$

where $V_{dc}$ is the dc-link voltage, $R_{shunt}$ is the resistance of the coaxial shunt, $L_{loop}$ is the power loop inductance, and $i_d$ is

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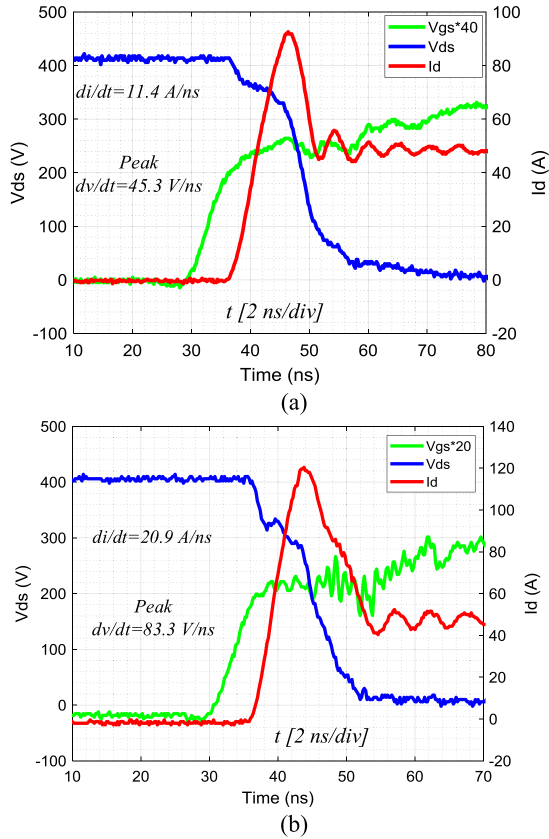


Fig. 13. *di/dt* and *dv/dt* comparison under 400 V and 50 A (a) at room temperature and (b) at cryogenic temperature.

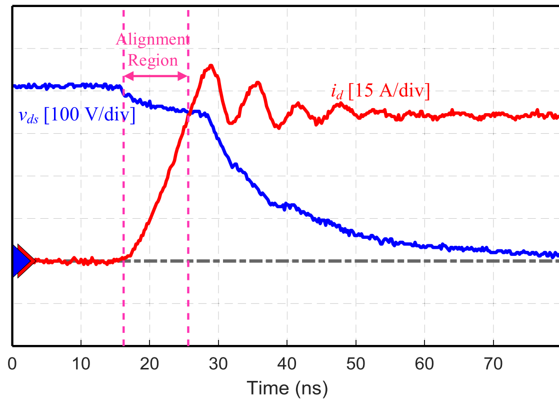


Fig. 14. Zoomed-in view of testing waveform for $V$–$I$ alignment illustration.

the measured drain current. Power loop inductance $L_{\mathrm{loop}}$ can be obtained based on the resonant frequency of drain–source voltage during turn-off since the resonant frequency is determined by $L_{\mathrm{loop}}$ and $C_{\mathrm{loss}}$ (at 400 V). Fig. 15 shows that the resonant period of voltage oscillation during turn-on is 8.2 ns. Considering $C_{\mathrm{loss}}$ (at 400 V) of selected GaN HEMT is 130 pF, $L_{\mathrm{loop}}$ is calculated as 13.1 nH in total (also including the parasitic inductance of coaxial shunt).

With the calculated $L_{\mathrm{loop}}$ and time-domain $i_{\mathrm{ds}}$, the calculated $v_{\mathrm{ds}}$ waveform based on (1) can be obtained to compare with the measured $v_{\mathrm{ds}}$ waveform. The observation of overlaps

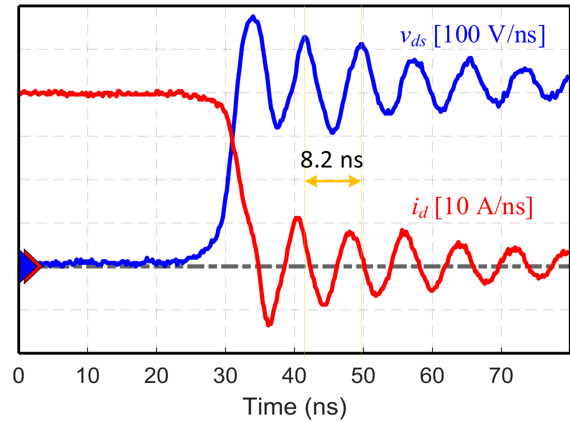


Fig. 15. Zoomed-in view of turn-off waveform for extraction of $L_{\mathrm{loop}}$.

between the calculated and measured waveforms is used to adjust the deskew and to correct misalignment timing. The deskew here is defined as the time difference between $i_d$ and $v_{\mathrm{ds}}$ waveforms, and Fig. 16 illustrates how to use this method to adjust $V$–$I$ alignment. In Fig. 16(a), it is obvious that the calculated $v_{\mathrm{ds}}$ is offset to the right compared with the measured one with 2-ns deskew. Vice versa, as shown in Fig. 16(b), the calculated $v_{\mathrm{ds}}$ is obviously offset to left compared with the measured one with −2-ns deskew. The offset can be corrected by shifting $i_{\mathrm{ds}}$, and Fig. 16(c) shows the final corrected deskew adjustment of 0.6 ns, in which the calculated and measured $v_{\mathrm{ds}}$ waveforms properly match.

Table I further gives the loss calculation comparisons between three deskews to illustrate the importance of $V$–$I$ timing alignment in the measurement for ultrafast switching speed applications. Without correct $V$–$I$ alignment, the switching loss data error can be up to 16% compared with the correct one.

The second issue is ultrafast switching speed-induced device failure because of high sensitivity to parasitics. The detailed failure modes will be analyzed in Section V. Since several failures were observed under dual-GaN HEMT bridge configuration, the testing configuration changed from that in Fig. 17(a) to that in Fig. 17(b) by substituting GaN HEMT with the SiC diode C3D16065A from CREE whose voltage rating is also 650 V. SiC diode-based bridge can avoid the shoot-through problem and device failure problem. The following loss data are also from this SiC-diode-based bridge setup.

Fig. 18 shows the loss comparison at different junction temperatures. The parameters employed by the gate drive in the test are: turn-on resistance is 20 Ω, turn-off resistance is 2 Ω, and the gate drive IC is Si8271 from Silicon Labs. Since the gate driver IC cannot work properly below the temperature of 133 K, the loss data are only given until 133 K. Fig. 18(a) shows that the turn-on loss descends with the decease in junction temperature. When the test condition is under 400-V bus voltage and 40-A load current, the turn-on loss is 177.5 $\mu$J at 133 K, while it is 277.7 $\mu$J at 298 K. The turn-on loss is reduced by 36% at 133 K compared with that at room temperature. For the turn-off loss, due to the lower threshold voltage, the turn-off loss increases slightly at 133 K compared

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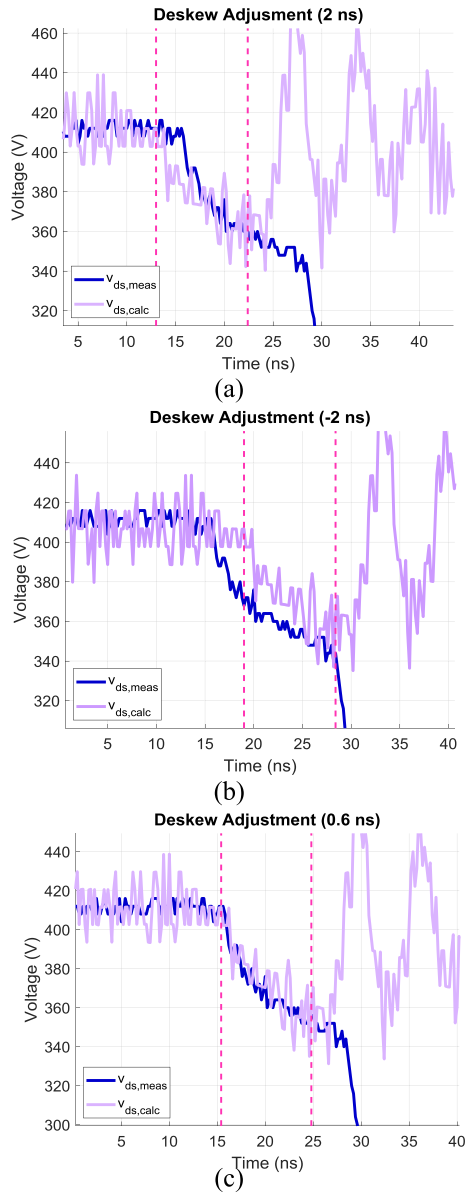



Fig. 16. $V$–$I$ alignment with different deskews between $v_{ds}$ and $i_d$.

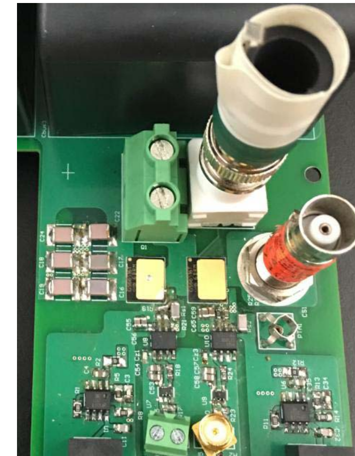
TABLE I
SWITCHING LOSS COMPARISONS AT DIFFERENT $V$–$I$ TIMING ALIGNMENTS

| Deskew (ns) | Eon (μJ) | Eoff (μJ) |
|---|---|---|
| 2 | 253.9 | 36 |
| -2 | 285.7 | 15.2 |
| 0.6 | 212.9 | 66.7 |

with that at room temperature. In the end, the total switching loss, dominated by the turn-on loss at 133 K, can be reduced by 29.8% compared with that at room temperature.

## V. FAILURE ANALYSIS WITH ULTRAFAST SWITCHING SPEED

As stated in Section IV, several GaN HEMT failures were observed during dynamic characterization with dual-active switch bridge configuration due to high *dv*/*dt* and *di*/*dt*. High


(a)

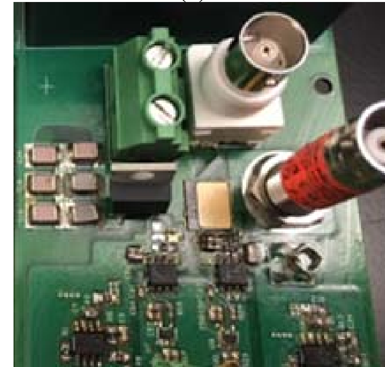

(b)

Fig. 17. DPT circuits configuration. (a) Upper device is a GaN device. (b) Upper device is a SiC diode.

*dv*/*dt*- and *di*/*dt*-induced different false turn-on mechanisms were reported in [16] and [17]. For high *dv*/*dt*-induced failure, the main reason is that the high *dv*/*dt* produces displacement current flowing through the Miller capacitance and gate resistance, which makes gate voltage exceed the threshold voltage and causes shoot-through [16]. In addition, based on [17], due to high *di*/*dt*, even though the device package has very small common source inductance (CSI) $L_{ss}$, it may still false trigger the device, but this high *di*/*dt*-induced false trigger only happened in the turn-off transition of the active switch. However, under the testing at cryogenic temperatures, ultrahigh *di*/*dt* can also cause amplified gate voltage oscillation and breakdown the gate structure with overstressed gate voltage even in the turn-on transition of the active switch. In this section, two typical failing waveforms are given at cryogenic temperatures with the high-side GaN HEMT configuration to illustrate the failure mechanisms.

It is obvious that a shoot-through current, much larger than the inductor current, occurred during the turn-on transient. Fig. 19(b) shows the detailed zoom-in waveform during the turn-on transient. As can be seen, the peak *dv*/*dt* arrived at 86.7 V/ns. Fig. 19(c) displays the equivalent circuits of DPT circuits during *dv*/*dt* transients. The high *dv*/*dt* will induce a displacement current by Miller capacitance going through the internal gate resistance of the upper switch. The GaN device (GS66516T) used in this article has a 1.5-Ω internal gate

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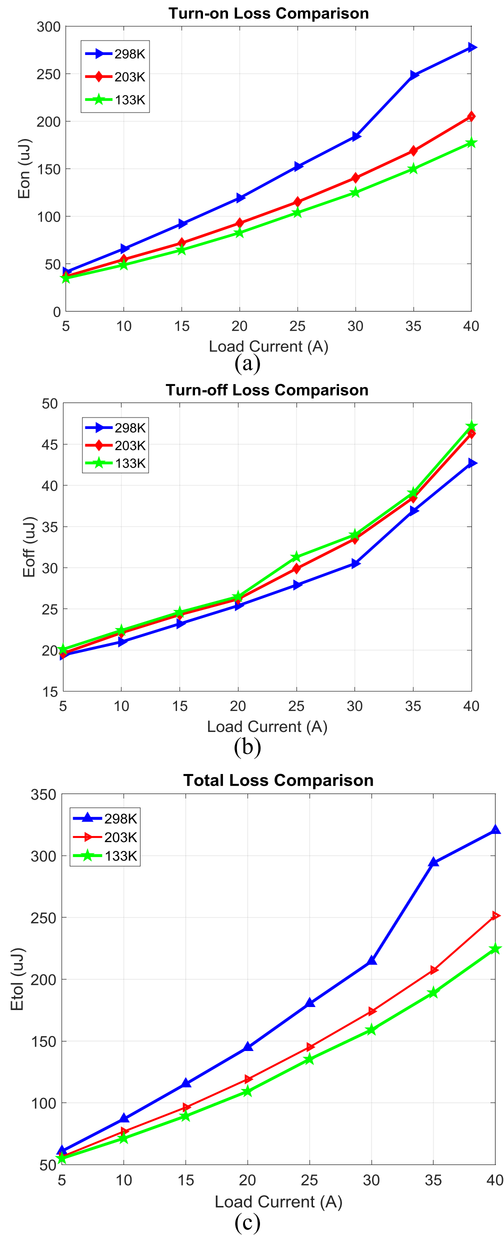


Fig. 18. Loss comparison under different junction temperatures. (a) Turn-on loss. (b) Turn-off loss. (c) Total switching loss.

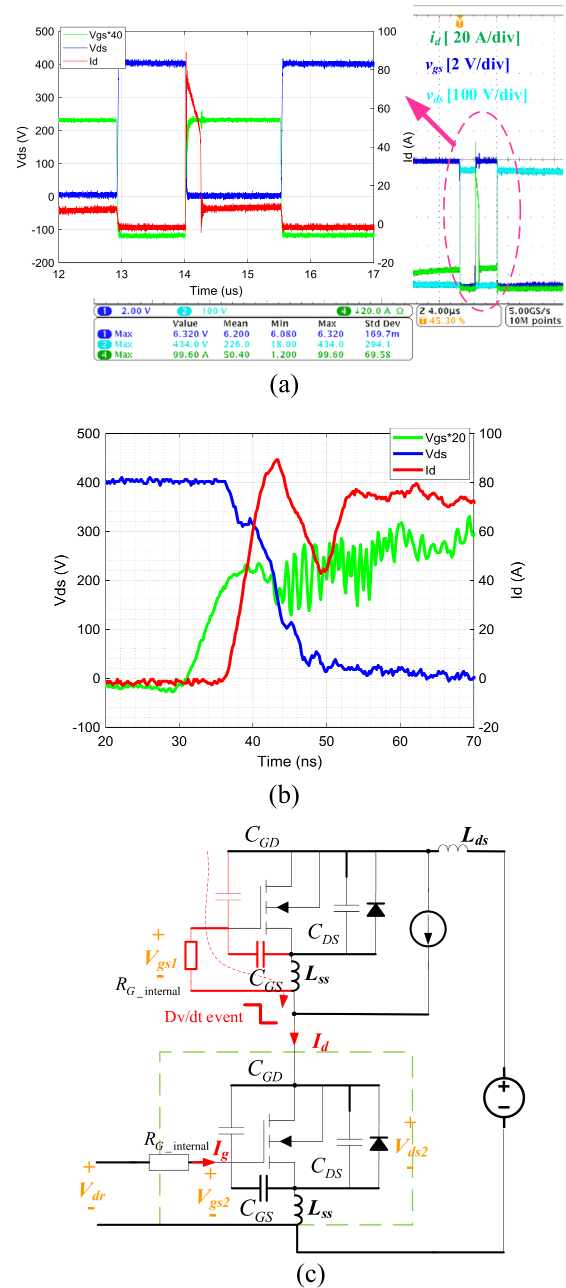


Fig. 19. Illustration of high *dv*/*dt*-induced false turn-on. (a) DPT waveform under cryogenic temperature with shoot through under a short transient. (b) Zoomed-in view of DPT waveform. (c) Circuits illustration for the induced false turn-on.

resistance. Once the induced voltage $v_{gs}$ in Fig. 19(c) by *dv*/*dt* exceeds the threshold voltage of the gate, the upper device would falsely turn-on causing a short time shoot-through.

In Fig. 20(a), ultrahigh *di*/*dt* at cryogenic temperatures caused an overvoltage issue for the gate structure of the GaN HEMT leading to a device damage issue. The main difference compared with that in Fig. 19(a) is $v_{gs}$ waveform, and it has an obvious voltage spike during turn-on, while $v_{gs}$ has no overshoot during turn-on as shown in Fig. 19(a). The GaN device (GS66516T) used in this article does not have a Kelvin source connection because of the top cooling design. Assuming $L_{ss}$ is only 0.5 nH for this GaN HEMT, the *di*/*dt*-induced voltage across $L_{ss}$ is still as high as 11 V.

This induced voltage of CSI can impact the gate loop to cause overshoot of the gate voltage or cause gate loop oscillation, as shown in Fig. 20(b). Fig. 20(b) shows the peak $v_{gs}$ during the *di*/*dt* transition arrived at 15.6 V, having exceeded the maximum breakdown gate voltage of the GaN HEMT. This may overstress the gate structure of the GaN HEMT and ultimately lead to device damage. In the experiments, once the junction temperature was decreased to 133K, it would easily damage the upper device after several DPTs.

Photographs of failed devices are shown in Fig. 21. There are no obvious marks of damage both at the top or bottom side of damaged devices, and with measurement, all gate to source are shorted.

The trend of the switching speed with temperature variations is mainly determined by a semiconductor material itself, so all GaN HEMTs will possibly achieve a much faster switching

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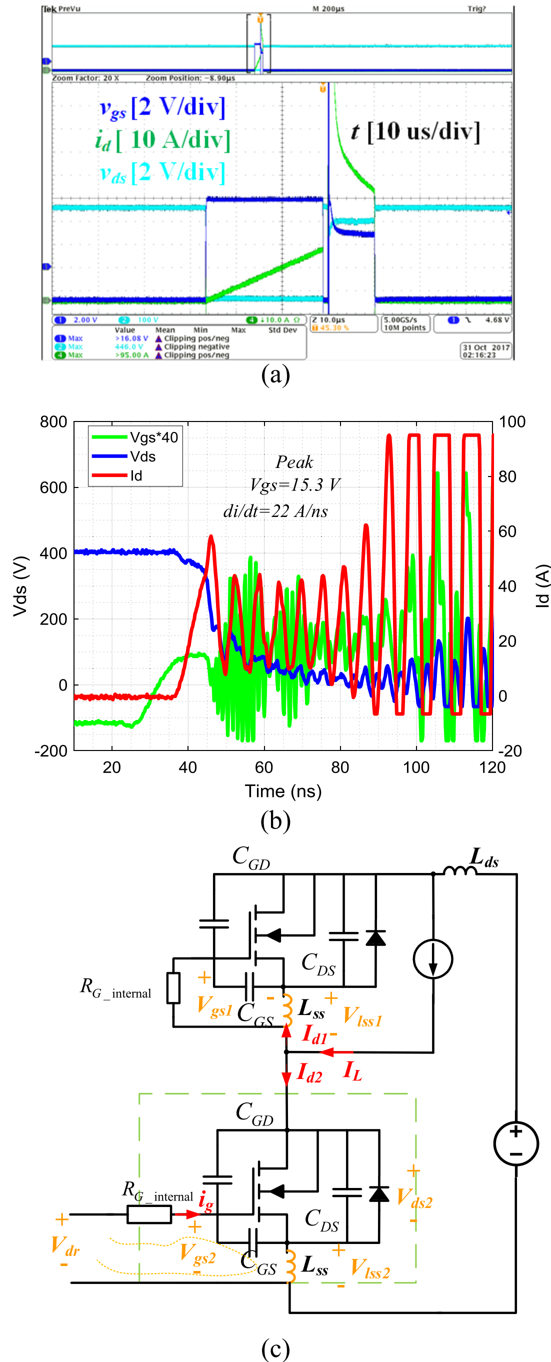


Fig. 20. Illustration of high *di*/*dt*-caused gate damage. (a) DPT waveform under cryogenic temperature with overvoltage of gate–source voltage. (b) Zoomed-in view of DPT waveform. (c) Circuits illustration for the induced $v_{gs}$ overvoltage issue.

speed at cryogenic temperatures due to 3–5 times higher transconductance compared with that at room temperature. The uncertain factor is the package of GaN HEMTs from different manufacturers could be different. If the parasitic CSIs of packages from other companies are similar to GS666516T's package shown in Fig. 21, the same failure mechanisms can happen, and the same failure analysis can also be applied. On the contrary, if a more advanced package of GaN HEMTs is developed, this failure mechanism could be avoided. However, it could be very difficult to develop such a good package since even a small 0.5-nH CSI can induce an overstressed gate voltage (∼11 V) with 22 A/ns *di*/*dt*.

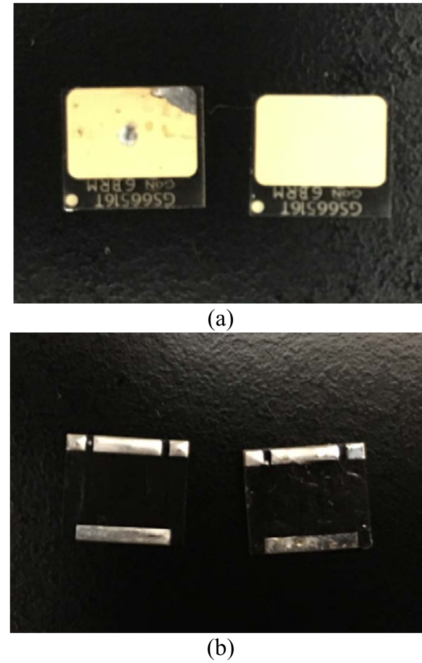


Fig. 21. Photographs of failed devices. (a) Topside. (b) Bottom side.

Those ultrafast switching speed-induced failures indicate that only having an ideal switch is not enough. When the switching speed becomes faster and faster, the high sensitivity of parasitics will render gate drive design, packaging, and PCB layout more challenging and difficult. For the package design, a kelvin connection of source terminal should be used for this application and shared common trace or wire bond between the gate loop and the power loop inside the package should be also avoided to achieve a CSI as low as possible. For the gate drive design, a clear separation of layouts between the power loop and the gate loop should be paid attention to. Also, some advanced gate technologies such as active Miller clamp and *dv*/*dt*, *di*/*dt* active control can be applied to avoid device failures. All those aspects require careful investigations in future work.

## VI. Conclusion

This article presents a characterization of the 650-V enhancement GaN HEMT at cryogenic temperatures, including the static and dynamic characteristics. One setup issue in static characterization is the overshoot of gate–source voltage caused by coupling effects between the gate and drain testing wires. The method to eliminate this issue is to separate the gate and power loops, which is realized by not twisting the gate and drain measurement wires. Based on the characterization results, the 650-V enhancement GaN HEMT is a promising candidate in cryogenically cooled power electronics converters. At cryogenic temperatures, the switching loss can be reduced by about 30%, and the conduction loss is also decreased with only 25% ON-resistance compared with that at room temperatures. However, due to extremely fast switching

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speed at cryogenic temperatures, the high *dv/dt*-induced self-turn-on and high *di/dt*-induced gate voltage overshoot of the upper device can be observed, and related failure mechanisms are analyzed. Displacement current induced by high *dv/dt* going through Miller capacitance can falsely turn on the device, while the overvoltage, across the gate–source, caused by the voltage drop of CSI with high *di/dt*, can damage the gate structure and the device. Hence, considerations in gate drive and packaging design for cryogenic temperatures should be conducted further to adapt to an ultrafast switching speed.

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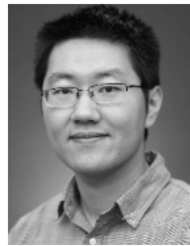

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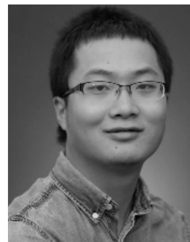

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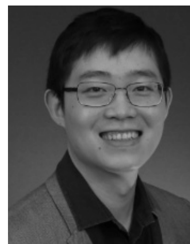

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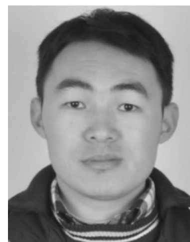

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