

Improved Lifetime of GaN-Based Single Phase PV Inverter Using Dynamic Hardware Allocation

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Abstract—Power electronic inverters for photovoltaic (PV) systems over the years have trended towards high efficiency and power density. However, reliability improvements of inverters have received less attention. Inverters are one of the lifetime-limiting elements in most PV systems. Their failures increase system operation and maintenance costs, contributing to an increased lifetime energy cost of the PV system. Opportunities exist to increase inverter reliability through design for reliability techniques and the use of new modular topologies, semiconductor devices, and energy buffering schemes. This paper presents the implementation and design for reliability for a GaN-based single-phase residential string inverter using a new topological and control scheme that allows dynamic hardware allocation (DHA). In the proposed inverter architecture, a range of identical modules and control schemes are used to dispatch hardware resources within the inverter to variably deliver power to the load or filter the second harmonic current on the DC side. This new approach more than triples the lifetime of GaN-based inverters, reducing system repair/replacement costs, and increasing the PV system lifetime energy production.

Index Terms—Single-phase inverter, boundary current mode (BCM), gallium nitride (GaN), design for reliability (DfR), zero voltage switching (ZVS).

I. INTRODUCTION

With recent advancements in power semiconductor technology, such as Gallium Nitride (GaN) and Silicon Carbide (SiC) transistors, power converters for PV applications have been able to reach a peak power efficiency of 99% and achieve a power density of 243 W/in³ [1–3]. Despite these achievements, the reliability of PV inverters has been a limiting factor in PV systems, leading to significant downtimes [4]. PV converter topologies are depicted conceptually in Fig. 1. Traditional PV converter topologies are implemented using single-purpose power stages and passives as shown in Fig. 1a with bulky electrolytic capacitors used to decouple the double-line-frequency power. However, the inverter reliability and lifetime evaluation are impacted by the DC-link capacitor and power devices [5]. When used, electrolytic capacitors are the dominant component limiting the lifetime of the inverter. Longer lifetimes are obtained when power filtering is accomplished without the use of bulk electrolytic capacitors [6]. To address reliability challenges, a common approach is to use some type of active power filter (APF), as depicted in Fig. 1b, to reduce the required capacitance thus allowing the

use of more reliable film or ceramic capacitors. Following the elimination of bulk electrolytic capacitors, further improvement of inverter lifetime requires consideration of the overall system architecture including power devices.

To address these shortcomings of PV inverters, a new topological and control scheme using the concept of dynamic hardware allocation (DHA) is introduced and illustrated in Fig. 1c. In the proposed converter implementation, a common set of hardware resources shift operation between different conversion functions dynamically in time. Note that this is not a static, integrated topology which has dedicated pathways for each; instead, the system consists of a pool of identical modules that can be dispatched to perform a specified function, principally active power filtering (APF: double-line-frequency decoupling) and line frequency inverter operation. In addition, available modules can be reassigned in the event of a single failure of any element.

The benefit of this approach is multifold. First, the inverter lifetime and reliability are increased substantially because the pooled hardware resources can be re-assigned in the event of a single failure of any element. In the traditional architecture, Fig. 1(a-b) any semiconductor element is often a single point of failure (SPOF). If an inverter transistor fails, the system can no longer supply power to the grid. In the DHA scheme, if a transistor that is currently performing dc-ac inversion fails, the failure can be isolated and hardware resources are re-routed from alternate functions to replace it. The modular nature of the system facilitates the use of high-reliability components, and allows for simple repair or maintenance through replacement of individual modules instead of requiring a complete inverter replacement. The operation of the proposed inverter architecture is further discussed in Section II, followed with the converter loss and reliability model in Section III. The DHA design for reliability is illustrated in Section V. The experimental prototype and results are presented in Section VI. Finally, the conclusions and future works are stated in Section VII.

II. OPERATIONAL CONCEPT

The proposed multiphase single-phase BCM inverter architecture using the DHA scheme is shown in Fig. 2. This implementation consists of three high frequency (HF) phases/modules and a single line-frequency (LF) return phase.

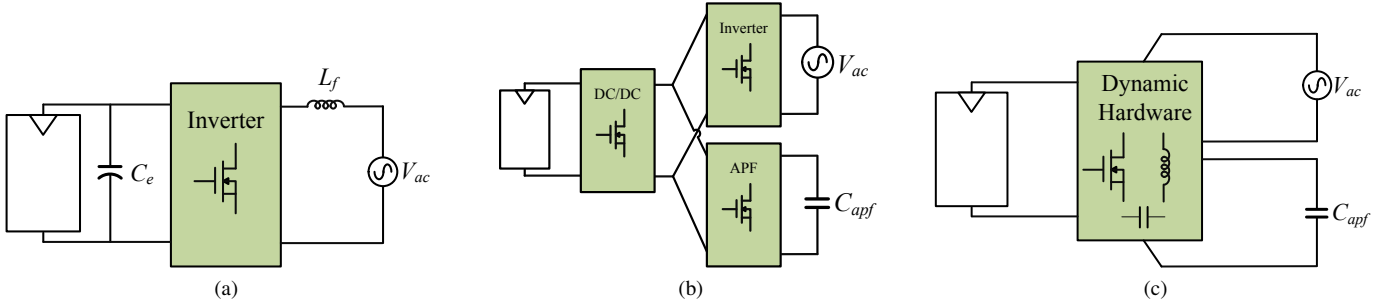


Fig. 1. Conceptual PV converter topologies (a) traditional electrolytic-decoupled string inverter; (b) generalized diagram of APF-based system; (c) dynamic hardware-based (DHA) system.

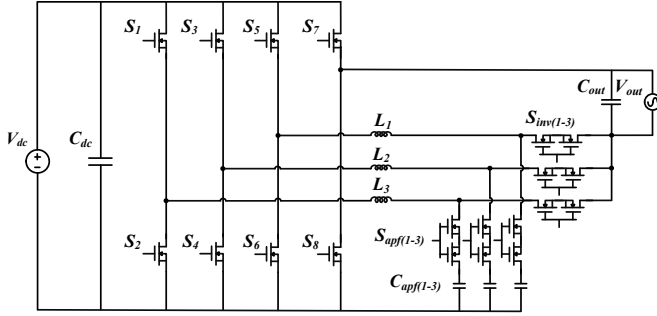


Fig. 2. Proposed DHA inverter topology.

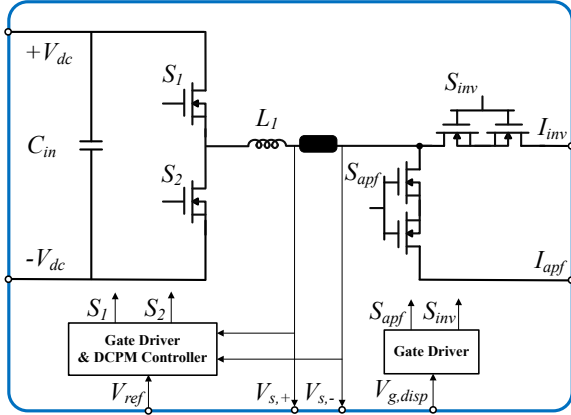


Fig. 3. DHA inverter single module.

A schematic of a single HF module is depicted in Fig. 3. Each of these modules is a zero-voltage switching half-bridge employing a dual-current programmed mode (DCPM) control [7, 8] with a low-frequency reference V_{ref} to achieve boundary current mode (BCM) switching [9]. The pair of switches S_{inv} and S_{apf} control the hardware allocation, allowing the module to function as an inverter, shunt APF, or idle.

The DHA approach exhibits all the potential advantages of a traditional soft-switching multiphase converter: current sharing among modules, phase shedding, and ripple cancellation. In addition, the DHA is able to dynamically dispatch each high frequency module to either APF or inverter operation. In an example case, the DHA may use the majority of the modules

for inverter operation during the peak output current, and the majority for APF operation during the output current zero-crossing to reduce peak current stresses. When the dispatching scheme is optimized, DHA has the potential to improve both the efficiency and lifetime of a non-DHA implementation with the same hardware. The power loss and reliability model are derived next and used to design the DHA inverter with BCM operation.

III. CONVERTER LOSS MODEL

The dominant loss mechanisms in the converter include inductor core and winding loss in addition to device switching and conduction loss. Other forms of loss do not vary significantly and have not been considered in this model.

A. Switching Frequency

The switching frequency in the unipolar switched BCM inverter varies along the line cycle and is at its maximum near the zero crossings. The resulting frequency can reach values in the MHz range, so it is important to limit the frequency to a range that guarantees noise immunity and a good performance of the control [7, 8]. Thus, a minimum ON/OFF time of 200 ns and a maximum switching frequency of 800 kHz are selected, based on the hardware design in [9]. These limits constrain the selection of inductance and the reverse conduction current required to achieve ZVS. For an inductance of 20 μH , Fig. 4 shows the relationship between the ZVS current and the switching frequency for a given average inductor current. For instance, for an average inductor current above 3.5 A, the reverse conduction current can be set to a minimum of 1.1 A to achieve ZVS while keeping the switching frequency to below 800 kHz. Near the output current zero-crossing, where the current is at its minimum, the minimum ZVS current needs to be extended to 3 A to limit the switching frequency.

Using BCM modulation, ZVS is achieved throughout the line cycle; the remaining switching losses are primarily turn-off losses. For GaN-GIT devices, the turn-off loss can be estimated using the model developed in [10] for ZVS GaN-GIT devices operating in the low and high-frequency half-bridges.

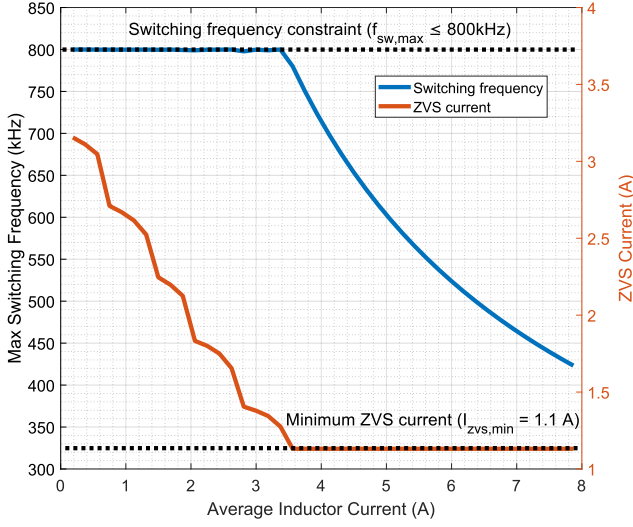


Fig. 4. Relationship between the ZVS current I_{zvs} and maximum switching frequency for a given average output current I_{out} .

B. Magnetic Loss

Given the modular nature of the system, low-profile PCB trace winding planar magnetics are employed in this design. For planar inductor design, the winding loss including the effect of skin and proximity effect in a particular layer is given by Dowell's equation [11, 12]. However, in a multi-layer winding, where the copper thickness h is less than the skin depth of the conductor δ , the proximity effect is often the dominant form of loss, and increases rapidly with frequency. The winding loss can be approximated as

$$P_w = I_{rms}^2 \cdot R_{dc} \cdot \left[1 + \frac{(\pi N_s)^2 \cdot h^6}{192 \cdot \delta^4 \cdot b^2} \right] \quad (1)$$

where I_{rms} is the expected inductor RMS current, N_s is the number of turns per section, and b is the breadth of the winding [13]. Furthermore, the ac resistance of the winding is estimated using a finite element analysis tool and measured experimentally with an impedance analyzer. After surveying available planar cores for high power, high-frequency applications, the EI38 planar core geometry with the high frequency core material 3F36 from Ferroxcube are considered to implement the inductor. The core parameters are summarized in Table I.

The core loss P_{fe} is estimated using the Steinmetz Equation for every switching period and averaged over the line cycle,

TABLE I
INDUCTOR CORE PARAMETERS

Core Type	Material	A_c (cm^2)	MLT (cm)	l_m (cm)	V_{ol} (cm^3)
EI38	3F36	1.94	6.6	4.37	8.46

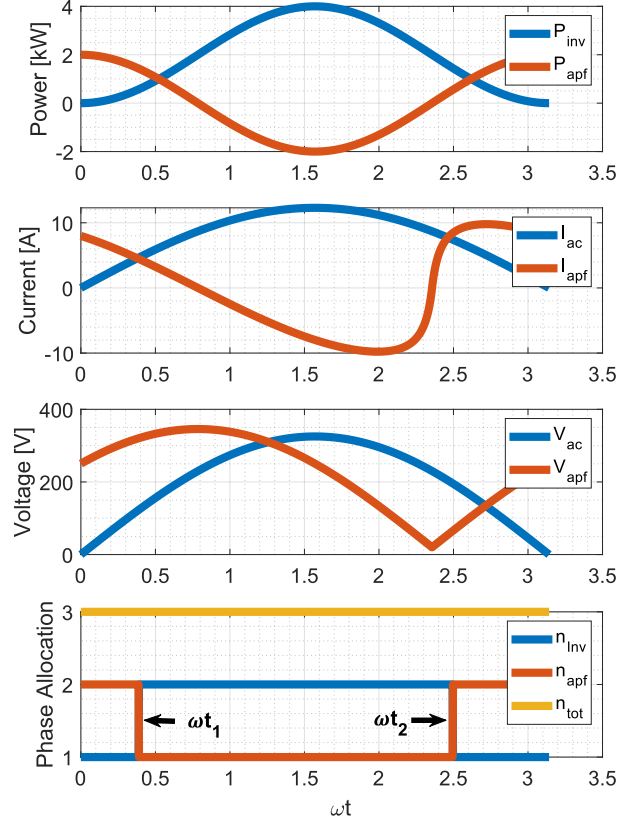


Fig. 5. Analytical waveform showing inverter and APF power (P_{inv} , P_{apf}), average output AC current and APF current (I_{ac} , I_{apf}), average output AC voltage and APF capacitor voltage (V_{ac} , V_{apf}) and phase allocation (n_{inv} , n_{apf}) for a 3 module 2 kW DHA system.

$$P_{fe} = \frac{2A_c \cdot l_m}{\pi} \int_0^\pi (K \cdot f_s(\theta)^\alpha \cdot \Delta B(\theta)^\beta) d\theta \quad (2)$$

where A_c represents the core cross-sectional area and l_m is the mean magnetic path length. The core material parameters K , α , and β are provided by the core manufacturer.

C. Phase Allocation

With the module-level power loss model developed, the device and magnetic loss model are used to determine the allocation that would yield the lowest converter loss for a given number of phases. In this analysis with a total of 3 HF modules ($n = 3$), a simple search algorithm loops through the total number of modules and computes the losses for each possible allocation, at each point in the line cycle.

Fig. 5 shows the analytical waveform of the powers, currents and voltages in an inverter and APF operation with its subsequent phase allocation during the positive half cycle. This plot is based on a unity power factor for a 2 kW average power system, an output voltage of $240 V_{rms}$ at 60 Hz and an APF capacitor value of $100 \mu F$ which is enough to meet

the energy and capacitance requirements to buffer the second-harmonic ripple power on the DC side [14]. Starting at $\omega t = 0$, there are 2 modules locked into APF operation ($n_{apf} = 2$) while one module is allocated for inverter ($n_{inv} = 1$). At $\omega t = \omega t_1$, the allocation switches to 2 phases in inverter mode ($n_{inv} = 2$) while only one phase is in APF mode ($n_{apf} = 1$) throughout the peak inductor current. At $\omega t = \omega t_2$, when APF is transitioning to peak APF current, the allocation switches back to $n_{apf} = 2$ and $n_{inv} = 1$. All waveforms are identical in the negative half-cycle. In the case of Non-DHA scheme, the multiphase inverter consists of 4 HF modules ($n = 4$) with two phases locked in inverter mode ($n_{inv} = 2$) while the remaining two phases perform APF operation ($n_{apf} = 2$). The allocation is static and does not change throughout the line cycle.

IV. RELIABILITY MODEL

The reliability of power converters depends heavily on the performance of each component in the converter. According to operational field data, components such as power devices, capacitors, gate drivers, and fans are generally responsible for failures in PV inverters [15]. However, the power semiconductor devices and capacitors have been reported in [5, 16, 17] and [18] as the main lifetime limiting components of the system. Therefore, this analysis only considers the reliability model of power devices and DC-link capacitors.

A. Lifetime Model of DC-Link Capacitors

From a PV inverter reliability standpoint, Metallized Polypropylene Film Capacitors (MPPF-Caps) have a well-balanced performance in comparison to Aluminum Electrolytic Capacitors (Al-Caps), which are widely considered as the most unreliable component in inverters [17, 19, 20]. The two stress factors that have a huge influence on capacitor reliability are operating temperature and voltage. The lifetime of the capacitor rapidly degrades as its hot spot temperature increases. The lifetime model of capacitors used in this work is

$$L_c = L_0 \times \left(\frac{V}{V_0}\right)^{-n} \times 2^{\frac{T_0 - T}{10}} \quad (3)$$

where V_0 , L_0 and T_0 are the rated voltage, lifetime, and temperature respectively under manufacturer testing conditions. V is the voltage and T is the temperature at operating condition. n is the voltage stress exponent and can be around 7 to 9.4 for MPPF Caps [21]. Table II summarizes the film capacitor parameters from KEMET corporation used in this model.

B. Lifetime Model of Silicon Power Devices

Silicon power semiconductor devices have been in use for many years, resulting in a wealth of operational and test data to accurately model their lifetime. Failure mechanism and stress factors have been studied extensively and are well understood. Thermo-mechanical stress from temperature cycles resulting in failures including bond wire lift-off, and base plate solder failure have been determined to be the main

TABLE II
PARAMETERS OF THE FILM CAPACITOR LIFETIME MODEL

Parameter	Label	Value
Rated Lifetime	L_0	100,000 hours
Rated Voltage	V_0	650 V
Rated Temperature	T_0	70 °C
Operating Voltage	V_{dc}	400 V
Max. Operating Temperature	T	60 °C

cause of failure in silicon power devices such as IGBTs. Several empirical lifetime models such as LESIT, BAYERER, and SEMIKRON solely derived from empirical data for silicon devices have demonstrated to yield good lifetime estimations [22–24]. These models are expressed as equations for the number of cycles to failure (N_f). The SEMIKRON model

$$N_f = A \cdot (\Delta T_j)^\alpha \cdot ar^{\beta_1 \cdot \Delta T_j + \beta_0} \cdot \left(\frac{C + t_{on}^\gamma}{C + 1}\right) \cdot e^{\frac{E_a}{k_B \cdot T_{j,m}}} \cdot f_{diode} \quad (4)$$

introduced in [23] is used to estimate the number of cycles to failure of the Silicon power MOSFET. $T_{j,m}$ is the absolute mean junction temperature, ΔT_j is the junction temperature swing, and t_{on} is the cycle period. The lifetime consumption (LC) of the device is calculated using Miner's rule

$$LC = \sum_i n_i / (N_f)_i \quad (5)$$

where n_i is the number of cycles per year. The device reaches end of life when LC is unity [25].

C. Lifetime Model of GaN-GIT Power Devices

With the recent push for the wide adoption of SiC and GaN power devices, lifetime models for Silicon power devices have been used to estimate their reliability, often leading to erroneous estimation [26]. Having lifetime models based solely on wide bandgap power modules is essential to accelerate their worldwide acceptance. According to reliability analysis in [27], temperature, voltage, and current are the three stress factors that are essential in evaluating the switching lifetime of GaN FET. However, based on the switching lifetime evaluation for Hybrid Drain-embedded Gate Injection Transistor (HD-GIT) in [28] developed by Panasonic Corporation, the switching lifetime of their device depends strongly on the peak drain current I_{DP} and voltage V_{DD} . The HD-GIT switching lifetime (τ) is

$$\tau(V_{DD}, I_{DP}) = A \cdot \exp[-(\beta_v \cdot V_{DD} + \beta_c \cdot I_{DP})] \quad (6)$$

where β_v is the voltage acceleration factor and β_c is the current accelerated factor. The acceleration factor test of the voltage V_{DD} and current I_{DP} on the lifetime yielded that $\beta_v = 0.039$ and $\beta_c = 0.47$. A is a constant factor approximately equal to $1e15$. During every switching action, V_{DD} and I_{DP} reduce the switching lifetime of the device by

$$\Delta\tau(V_{DD}, I_{DP}) = \frac{1}{\tau(V_{DD}, I_{DP}) \cdot f_{sw}} \quad (7)$$

where f_{sw} is the switching frequency. Similar to the Silicon power device lifetime model, the GaN-GIT device reaches the end of lifetime when its switching stress $\Delta\tau$ accumulates to unity [28].

V. DHA DESIGN FOR RELIABILITY

The current state-of-the-art design for reliability (DfR) technique proposed in [29] is used to predict the lifetime, failure rate, and design robustness of individual components in order to design the inverter. This method takes full consideration of the operating condition, commonly denoted as mission profile, which is important in the lifetime calculation. For PV systems, the ambient temperature and solar irradiance of the location are the two important parameters in establishing the operating condition of the inverter. Thus, a mission profile based on a PV system installed in Phoenix, AZ, is used as the base location for this analysis. Furthermore, statistical analysis coupled with components lifetime models are used to predict the reliability of the system. The proposed multiphase inverter with DHA uses 3 high frequency modules ($n = 3$) for both inverter and APF operation, while the Non-DHA uses a set of 2 high frequency module for each operation ($n = 4$). The converter design parameters for a 2 kW PV system are given in Table III. Table IV provides the list of the components employed in this analysis.

A. Monte Carlos-Based Lifetime Evaluation of Components

In order to determine the inverter-level reliability, the lifetime of individual components is first evaluated using Monte Carlo simulation, where the stress factors of each component are varied. These stress factors such as device junction temperature T_j , temperature swings ΔT_j and cycle period t_{on} are derived from the thermal loading of the converter based on the mission profile in Phoenix, AZ. Given that the operating condition is dynamic and changing throughout the year, it is challenging to apply parameter distribution to T_j and ΔT_j in the Monte-Carlo simulation. As a result, equivalent static

TABLE III
CONVERTER DESIGN PARAMETERS

Parameter	Label	Value
PV rated power	P_{dc}	2 kW
DC-link voltage	V_{dc}	400 V
AC output voltage	V_{ac}	$240 V_{rms}$
Switching frequency	f_{sw}	≤ 800 kHz
Grid frequency	f_{line}	60 Hz
Module inductor	L_i	20 μ H
APF capacitor	C_{apf}	100 μ F

TABLE IV
SUMMARY OF COMPONENTS USED IN THE ANALYSIS

Parameter	Type	Value
GaN	GaN-GIT	600V/70m Ω (PGA26E07BA)
MOSFET	CoolMOS	650V/33m Ω (IPT65R033G7)
Capacitor	MPPF	650 V/110 μ F (C4AQCEW6110A3AJ)

TABLE V
STATIC PARAMETERS USED FOR MOSFET LIFETIME MODEL

Parameter	Label	Value
Mean ambient temperature	$T_{a,m}$	22 $^{\circ}$ C
Mean Junction temperature	$T_{j,m}$	32.92 $^{\circ}$ C
Temperature swing	ΔT_j	4 $^{\circ}$ C
Cycle period	t_{on}	0.083 s
Yearly cycles	n_i	1.89×10^9

values are used and have been shown in [30] to yield the same results as using dynamic variables. Table V gives a summary of the static parameters used in the model.

The unreliability evaluation result for each component in both DHA and Non-DHA modules is shown in Fig. 6. Their B_{10} lifetime percentage, which is defined as the lifetime when 10% of the population have failed, is summarized in Table VI. In both cases, the GaN-GIT device is the most unreliable component in the system. However, in the case of the DHA technique, there is less peak current stress on the GaN-GIT allowing for a higher lifetime in contrast to Non-DHA. The lifetimes of the MPPF-Cap in both schemes are nearly equal. Lastly, the MOSFET devices in the DHA module have such a significant lifetime of 600 years that it would not have much impact on the overall converter reliability at this power level. Its high reliability in this design is mainly due to the minimal junction temperature swings.

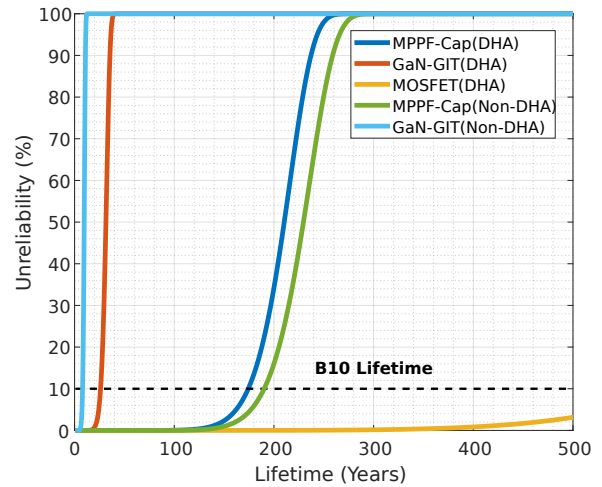


Fig. 6. Unreliability function showing B_{10} lifetime of MPPF-Capacitor, MOSFET and GaN-GIT devices for both DHA and Non-DHA.

TABLE VI
SUMMARY OF B_{10} LIFETIME EVALUATION RESULTS OF COMPONENTS FOR DHA AND NON-DHA MODULE

Components	DHA B_{10} Lifetime (Year)	Non-DHA B_{10} Lifetime (Year)
GaN-GIT	25	8
MPPF-Cap	172	190
MOSFET	600	-

B. System-Level Reliability Analysis

From the unreliability function $F(x)$ of individual components, the unreliability of a single module is calculated before evaluating the lifetime of the entire system. Each DHA module is a half-bridge topology consisting of six power switches ($S_1 - S_6$), an inductor (L_1) and a capacitor (C_{apf}). The Non-DHA module is the same with the exception of the switches $S_3 - S_6$. All the components in the module are in a series configuration given that a failure of any one of them will cause the entire module to fail. Thus, the unreliability of a DHA single module $F_{mod,dha}(x)$ is given by

$$F_{mod,dha}(x) = 1 - [(1 - F_{gan}(x))^2 \cdot (1 - F_{dsp}(x))^4 \cdot (1 - F_{cap}(x))] \quad (8)$$

where $F_{gan}(x)$ is the unreliability of the GaN-GIT power switches (S_1, S_2), $F_{dsp}(x)$ is the unreliability of the dispatch power switches ($S_3 - S_6$) and $F_{cap}(x)$ is the unreliability of the APF capacitor. In the case of Non-DHA, its single module unreliability function $F_{mod,nondha}(x)$ is

$$F_{mod,nondha}(x) = 1 - [(1 - F_{gan}(x))^2 \cdot (1 - F_{cap}(x))] \quad (9)$$

The reliability models for single modules, are used to generate the lifetime for the system. In this design, the failure of a single module due to internal component failure will not cause the entire system to seize operation. However, a minimum of two phases ($n = 2$) have to be operational in the case of DHA, with one phase dedicated to inverter operation while the other performs active power filtering. In the case of Non-DHA, one of each phase has to be operational at any given time. Thus, both DHA and Non-DHA power stage reliability is a parallel configuration system with identical element reliability $R(x)$ that can be calculated using the simplest case of k out of n hot redundancy given by

$$R(x) = \sum_{i=k}^n \binom{n}{i} R_{mod}(x)^i (1 - R_{mod}(x))^{n-i} \quad (10)$$

and

$$R_{mod}(x) = 1 - F_{mod}(x) \quad (11)$$

where k out of n available items are required for the system to properly operate [31]. In addition, there is a half-bridge module operating at line frequency (LF) used as the return phase leg. The LF module consists solely of two MOSFET power devices and can cause the entire system to fail if either of the devices fails. However, the probability of failure of a single MOSFET device is so low that it does not constitute a significant impact on the overall reliability of the system. The unreliability of the LF module is

$$F_{LF}(x) = (1 - F_{mos}(x))^2 \quad (12)$$

The total system unreliability function is

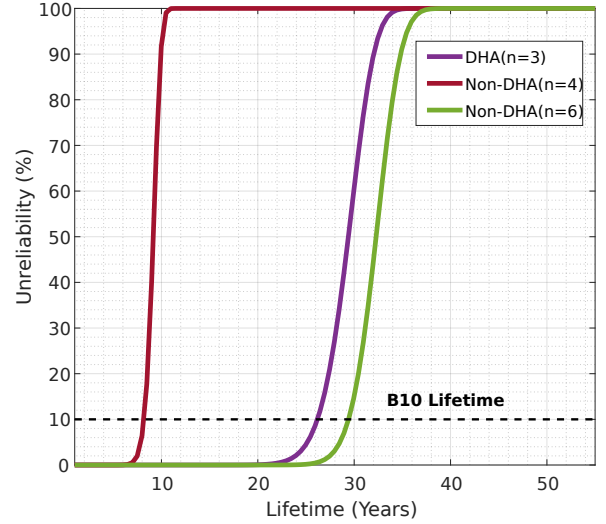


Fig. 7. Unreliability function of proposed 3 modules DHA ($n=3$) and 4 modules Non-DHA ($n=4$) showing B_{10} lifetime.

TABLE VII
SUMMARY OF B_{10} LIFETIME EVALUATION RESULTS OF DHA AND NON-DHA

Parameter	Units	DHA	Non-DHA	Non-DHA
Allocation Type		Dynamic	Static	Static
Number of Modules (n)		3	4	6
B_{10} Lifetime (B_{10})	Years	26	8	29
Peak Efficiency (η)	%	96.10	96.48	96.51

$$F_{sys}(x) = 1 - [(1 - F_{HF}(x)) \cdot (1 - F_{LF}(x))] \quad (13)$$

Fig. 7 shows the total estimated unreliability waveform of both the multiphase inverter architecture using DHA with 3 modules and Non-DHA with 4 and 6 modules. The obtained B_{10} lifetime and CEC efficiency of both schemes is given in Table VII. Although both architecture achieves comparable CEC efficiency performance, the DHA inverter yields a B_{10} lifetime of 26 years, which is more than three times that of the lifetime of a multiphase Non-DHA approach. To achieve comparable lifetime results to the DHA inverter, a Non-DHA system will require 6 modules with 3 phases each doing inverter and APF. When using the DHA technique, the reliability performance of the GaN-based inverter is greatly improved with fewer number of phases in comparison to the traditional multiphase approach.

VI. EXPERIMENTAL PROTOTYPE

A low power and voltage experimental prototype of the proposed DHA inverter has been implemented to demonstrate the feasibility of the DHA concept. The prototype consists of 3 HF modules with a single low-frequency return phase. A picture of the hardware is given in Fig. 8. Each module is operated using BCM modulation with unipolar switching. The power stage

TABLE VIII
PARAMETERS OF PROTOTYPE

Parameter	Value
Input voltage V_{dc}	80 V
Output voltage V_{out}	30 V/60 Hz
GaN Device	GaN-GIT (PGA26E07BA)
MOSFET Device	CoolMOS (IPT65R033G7)
MPPF APF Capacitor	3x30 μ F (MKP1847630354Y5)
Inductor L_1, L_2, L_3	20 μ H
Shunt Resistor R_{shunt}	20 m Ω
Inductor Core Geometry	Planar EI38
Inductor Core Material	Ferroxcube 3F36
Switching Frequency	120 kHz - 750 kHz

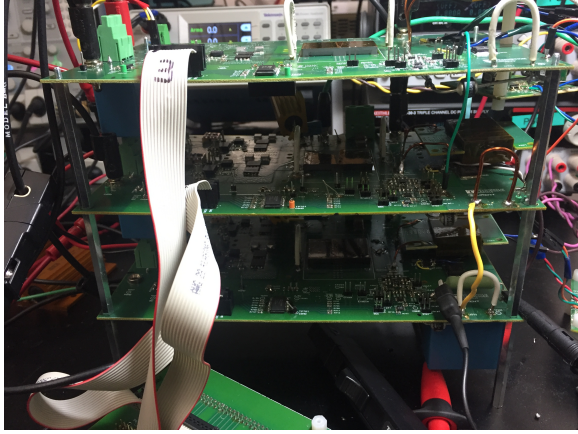


Fig. 8. Experimental prototype board.

of the high-frequency module uses 600V/70m Ω GaN-GIT devices from Panasonic while 650V/33m Ω CoolMOS devices from Infineon are used for the DHA switches (S_{inv}, S_{apf}). A XILINX Spartan 6 FPGA is used for digital logic and control. The experimental switching frequency ranges from 150 kHz to 800 kHz. Fig. 9 and Fig. 10 show the operation of the inverter using DHA for 1.5 A RMS output current and 30 V RMS output voltage. The inductor current for all three modules ($I_{L1} - I_{L3}$) and AC output voltage V_{out} can be seen in Fig. 9. In this test, module 1 is allocated for inverter operation, module 2 for APF, and module 3 switches operation between inverter and APF operation. The figure also illustrates the total number of modules allocated for each operation (n_{inv} or n_{apf}) during the entire line cycle. The peak inverter and APF current are well regulated through the DCPM control and are 4 A and 2.5 A respectively. Fig. 10 gives the measured APF capacitor voltage V_{apf} and the DC-link current I_{dc} . It can be seen that the APF successfully filters the second harmonic ripple power, and the DC-link current does not exhibit much fluctuation.

VII. CONCLUSIONS AND FUTURE WORK

The design for reliability analysis and implementation of a GaN-based single-phase inverter using DHA have been carried out and compared with a multiphase inverter with the static

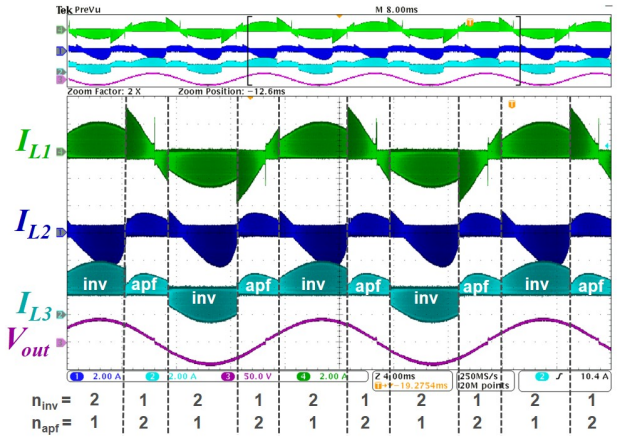


Fig. 9. Prototype experimental waveform of DHA inverter showing module 1, 2 and 3 inductor current ($I_{L1} - I_{L3}$), and AC output voltage V_{out} .

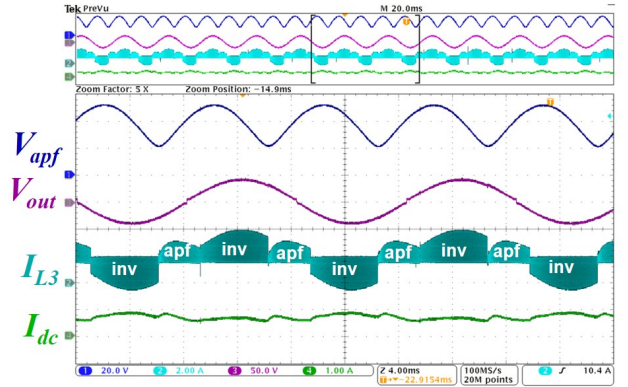


Fig. 10. Prototype experimental waveform of DHA inverter showing APF capacitor voltage V_{apf} , AC output voltage V_{out} , module 3 inductor current I_{L3} and DC-link current I_{dc} .

allocation (Non-DHA). The GaN device was determined to be the limiting component in the system. However, with the DHA inverter approach, the system achieves a much longer lifetime of approximately 26 years, outperforming the lifetime of a multiphase Non-DHA system with comparable efficiency metrics. In addition, the investigation in this paper showed that it is essential to integrate design for reliability analysis during the converter design stage instead of designing for just high efficiency. A low voltage and current experimental prototype have been successfully built and tested to validate the feasibility of the DHA concept. Future work will focus on improving the module power stage to allow for better efficiency and the converter demonstration at full rated power.

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