Mitigation of Current Distortion for GaN-Based CRM Totem-Pole PFC Rectifier with ZVS Control

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***Abstract*—The GaN-based critical conduction mode (CRM) totem-pole power factor correction (PFC) converter with full-line-cycle zero voltage switching (ZVS) is a promising candidate for high-efficiency front-end rectifiers. However, the input current can be degraded by line-cycle current distortion and ac line zero-crossing current spikes, and maintaining reliable ZVS control is difficult in noise-susceptible high-frequency environments. In this paper, a detailed analysis of the current distortion issues in a GaN-based CRM totem-pole PFC with digital ZVS control is provided, and effective approaches are proposed to mitigate different kinds of current distortion and ensure stable ZVS control under high-frequency operation. The proposed solutions have the advantages of straightforward implementation and do not increase the control complexity. The current distortion issues are demonstrated in two GaN-based CRM totem-pole PFC prototypes, a 1.5 kW PFC for data centers and a 100 W PFC in a 6.78 MHz wireless charging power supply for consumer electronics. The proposed methods are experimentally verified with effective mitigation of the current distortion and improvement of the converter power efficiency.**

***Index Terms*—GaN, CRM, totem-pole PFC, ZVS control, current distortion, data centers, wireless charging**

I. Introduction

POWER factor correction (PFC) converters are widely used in power supplies to satisfy requirements on power factor and harmonics. The traditional boost PFC has been utilized for many years, but is hampered by the high conduction loss on the front-end diode bridge [1]–[3]. Bridgeless PFC topologies have received attention as a means to eliminate the conduction losses of the diode bridge [4]. Among these, the totem-pole bridgeless PFC circuit is popular because of the simple structure, low conduction loss, and high utilization of devices [5]. Nevertheless, with silicon (Si) MOSFETs, the totem-pole PFC suffers from large body diode reverse recovery loss [4]. Employing gallium-nitride (GaN) devices, body diode reverse recovery loss is eliminated and lower on-resistance, faster switching speed, and higher thermal performance can be achieved [6], [7].

The hard-switching GaN-based totem-pole PFC with continuous conduction mode (CCM) operation has been demonstrated with high efficiency, but the switching frequency is usually limited below 120 kHz due to the switching loss [8], [9]. To reduce the switching loss and increase the switching frequency for higher power density, the totem-pole PFC with critical conduction mode (CRM) operation has attracted more attention because of the capability of achieving zero voltage switching (ZVS). The line-cycle rectifier diodes are usually replaced by Si MOSFETs to achieve lower conduction loss and allow reverse conduction current for ZVS operation. The GaN-based CRM totem-pole PFC converter is particularly suitable for low and medium power applications such as consumer electronics [10], telecommunication equipment [11], and data centers [12].

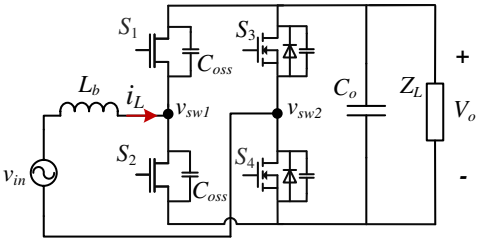


Fig. 1. Topology of the GaN-based totem-pole PFC converter.

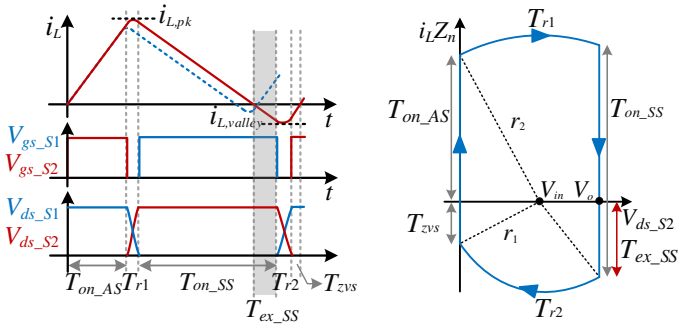


Fig. 2. Operation principle of the CRM totem-pole PFC with full-line-cycle ZVS in one switching period within the positive half-line cycle. (a) Switching waveforms; (b) State-plane trajectory.

Fig. 1 shows the topology of the GaN-based totem-pole PFC converter, where switches S_1 and S_2 are GaN transistors operating at the switching frequency, and S_3 and S_4 are Si MOSFETs working at ac line frequency. During the positive half line cycle, S_4 is always on, S_3 is always off, S_2 is the active switch (AS), and S_1 is the synchronous switch (SS). During the negative half-line cycle, S_3 is always on, S_4 is always off, S_1 is the active switch, and S_2 is the synchronous switch. For the CRM totem-pole PFC, ZVS is inherent only when $v_{in} \leq 0.5V_o$. When $v_{in} > 0.5V_o$, ZVS cannot be passively achieved due to insufficient energy stored in the inductor, leading to partial hard switching loss without modifications to the modulation pattern [13].

A. Full-Line-Cycle ZVS Modulation

Full-line-cycle ZVS modulation techniques are used to fully eliminate the turn-on switching loss of GaN devices [11], [12], [14], [15]. Fig. 2 illustrates the operation principle of the CRM totem-pole PFC with full-line-cycle ZVS, where V_{in}

is assumed nearly-constant in one switching cycle, and Z_n is the characteristic impedance defined as $Z_n^2 = {}^{L_b}/_{(2C_{oss})}$. The basic idea for achieving ZVS within the whole line cycle is to extend the conduction time of the synchronous switch T_{on_SS} by T_{ex_SS} during the non-natural ZVS region, so that the inductor valley current magnitude $|i_{L,valley}|$ is sufficiently large to enable ZVS. In the natural ZVS region, T_{ex_SS} is not needed, and S_1 is turned off at the positive-to-negative zero current crossing point.

The required extension time should be controlled accurately since shorter T_{ex_SS} cannot ensure ZVS, but longer T_{ex_SS} leads to larger current ripple and higher loss. In [13], [14], accurate modeling of the inductor current is developed and switching time intervals are calculated precisely considering non-linear effects. However, since the calculation is complicated and time-consuming, the conduction time is calculated offline and loaded into the controller, which limits the adaptability of the converter in wide input voltage range and varying output loads. To program the conduction time in real time with one microcontroller, a simplified but accurate calculation method is proposed in [16], where the inductor current is approximated as a triangular waveform. Based on the simplified calculation, [12] and [15] propose adaptive analytical models of the CRM totem-pole PFC converter with ZVS time margins. Based on the state trajectory (Fig. 2(b)), the extended conduction time is

$$T_{ex\_SS} = \frac{\sqrt{(k^2-1)V_{in}^2 - V_o^2 + 2V_oV_{in}}}{w_r(V_o - V_{in})} \tag{1}$$

where w_r is the resonant angular frequency, $w_r^2 = {}^1/_{(2C_{oss}L_b)}$ and k is the coefficient to ensure ZVS

$$k = \frac{r_1}{V_{in}} = \begin{cases} \frac{V_o - V_{in}}{V_{in}}, & V_{in} \le V_{bound} \\ k_0, & V_{in} > V_{bound} \end{cases} \tag{2}$$

k_0 is the selected ZVS margin, and $V_{bound} = {}^{V_o}/_{(k_0+1)}$ is the boundary input voltage between natural ZVS region and non-natural ZVS region. When $V_{in} \le V_{bound}$, $T_{ex\_SS} = 0$; when $V_{in} > V_{bound}$, $T_{ex\_SS} > 0$.

Since the resonant time is very short, the inductor current can be represented by $i_{L,pk} \approx ({}^{V_{in}}/_{L_b})T_{on\_AS}$, $i_{L,valley} = -{}^{kV_{in}}/_{Z_n}$, and $i_{L,ave} \approx {}^{(i_{L,pk}+i_{L,valley})}/_2$. Assuming $v_{in} = \sqrt{2}V_{in,rms}\sin\omega t$ and $i_{in} = \left({}^{\sqrt{2}P_o}/_{(\eta V_{in,rms})}\right)\sin\omega t$, the active switch conduction time T_{on_AS} is given by letting $i_{in} = i_{L,ave}$.

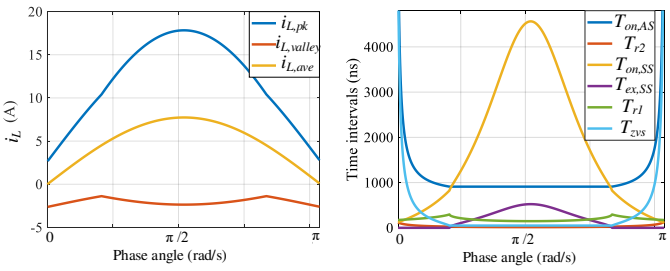
$$T_{on\_AS} = \frac{2P_oL_b}{\eta V_{in,rms}^2} + \frac{k}{w_r} \tag{3}$$

where η is the converter efficiency, $T_{on\_c} = {}^{2P_oL_b}/\left(\eta V_{in,rms}^2\right)$ is constant during steady-state operation, and $T_{on\_v} = {}^k/_{w_r}$ varies simultaneously with the the input voltage. More detailed calculations of the time intervals are available in [15]. Fig. 3 shows the ideal inductor currents and time intervals of a CRM totem-pole PFC converter with full-line-cycle ZVS.

B. Digital-Based Variable On-Time Control

Implementation of the full-line-cycle ZVS requires accurate switching signals and variable conduction time in one line cycle. Hence, digital-based control with real-time calculation is preferred to provide the computational flexibility and operation adaptability [16], [17]. Typically, a low-bandwidth proportional-integral (PI) controller is used to control the output voltage, and the PFC current can be regulated by hysteresis current control [18], [19], time-based current control [11], [15], or hybrid current control [12], [20]. In the hysteresis current control, inductor current can be well-regulated within the current bands, but the instantaneous current sensing is especially challenging in high-frequency applications. For the time-based current control, a zero-current-detection (ZCD) circuit is needed to generate a digital ZCD signal which is used to synchronize the controller timer, and gate signals are determined by comparing the timer with the calculated time intervals. Although hybrid current control combines the advantages of hysteresis control and time-based control, it requires both the ZCD signal and instantaneous current sensing, which increases the implementation complexity.

Therefore, time-based current control is more straightforward, and variable on-time control is widely-used [11], [15], [21], [22]. Fig. 4 shows a typical variable on-time control implementation with a digital signal processor (DSP). The voltage loop generates partial on time T_{on_c} to control the peak inductor current, and the positive-to-negative ZCD signal is used to reset the PWM timer and limit the inductor valley



(a) (b)

Fig. 3. PFC current and switching time intervals in the positive half line cycle. (a) Inductor currents; (b) Switching time intervals with $k_0 = 1.1$.

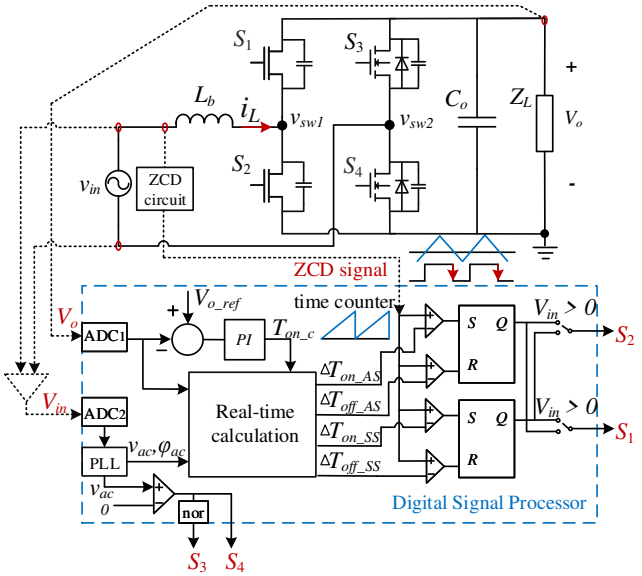
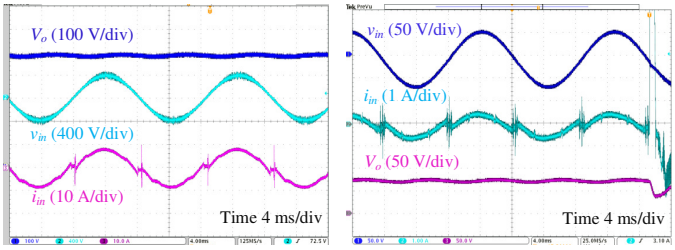


Fig. 4. Digital-based variable on-time control of a CRM PFC converter.



(a) (b)

Fig. 5. Experimental waveforms of GaN-based CRM totem-pole PFCs. (a) 1.5 kW CRM PFC for data center power supply unit; (b) 100 W CRM PFC for 6.78 MHz wireless consumer electronics power supply.

current. Switching time intervals are calculated in real time based on the converter model and sensed voltages, and GaN devices are switched after the associated time delays.

C. Current Distortion Issues

Maintaining reliable operation and low current distortion is challenging, especially in a noise-susceptible high-frequency environment. Fig. 5 presents example testing waveforms of two GaN-based CRM totem-pole PFC converters with ZVS control. Fig. 5(a) is measured on a 1.5 kW PFC for data centers, and Fig. 5(b) is a 100 W PFC for a 6.78 MHz wireless power tranfer (WPT) supply for consumer electronics. These prototypes are denoted "PFC_DC" and "PFC_WPT" respectively. In both cases, the input currents suffer from two distinct distortion mechanisms: the low-frequency line-cycle current distortion and the ac line zero-crossing current spike. For PFC_WPT in the WPT system, ZVS control becomes unstable with current runaway due to the high current distortion. Devices are turned off because of the over-current protection, and the PFC converter cannot operate at the target power.

The low-frequency line-cycle current distortion is caused by the inductor current ZCD sensing distortion due to signal propagation time delay and noise coupling during switching transitions. The ac line zero-crossing current spike results from two phenomena. The first is the asynchronization between the Si device switching and the input voltage zero-crossing, caused by the slower commutation of the Si devices (S_3, S_4) and practical implementation issues like inaccurate zero-crossing detection, sensing, and control time delay. The second is the high dv/dt noise induced during switching transition of the Si devices. To mitigate these two types of current distortion, research efforts have been made for totem-pole PFC converters [19], [23]–[33].

For the low-frequency line-cycle current distortion, to compensate the current sensing propagation time delay, [27] subtracts T_{delay} from the time difference T_{neg} between the two inductor current zero-crossing points based on the numerical relationship $T_{delay} < T_{neg}$. However, this method is not applicable for a high-frequency PFC converter with much smaller boost inductance because T_{neg} is comparable to or even smaller than T_{delay}. Paper [19] proposes a simple compensation method by tuning the propagation delay time and the parasitic inductance $L_{p,R}$ of the current sensing resistor. Given that the current sensing time error introduced by $L_{p,R}$ is a leading time error, it can be used to cancel out the propagation delay time. Nevertheless, the required $L_{p,R}$ for full compensation is quite large, and the sensing bandwidth is decreased, which is undesirable for high-frequency operation. On the other hand, in GaN-based high-frequency power converters with high dv/dt or di/dt, sensitive instantaneous voltage/current sensing circuits are easily disturbed with nonlinear dc bias or low-frequency shift [28], [29]. As a result, the sensing signal suffers from longer delay time, and the control becomes unstable.

For the ac line zero-crossing current spike that is related to the Si device switching, directly changing the switching speed by adjusting the gate resistance or adding additional drain-to-source capacitance cannot fully solve the problem, and may also increase the differential mode (DM) noise in the converter [30]. Soft transition approaches are proposed by turning on the GaN devices after each zero-crossing with gradually increased duty cycle or fixed small duty cycle [24], [26], [33]. However, these soft transition methods are either complicated or difficult to control precisely, and cannot be directly applied on the GaN-based high-frequency CRM totem-pole PFC with ZVS control. In [31], the current spike is completely suppressed by utilizing the LC resonance in an auxiliary circuit. However, the auxiliary circuit is complicated including two capacitors, one inductor, two MOSFETs, and two diodes. On the other hand, a hybrid PWM scheme is adopted in [32], where modulation switches from unipolar to bipolar during the zero-crossing to eliminate the current spike. However, bipolar modulation causes larger switching loss of the Si MOSFETs, or GaN devices are used in the slow phase leg for lower switching loss but leads to higher cost.

Therefore, the existing methods for mitigating current distortion have the disadvantages of complication, generation of other issues, or are not suitable for high-frequency and soft-switching operation. With a focus on the GaN-based CRM totem-pole PFC with digital ZVS control, this paper investigates the root causes of the current distortion and systematically addresses them. A detailed analysis of the current distortion is provided, and effective mitigation solutions are proposed for each type of current distortion. The proposed methods are straightforward and do not increase the control complexity. GaN-based CRM PFC prototypes in applications of data center and MHz wireless charging consumer electronics are used for demonstration. The current distortion issues are identified, and effectiveness of the proposed mitigation methods are validated.

This paper is organized as follows. Section II provides the detailed analysis of the current distortion issues. Section III illustrates the proposed methods to mitigate the current distortions. Section IV presents the experimental verification, and Section V gives the conclusions.

II. Analysis of Current Distortion Issues

A. Analysis of Line-Cycle Current Distortion

1) Impact of ZCD Signal Time Delay

One widely-used ZCD circuit is based on a shunt resistor R_{shunt}, as shown in Fig. 6. Various causes of ZCD signal time error are discussed in [29], with signal propagation delay

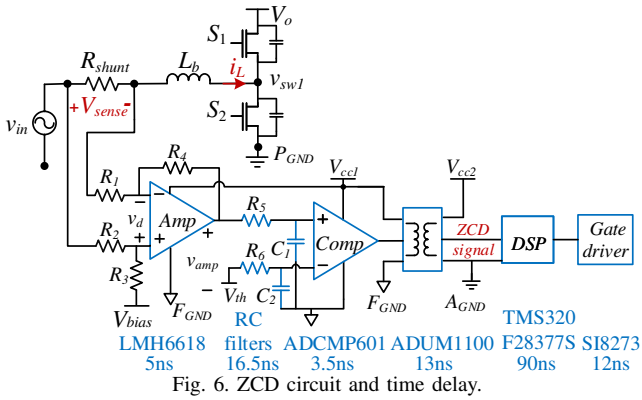


Fig. 6. ZCD circuit and time delay.

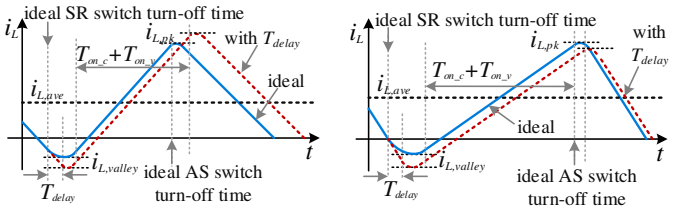


Fig. 7. Inductor current in one switching cycle with impact of ZCD time delay. (a) i_L when $V_{in} > V_{bound}$; (b) i_L when $V_{in} \leq V_{bound}$.

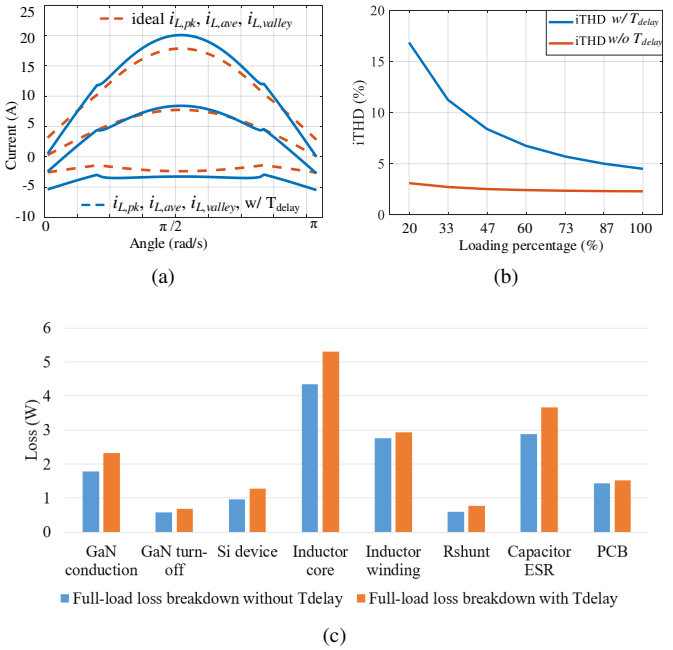


Fig. 8. Impacts of the ZCD time delay on the PFC performance: (a) inductor current; (b) input current THD; (c) power loss.

identified as the dominant mechanism. In the example implementation, around 140 ns time delay exists in the propagation path, leading to the line-cycle current distortion.

As elaborated in Fig. 7, the ZCD time delay T_{delay} causes the current to deviate from normal operation. The turn-off moment of the synchronous switch is late by T_{delay}, resulting in a lower inductor valley current. To maintain the same output power, the PI controller will increase its output T_{on_c} to increase the conduction time of the active switch T_{on_AS} and inductor peak current. According to the variable on-time control, $T_{on\_AS} = T_{on\_c} + T_{on\_v}$, where T_{on_v} is the changing part from the model-based calculation. When $V_{in} > V_{bound}$ (Fig. 7(a)), $i_{L,pk}$ is higher with the increased T_{on_c} since $T_{on\_v} = 0$ and $T_{on\_AS} = T_{on\_c}$. However, when $V_{in} \leq V_{bound}$ (Fig. 7(b)), $T_{on\_v} \neq 0$ and varies instantaneously with the sensed voltages. Although T_{on_c} is increased by the PI controller, T_{on_v} is still calculated based on the ideal model, which is not adequate to maintain the same peak current. Hence, with ZCD time delay, $i_{L,valley}$ is lower, but $i_{L,pk}$ is higher in the non-natural ZVS region and lower in the natural ZVS region.

Fig. 8 illustrates the impacts of the ZCD time delay on the current and power loss in an example CRM PFC converter operating at 1.5 kW. The inductor current is severely distorted with larger current ripple and RMS value (Fig. 8(a)). The current THD with T_{delay} is two times as high as the normal case at full load, and even worse at light load (Fig. 8(b)). Also, all loss mechanisms are increased compared with the case without T_{delay} and the total loss is increased from 15.4 W to 18.5 W (Fig. 8(c)).

2) Noise Impact on ZCD Signal

In conventional front-end power supplies, the PFC rectifier is connected to an isolated dc-dc converter. Typically, isolation is realized by a tightly-coupled magnetic transformer or integrated planar transformer [34]. For wireless charging power supplies, the transmitter and receiver coils are usually loosely-coupled with magnetic resonance [35]. In GaN-based high-frequency power supply systems, common-mode (CM) noise due to high dv/dt is significant, and will impact the generation of the ZCD signal.

Fig. 9 shows the CM noise propagation paths in a typical GaN-based two-stage ac-dc power supply system, where the dc-dc stage is represented by a half-bridge isolated converter with diode rectifier on the output. High dv/dt noise is created by the switching points v_{sw1}, v_{sw2}, and v_{sw3}. With the parasitic capacitance C_{p1}-C_{p4}, the generated noise currents are injected to the reference ground (E_{GND}). C_{p5} and C_{p6} are the parasitic capacitance between the transformer/WPT coils and E_{GND}, which are negligible for transformers, but can be significant for WPT coils with large area. Bridging parasitic capacitance C_{p7} transmits the noise current from the primary side to the secondary side. Parasitic capacitances C_{p8} and C_{p9} exist between high dv/dt nodes A, B and E_{GND}. Given the distances between A, B and E_{GND} are the same, and the dv/dt waveforms generated at A, B have 180° phase shift, noise currents flowing through C_{p8} and C_{p9} are canceled out. The noise current finally flows into the ground via load parasitic capacitance C_{p10} and C_{p11}.

The noise currents then propagate to the ac input terminal, and flow back leading to a conduction loop. Even with the input EMI filter, partial CM noise current still flows into the ZCD circuit through the current sensing terminals or parasitic capacitance C_{p0}, which might pollute the ZCD signal.

Fig. 10 presents the simulated waveforms of the two-stage ac-dc power supply system (Fig. 9) in different operating conditions, including the low-side drain-to-source voltages $v_{ds,S2}, v_{ds,S6}$, the inductor current i_L, the differential input signal v_d of the amplifier in ZCD circuit, the amplifier

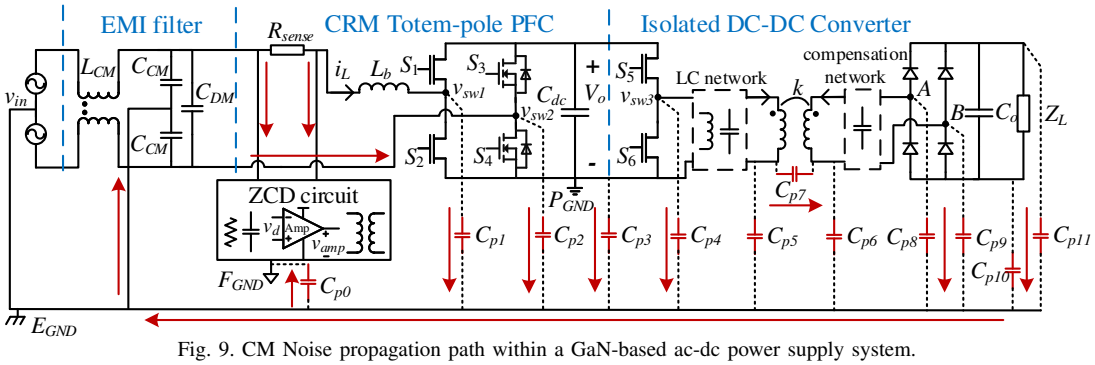
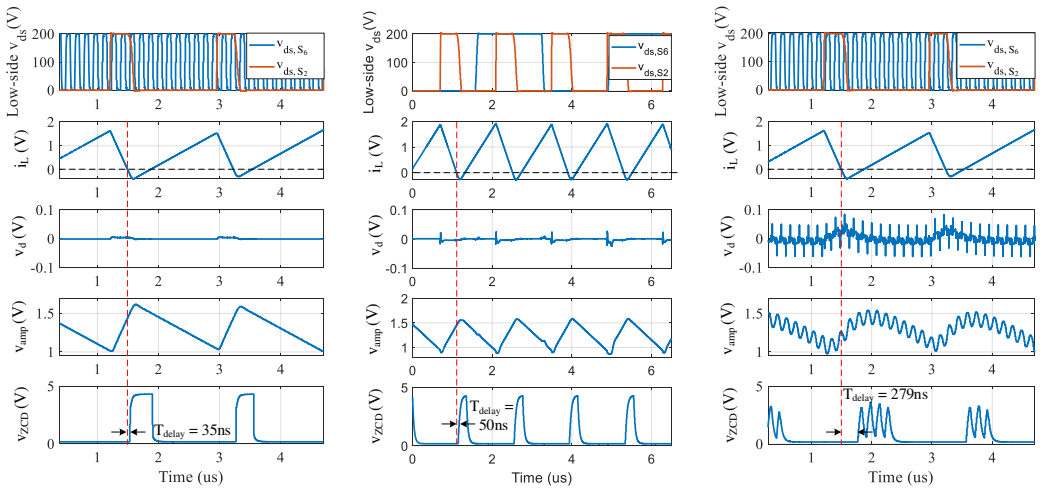


Fig. 9. CM Noise propagation path within a GaN-based ac-dc power supply system.



(a) (b) (c)

Fig. 10. Simulated waveforms of the ZCD circuit at $V_{in} = 70$ V in ac-dc power supply systems with $v_{in} = 120\ \mathrm{V_{ac}}, V_{dc} = 200$ V, $V_o = 30$ V, and $P_o = 100$ W. (a) Normal case with no parasitic capacitance and noise propagation; (b) Case where the PFC is connected to a 300 kHz half-bridge LLC isolated converter; (c) Case where the PFC is connected to a 6.78 MHz wireless charging system with a half-bridge inverter and WPT coils.

output signal v_{amp}, and the ZCD signal v_{ZCD}. To fairly compare, all the cases are simulated with $v_{in} = 120\ \mathrm{V_{ac}}, V_{dc} = 200$ V, $V_o = 30$ V, $P_o = 100$ W, and ZVS turn-on switching is achieved in all GaN-based active switches. Fig. 10(a) shows the ideal case without the high-frequency CM noise. v_{amp} is a clean waveform proportional to the inductor current, and the ZCD signal is a clear pulse with 35 ns delay time.

Fig. 10(b) is the application where the PFC converter is followed by a typical half-bridge LLC isolated converter switching at 300 kHz, and parasitic capacitance is considered. The amplifier signals are barely influenced with only small notches due to the PFC switching noise, and the ZCD signal is a clear pulse with small time delay.

Fig. 10(c) presents the case of a wireless charging power supply system based on MHz magnetic resonance, where the CRM PFC is connected to a 6.78 MHz half-bridge inverter and transmitter/receiver coils. The amplifier differential input v_d is coupled with a large amount of switching noise, and v_{amp} has resonant ripples at 6.78 MHz. Consequently, noise occurs in the ZCD signal, and the time delay is much longer at 279 ns.

Therefore, in high-frequency applications with significant dv/dt noise, the ZCD circuit is easily distorted, leading to longer ZCD time delay and current distortion. Distortion of the ZCD signal can also result in erroneous switching actions, impacting control stability as displayed in Fig. 5(b).

B. Analysis of Ac Line Zero-Crossing Current Spike

1) Current Spike due to Slower Transition of Si Devices

One typical reason for the ac line zero-crossing current spike is the asynchronization between the Si device switching and the input voltage zero-crossing [24], [25], [33]. Compared with the GaN device switching speed with dv/dt in excess of 100 V/ns, the commutation speed of the Si MOSFET is much slower [6]. In practical implementations, small delays, switching noise, limited dv/dt, and input voltage PLL error cause the Si device switching to not be perfectly synchronized to the input voltage zero-crossing.

To avoid inductor current instability that occurs when the polarity of the input voltage is not matched to the Si device switching state, a small blanking time is normally adopted near the voltage zero-crossing during which all switches are shut off [36]. As illustrated in Fig. 11(a), just before the negative-to-positive transition, S_1 and S_3 conduct, and v_{sw1}, v_{sw2} are tied to the high output voltage. During the blanking time, $S_1 - S_4$ are all off, and $i_L = 0$ (Fig. 11(b)). Ideally, after the blanking time, the GaN devices and the Si devices switch simultaneously with the same speed. S_2 becomes the active switch conducting with large duty cycle, and the inductor current is charged by the small input voltage (Fig. 11(d)). As shown in Fig. 12(a), i_L gradually increases with a small slope and no current spike occurs.

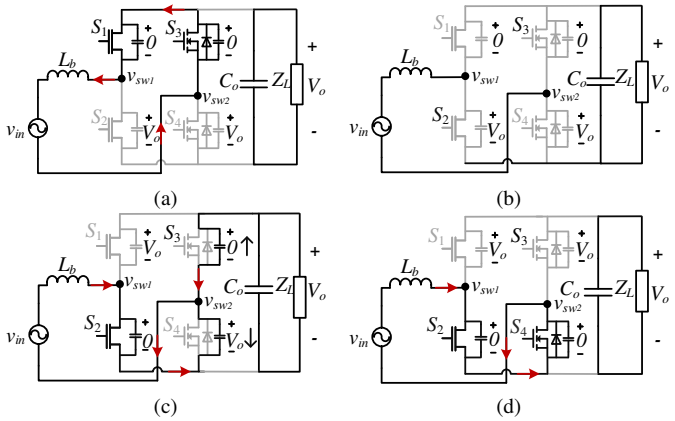


Fig. 11. Negative-to-positive transition process of the totem-pole PFC.

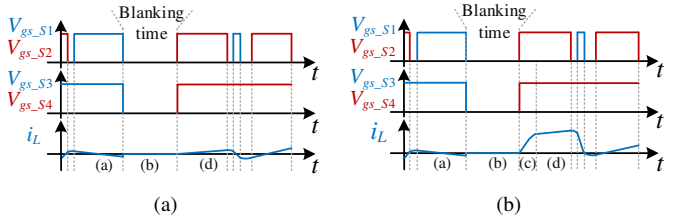


Fig. 12. Device gate signal and inductor current during the negative-to-positive transition of the totem-pole PFC. (a) Ideal case with perfect device synchronization; (b) Practical case with slower Si device commutation.

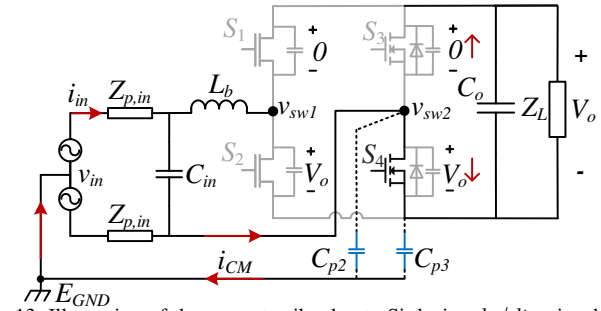


Fig. 13. Illustration of the current spike due to Si device dv/dt noise during the negative-to-positive transition.

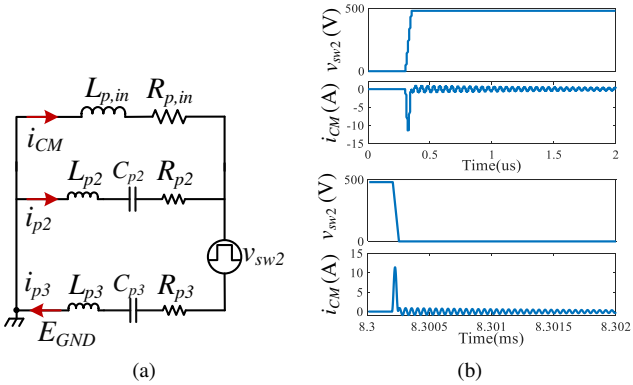


Fig. 14. Modeling of the current spike due to Si device switching. (a) High-frequency noise model; (b) Predicted i_{CM} when v_{sw2} changes.

Nevertheless, in practice, Si MOSFETs commutate much slower than the GaN devices. Once the blanking time ends, S_2 turns on and, due to the smaller C_{oss} and Q_g of the GaN transistors, v_{sw1} drops nearly to zero well before the Si MOSFET commutation completes. During the process (Fig. 11(c)), the voltage applied on the inductor is $(v_{in} + v_{sw2})$, which gradually decreases from $(v_{in} + V_o)$ to v_{in} as S_4 C_{oss} is discharged. As presented in Fig. 12(b), the inductor current rises quickly until S_4 is fully on (Fig. 11(d)). Consequently, a positive current spike occurs during the negative-to-positive transition. Similarly, a negative current spike occurs during the positive-to-negative transition.

2) *Current Spike due to Si Device Switching dv/dt Noise*

To avoid the current spike due to slow switching of the Si devices, the Si devices can be purposely turned on earlier during the blanking time. However, this scheme may not fully eliminate current distortion at the voltage zero-crossing. Although this approach mitigates the phenomenon shown in (Fig. 11(c)), a second mechanism remains due to the Si device switching dv/dt noise and the parasitic capacitance as illustrated in Fig. 13. Although Si devices have longer commutation time than GaN devices, the switching speed is still in tens of V/ns [37]. During the negative-to-positive blanking time, $S_1 - S_3$ remain off while S_4 turns on, leading to v_{sw2} decreasing from V_o to 0 with around -10 V/ns slew rate. Since parasitic capacitances C_{p2} and C_{p3} are connected to E_{GND}, CM noise current is induced and propagates to the input line, resulting in a large current spike in i_{in}.

To analytically understand the CM noise current resulting from v_{sw2} dv/dt noise, an equivalent high-frequency CM noise model is extracted from Fig. 13, as presented in Fig. 14(a). During the zero-crossing, the input ac source is approximated as short circuit, and the input capacitor C_{in} can be ignored. $L_{p,in}$, $R_{p,in}$ are the equivalent inductance and resistance of the input line impedance, $Z_{p,in}$. High-frequency models of C_{p2} and C_{p3} are represented by series RLC circuits. The noise source v_{sw2} is modeled by a line frequency square waveform with 10 V/ns rising and falling slope.

$$v_{sw2}(t) = \big(u(t) - u(t-t_0)\big)\frac{V_o}{t_0}t + V_o\big(u(t-t_0) - u(t-t_1)\big) - \big(u(t-t_1) - u(t-t_0-t_1)\big)\frac{V_o}{t_0}(t-t_0-t_1) \tag{4}$$

where t_0 is the voltage rising and falling time, and $t_1 = 1/2f_{line}$ with $f_{line} = 60$ Hz. In the s domain, the circuit equations based on KVL and KCL laws are

$$\begin{cases} 0 = V_{sw2}(s) + I_{p3}(s)\big(Z_{p3}(s) + \frac{Z_{p2}(s)Z_{p,in}(s)}{Z_{p2}(s)+Z_{in}(s)}\big) \\ I_{CM}(s) = I_{p3}(s)\big(\frac{Z_{p2}(s)}{Z_{p2}(s)+Z_{p,in}(s)}\big) \end{cases} \tag{5}$$

where $V_{sw2}(s) = \mathscr{L}(v_{sw2}(t))$, $Z_{p,in}(s) = 2(sL_{p,in} + R_{p,in})$, $Z_{p2}(s) = sL_{p2} + R_{p2} + 1/sC_{p2}$, and $Z_{p3}(s) = sL_{p3} + R_{p3} + 1/sC_{p3}$. Then the CM noise current is solved by the inverse Laplace transform of $I_{CM}(s)$

$$i_{CM}(t) = \mathscr{L}^{-1}(I_{CM}(s)) = \mathscr{L}^{-1}\left(\frac{-V_{sw2}(s)}{Z_{p3}(s)(1+\frac{Z_{p,in}(s)}{Z_{p2}(s)}) + Z_{p,in}(s)}\right) \tag{6}$$

Fig. 14(b) shows the predicted i_{CM}, which has a significant spike when v_{sw2} changes during the ac line zero-crossing.

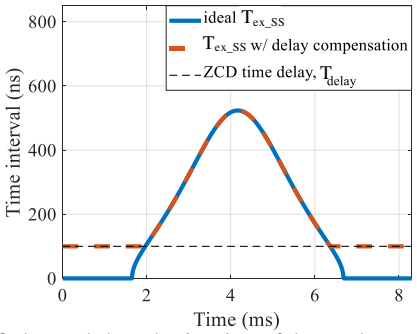


Fig. 15. Modified extended conduction time of the synchronous switch in the half line cycle for delay compensation.

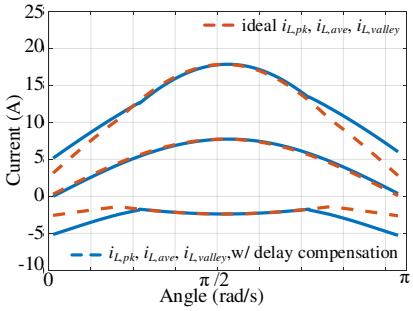


Fig. 16. Inductor current in the positive half line cycle with the modified converter model for ZCD T_{delay} compensation.

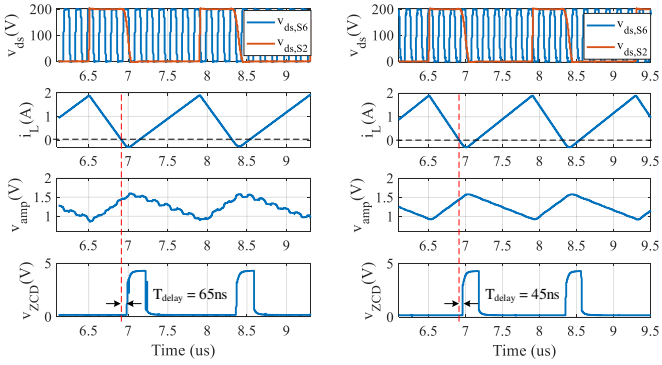


Fig. 17. Simulated waveforms of the ZCD circuit with noise attenuation. (a) With CM choke in the dc-dc stage LC network; (b) With CM filter on dc bus between the PFC stage and the dc-dc stage.

III. Mitigation Methods for Current Distortion

A. Mitigation Methods for Line-Cycle Current Distortion

1) Delay Compensation with Modified Converter Model

Because of the ZCD time delay, the actual extended conduction time of the synchronous switch T_{ex_SS} is increased as the sum of T_{delay} and the ideal extension time $T_{ex\_SS,ideal}$, leading to lower $|i_{L,valley}|$ and distorted input current. In order to maintain the ideal input current, the converter model should be modified considering T_{delay}, and $i_{L,valley}$ should be kept close to the ideal value to limit distortion and/or additional conduction loss.

First, T_{ex_SS} is adjusted close to $T_{ex\_SS,ideal}$. As presented in Fig. 15, when $T_{ex\_SS,ideal} \geq T_{delay}$, compensation can be easily achieved by subtracting T_{delay} from $T_{ex\_SS,ideal}$; when $T_{ex\_SS,ideal} < T_{delay}$, T_{ex_SS} is minimized at T_{delay}, as the switching instant cannot occur before the sensed ZCD signal without significant changes to the control architecture. Thus, the actual extended conduction time is

$$T_{ex\_SS} = \begin{cases} T_{ex\_SS,ideal}, & T_{ex\_SS} \geq T_{delay} \\ T_{delay}, & T_{ex\_SS} < T_{delay} \end{cases} \tag{7}$$

Second, the converter model should be modified based on T_{ex_SS} to ensure minimal distortion of i_{in}. Comparing T_{ex_SS} with $T_{ex\_SS,ideal}$, the only difference is the minimum extended conduction time, which is increased from zero to T_{delay} during the natural ZVS region. Hence, letting $T_{ex\_SS} = T_{delay}$ in (1), $k^2 = (1+(\omega_n)^2(T_{delay})^2)(V_o - V_{in})^2/V_{in}^2$, and the ZVS margin k shown in (2) is updated as

$$k = \begin{cases} \frac{V_o - V_{in}}{V_{in}} \sqrt{1+(\omega_n)^2(T_{delay})^2}, & V_{in} \leq V_{bound} \\ k_0, & V_{in} > V_{bound} \end{cases} \tag{8}$$

V_{bound} should also be altered to maintain a smooth transition between the natural ZVS region and ZVS extension region.

$$V_{bound} = V_{in}\Big|_{k(V_{in} \leq V_{bound}) = k(V_{in} > V_{bound})} \tag{9}$$

$$V_{bound} = \frac{\sqrt{1+(\omega_n)^2(T_{delay})^2}}{k_0 + \sqrt{1+(\omega_n)^2(T_{delay})^2}} V_o \tag{10}$$

Expressions for $i_{L,pk}$, $i_{L,valley}$, T_{on_AS}, T_{r1}, T_{on_SS}, T_{r2}, and T_{ZVS} do not change.

Fig. 16 shows the inductor currents in the positive half line cycle. With the modified converter model, the average inductor current $i_{L,ave}$ is kept unchanged as the ideal case, and inductor current ripple is not increased over the majority of the line cycle. The only difference is the slightly enlarged current ripple during the natural ZVS region, where T_{delay} cannot be fully compensated. However, the impact of such discrepancy is not severe because both the voltage and current are low in this region, and $i_{L,ave}$ is not distorted.

2) Approaches for High-Frequency Noise Immunity

To prevent CM noise from distorting the sensed ZCD signal, the noise should be attenuated in the path of the ZCD circuit. In general, efforts can be made in two directions. First, the CM impedance within the power stage can be increased to attenuate the overall noise current. In the ac-dc power supply system (Fig. 9), a CM filter can be placed on the dc bus so that the high-frequency noise from the dc-dc stage will not propagate to the PFC stage. Also, increasing the CM impedance of the LC network helps suppress the CM noise. Fig. 17 shows the simulated waveforms of the ZCD circuit with attenuated noise based on the same 6.78 MHz WPT system. In Fig. 17(a), a CM choke is added in the dc-dc stage LC network. As a result, the ZCD amplifier output has smaller noise ripple, the ZCD signal is much cleaner, and T_{delay} reduces to 65 ns. Adding a CM filter on the dc bus is more effective: as shown in Fig. 17(b), v_{amp} is nearly distortion-free, and the ZCD signal is almost ideal.

As a second alternative, the common mode noise rejection level of the ZCD circuit can be increased. For the differential amplifier used in the ZCD circuit (Fig. 6), the common mode

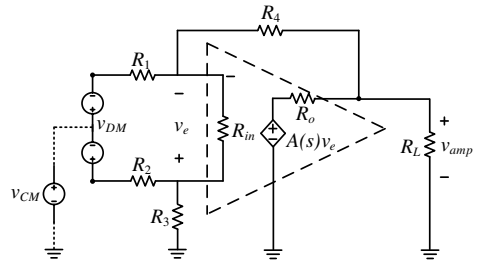
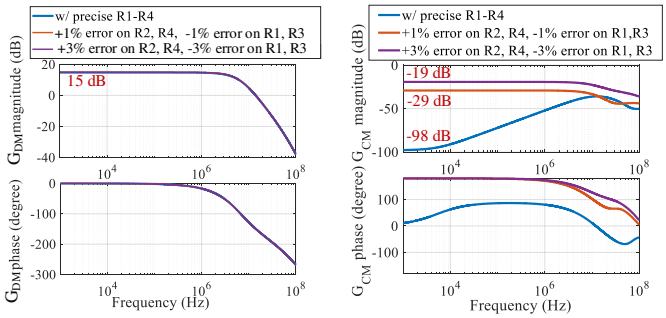


Fig. 18. Equivalent circuit of a typical differential amplifier.



(a) (b)

Fig. 19. Bode plot of the closed-loop gains in the differential amplifier with $R_1 = R_2 = 1$ kΩ, $R_3 = R_4 = 6$ kΩ, $R_{in} = 10^{12}$ Ω, $R_o = 10$ Ω (a) DM closed-loop gain; (b) CM closed-loop gain.

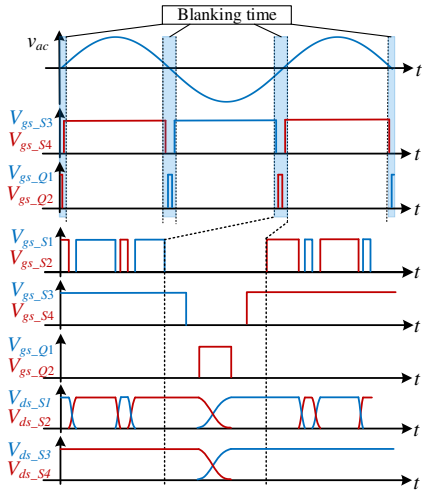


Fig. 20. Device switching sequence during the ac line zero-crossing.

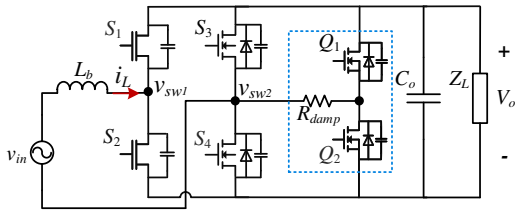


Fig. 21. Auxiliary circuit for eliminating the dv/dt noise of Si device.

rejection rate (CMRR) highly depends on the precision of the feedback resistors $R_1 - R_4$. Fig. 18 shows the equivalent circuit of the differential amplifier, where $A(s)$ is the open-loop gain and represented by a multi-pole transfer function. Based on the model, the DM closed-loop gain $G_{DM} = {}^{v_{amp}}/_{v_{DM}}$ and CM closed-loop gain $G_{CM} = {}^{v_{amp}}/_{v_{CM}}$ are

$$G_{DM}(s) = \frac{1}{2}\left(\frac{R_4}{R_1}\cdot f_{A1}(s) + \frac{R_3}{R_1 + f_{A2}(s)}\cdot\frac{R_1+R_4}{R_2+R_3}\right) \quad (11)$$

$$G_{CM}(s) = -\frac{R_4}{R_1}\cdot f_{A1}(s) + \frac{R_3}{R_1 + f_{A2}(s)}\cdot\frac{R_1+R_4}{R_2+R_3} \quad (12)$$

where $f_{A1}(s), f_{A2}(s)$ are functions of $A(s)$. Since R_{in} and $|A(s)|$ are very large in the low-frequency range, $|f_{A1}(s)| \approx 1, |f_{A2}(s)| \approx 0$, and $G_{DM} = {}^{R_4}/_{R_1}, G_{CM} = 0$ with $R_1 = R_2, R_3 = R_4$.

$$f_{A1}(s) = \frac{\frac{A(s)}{R_o} - \frac{1}{R_4}}{\frac{A(s)}{R_o} + \frac{R_o+R_L}{R_oR_L} + \frac{R_1+R_{in}}{R_1R_{in}}\left(1 + \frac{R_4(R_o+R_L)}{R_oR_L}\right)} \quad (13)$$

$$f_{A2}(s) = \frac{R_o\left(1+\frac{R_o}{R_L}\right)\left(R_{in} + R_3 + \frac{R_1R_4}{R_1+R_4} - \frac{R_3}{R_2+R_3}\right)}{A(s)\frac{R_{in}}{R_1+R_4} + \frac{R_1R_o}{(R_1+R_4)^2}} \quad (14)$$

Fig. 19 displays the bode plots of G_{DM} and G_{CM} in three cases: a nominal case with precise resistances for $R_1 - R_4$, an error case with 1% error in resistance, and an error case with 3% error in resistance. In all cases, G_{DM} is nearly identical with 15 dB low-frequency gain. However, G_{CM} changes, with low-frequency gain increased from -98 dB in the nominal case to -29 dB in the 1% error case and to -19 dB in the 3% error case. Consequently, the amplifier CMRR is reduced from 113 dB to 34 dB. Therefore, resistors with higher precision should be used in the amplifier circuit to maintain high CMRR.

In addition, for the ZCD circuit (Fig. 6), balanced RC filters with $R_5 = R_6$, $C_1 = C_2$ between the amplifier and the comparator filter out the coupled noise on v_{amp} and v_{th}. These filters must be selected carefully to provide adequate noise attenuation without contributing significant propagation delay.

B. Mitigation Methods for Ac Zero-Crossing Current Spike

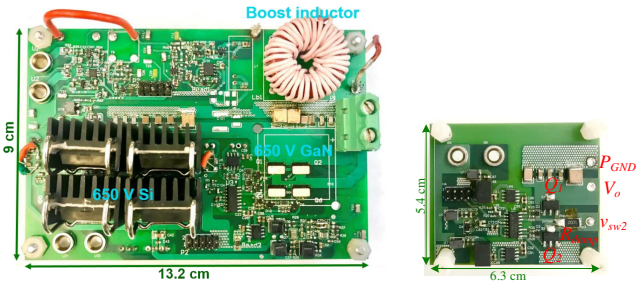
1) Device Switching Sequence

To reduce the current spike after blanking time, a fixed device switching sequence is assigned, as illustrated in Fig. 20. During the blanking time, the Si MOSFETs are turned off later and turned on earlier than the GaN devices. A sufficient delay time of a few μs is inserted between GaN switching and Si switching to ensure that the Si device is fully turned on when the GaN device turns on after the blanking time. To maintain ZVS in the first switching cycle, the GaN devices are turned on at the beginning of a new period.

2) Auxiliary Circuit for dv/dt Noise Elimination

In order to eliminate the current spike induced by the dv/dt noise of Si device switching, a simple auxiliary circuit consisting of one damping resistor R_{damp} and two Si MOSFETs Q_1, Q_2 is proposed, as shown in Fig. 21. Q_1 and Q_2 only conduct for a fixed short period during the blanking time (Fig. 20). In the process of the negative-to-positive transition, Q_2 is turned on when $S_1 - S_4$ are shut off, which provides a current flow path for voltage damping. Then the output capacitance of S_4 and R_{damp} form a R-C circuit, and v_{ds_S4} is smoothly damped to zero. Similarly, during the positive-to-negative transition, Q_1 is turned on within the blanking time to help damp v_{ds_S3}.

To ensure the voltage is completely damped, R_{damp} and Q_1, Q_2 conduction time should be selected properly. Small



(a) (b)

Fig. 22. (a) Prototype of PFC_DC; (b) Prototype of the auxiliary board for eliminating the ac line zero-crossing current spike.

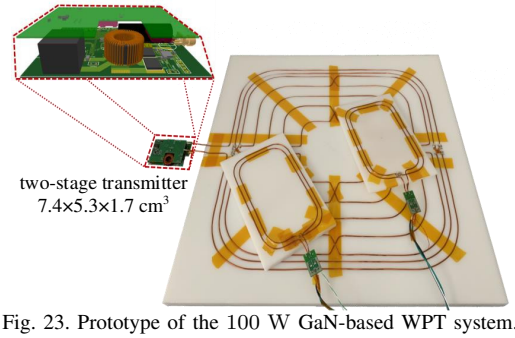


Fig. 23. Prototype of the 100 W GaN-based WPT system.

R_{damp} cannot sufficiently slow down the dv/dt, but high R_{damp} requires longer conduction time. During the damping process, the drain-to-source voltage of S_3 or S_4 is

$$v_{ds\_Si} = V_o e^{-\frac{t}{\tau}} \tag{15}$$

where time constant $\tau = R_{damp}C_{eq}$, and C_{eq} is the equivalent output capacitance of S_3 and S_4. Typically, the conduction time of Q_1,Q_2 is selected as $3\tau - 5\tau$. Given the Si MOSFET usually has C_{oss} in nF level, R_{damp} of a few kΩ can be used, resulting in a conduction time in tens of μs.

The auxiliary circuit has the benefits of simple topology, low cost, and almost no extra power loss. Since Q_1 and Q_2 switch at the line frequency and their conduction time is short, Si MOSFETs with very low current rating ($< 1A$) are adequate, and the device power consumption is negligible. The only power dissipation comes from the energy stored in the C_{oss} of S_3 and S_4, which is quite small, *e.g.*, $P_{damp} = 0.03$ mW with $f_{line} = 60$ Hz, $C_{eq} = 2.2$ ns, and $V_o = 480$ V.

$$P_{damp} \approx C_{eq} V_o^2 f_{line} \tag{16}$$

Implementation of the blanking time and the device switching sequence can be easily achieved through the digital phase-locked loop (PLL) and PWM module within the controller. No extra control resources are required.

IV. Experimental Verification

A. Hardware Prototypes

Two GaN-based CRM totem-pole PFC prototypes are used for experimental verification: a 1.5 kW PFC prototype for data center power supply [38] and a 100 W PFC for a 6.78 MHz GaN-based WPT system [39]. Both the PFC prototypes are

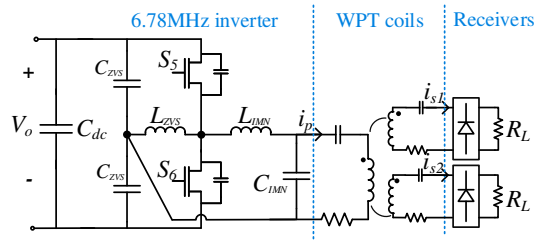
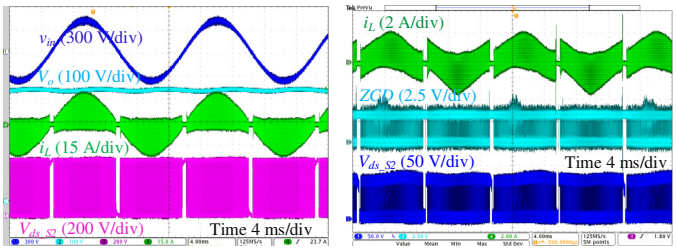


Fig. 24. Topology of the 6.78 MHz dc-dc stage in the WPT system.



(a) (b)

Fig. 25. Experimental waveforms of GaN-based CRM totem-pole PFCs with current distortions. (a) PFC_DC; (b) PFC_WPT.

implemented with variable on-time control for achieving full-line-cycle ZVS, and a TMS320F28377S DSP is used as the digital controller in both. Prototype circuitry of PFC_DC is shown in Fig. 22(a), and Table I presents the operation specifications. In order to validate the effectiveness of the proposed auxiliary circuit for eliminating the ac line zero-crossing current spike, a small board with a damping resistor and two Si MOSFETs is designed, as shown in Fig. 22(b). A 10 kΩ surface-mount resistor is selected as the damping resistor, and 600 V, 1 A STD1NK60T4 Si MOSFETs are used.

TABLE I. Specifications of PFC_DC [38].

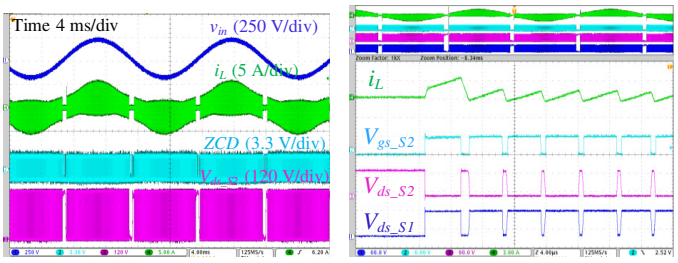
Parameter	Value
Input voltage v_{in}	277 V_{ac}, 60 Hz
Output voltage V_o	480 V_{dc}
Output power P_o	1.5 kW
Switching frequency f_{sw}	174 – 508 kHz
GaN devices S_1, S_2	GS66508T, 650 V
Si devices S_3, S_4	IPW65R019C7, 650 V
ZVS margin	$k_0 = 1.1$, $T_{ZVS,min} = 50$ ns

Fig. 23 shows the prototype of the 100 W 6.78 MHz GaN-based WPT system for consumer electronics. The CRM PFC is adopted in the first stage of the transmitter, and the second stage is a half-bridge inverter operating at 6.78 MHz with multiple receivers. Fig. 24 is the topology of the 6.78 MHz dc-dc stage used in the WPT system, and Table II shows the detailed specifications of the PFC_WPT.

TABLE II. Specifications of PFC_WPT [39].

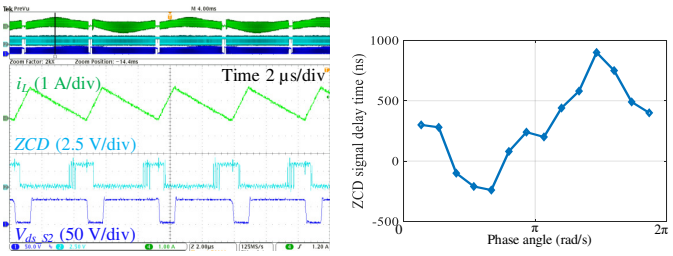
Parameter	Value
Input voltage v_{in}	120 V_{ac}, 60 Hz
Output voltage V_o	200 V_{dc}
Output power P_o	100 W
Switching frequency f_{sw}	187 – 725 kHz
GaN devices $S_1 - S_4$	GS66508B, 650 V
ZVS margin	$k_0 = 1.1$, $T_{ZVS,min} = 50$ ns

The testing results of the two PFC prototypes are shown in Fig. 5 and Fig. 25, where severe current distortion occurs



(a) (b)

Fig. 26. Experimental waveforms of PFC_DC with compensated ZCD signal propagation time delay.(a) Line cycle waveform; (b) Zoomed-in current spike after the blanking time.



(a) (b)

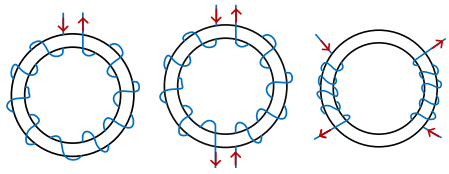
Fig. 27. Tested ZCD signal of PFC_WPT in the 6.78 MHz WPT system. (a) Noise on ZCD signal; (b) Varying ZCD time delay within one line cycle.

with both line-cycle current distortion and current spikes during the ac line zero-crossing. For PFC_DC, the line-cycle current distortion is mainly caused by the ZCD signal propagation time delay, and the ac line zero-crossing current spike is mostly due to the noise current generated from the switching dv/dt of Si devices (S_3, S_4). The inductor current spike due to the asynchronous Si device switching instant happens in the first switching cycle after the blanking time, which has limited impact on the input current THD. PFC_WPT, however, is impacted by the high dv/dt noise generated from the 6.78 MHz WPT system and therefore suffers from more severe line-cycle current distortion and unstable control with current runaway.

B. Experimental Verification of the Line-Cycle Current Distortion and Mitigation

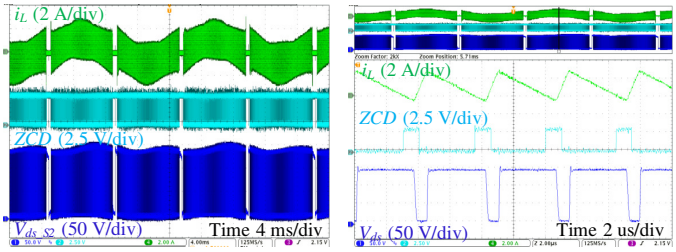
For the two PFC prototypes, the ZCD signal propagation delay is first compensated by embedding the modified converter model in the real-time calculation. As shown in Fig. 26, with the compensation, the line-cycle current distortion is almost remedied for PFC_DC, except for occasional inductor current spike after the blanking time (Fig. 26(b)). However, for PFC_WPT, the inductor current is still severely distorted due to the noise impact, which has a similar waveform as Fig. 25(b). Fig. 27 presents zoomed-in waveforms and the measured ZCD signal time delay of PFC_WPT in the WPT system. The ZCD signal is coupled with high-frequency noise, and has large and varying time delay within a line cycle.

To reduce the noise impact on the ZCD signal, system CM impedance and the ZCD circuit noise rejection level should be improved. Considering the limited converter space of the high-density power supply, additional CM filter or CM choke are not desired. For the WPT system, the CM impedance



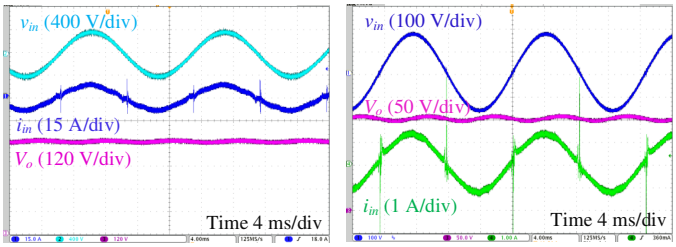
(a) (b) (c)

Fig. 28. IMN inductor. (a) Original single L_{IMN}; (b) Coupled L_{IMN}; (c) Coupled L_{IMN} with higher CM impedance.



(a) (b)

Fig. 29. Tested inductor current and ZCD signal of PFC_WPT with noise mitigation; (a) Inductor current; (b) ZCD signal.



(a) (b)

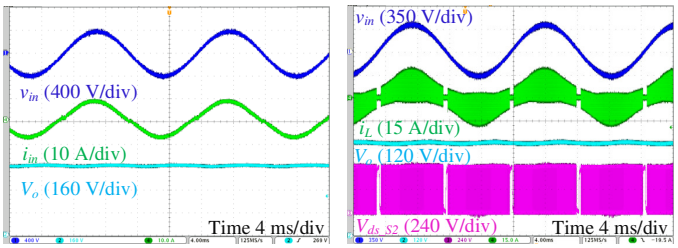
Fig. 30. Experimental waveforms of the PFC prototypes with mitigated line-cycle current distortion. (a) PFC_DC at 1.5 kW; (b) PFC_WPT at 100 W.

can be increased by adjusting the impedance matching network (IMN) tank to an L-C-L structure rather than an L-C structure. As shown in Fig. 28, L_{IMN} is reconfigured to a coupled inductor with the same inductance in the DM loop. To reach a higher CM impedance, a lower coupling coefficient k is achieved by dividing the windings to opposite directions of the low-permeability core (Fig. 28(c)). As presented in Table III, using the same core and winding wire, the CM impedance varies widely under various winding configurations. In the ZCD circuit, feedback resistors measured with lower than 1% error are selected for the amplifier to keep high CMRR, and the RC filters are carefully enlarged and balanced to help suppress the noise impact.

TABLE III. Impedance of different IMN inductors in Fig. 28.

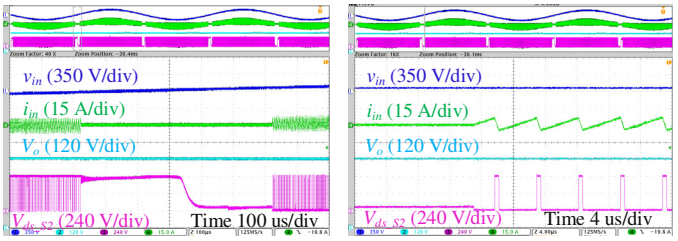
L_{IMN}	a	b	c
L_{DM}	1.68 uH	1.68 uH	1.68 uH
L_{CM1}	1.68 uH	0.55 uH	0.73 uH
L_{CM2}	0 uH	0.57 uH	0.7 uH
k	0	0.4822	0.1816

Fig. 29 displays the testing waveforms of PFC_WPT with noise mitigation. Not only is the ZCD signal clean, but also the varying time delay is eliminated. The inductor current is balanced and undistorted along the line cycle, and the PFC converter is able to operate at full load with target voltage and power. Fig. 30 shows the full-load experimental waveforms



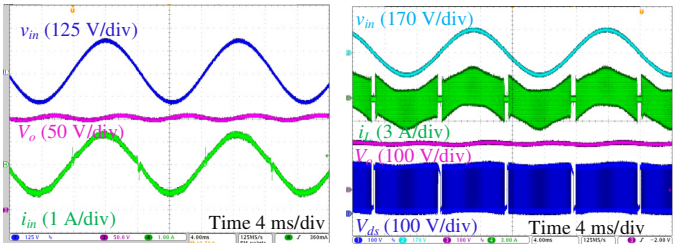
(a) (b)

Fig. 31. Experimental waveforms of PFC_DC at 1.5 kW with the proposed mitigation methods for current distortion.



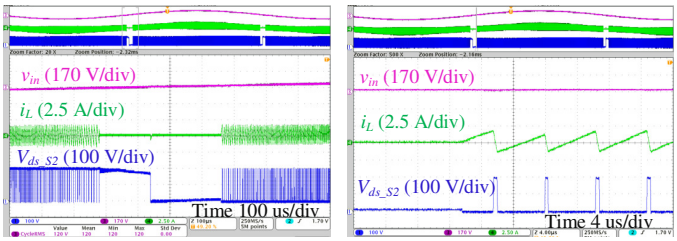
(a) (b)

Fig. 32. Ac line zero-crossing transition waveforms of PFC_DC with the proposed mitigation methods for current distortion. (a) Negative-to-positive transition; (b) Device turn-on waveforms in the positive half line cycle.



(a) (b)

Fig. 33. Experimental waveforms of PFC_WPT at 100 W in the 6.78 MHz WPT system with the proposed mitigation methods for current distortion.



(a) (b)

Fig. 34. Ac-line zero-crossing transition waveforms of PFC_WPT with the proposed mitigation methods for current distortion. (a) Negative-to-positive transition; (b) Device turn-on waveforms in the positive half line cycle.

of PFC_DC at 1.5 kW and PFC_WPT at 100 W with the mitigated line-cycle current distortion.

C. Experimental Verification of the Ac Line Zero-Crossing Current Spike and Mitigation

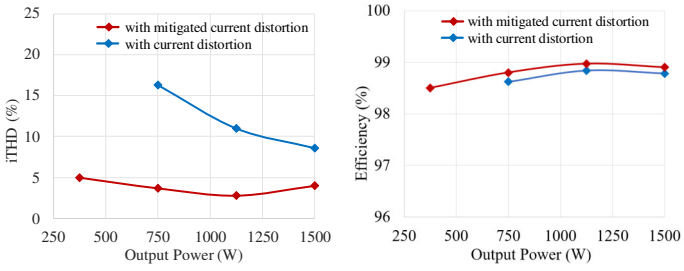
As presented in Fig. 30, large current spikes still exist in the input current. Also, when turning on GaN devices after the blanking time, large peak inductor current happens in the first switching cycle, as shown in Fig. 26(b).

To avoid the inductor current spike and ensure soft switching in each switching cycle, the proposed device switching sequence during the blanking time is implemented in both PFC prototypes. For PFC_DC, the proposed auxiliary circuit is adopted to eliminate the current spike induced by the dv/dt noise of Si devices S_3, S_4, where Q_1 and Q_2 conduct for 100 μs during the blanking time. Fig. 31 and Fig. 32 present the final experimental results of PFC_DC at full load. With 277 V_{ac} input, the output voltage is regulated at 480 V_{dc}, and full-line-cycle ZVS is achieved. Thanks to the damping circuit, the drain-to-source voltage is gradually changed with low dv/dt, and the input current spike is removed. Meanwhile, the GaN device is turned on with soft switching, and no current spike occurs in the first switching cycle.

For the high-density transmitter of the WPT system, adding an auxiliary circuit is not preferable. Hence, the CM choke of the EMI filter is built with a nanocrystalline core and high CM impedance to stop the noise current from polluting the input source. Fig. 33 and Fig. 34 show the full-load experimental results of PFC_WPT in the 6.78 MHz WPT system. With 120 V_{ac} input, the output voltage is regulated at 200 V_{dc} with reliable ZVS control. The ac line zero-crossing current spike is significantly attenuated with the heavier CM filter, but cannot be completely removed. As shown in Fig. 34, the high dv/dt still exists in v_{ds} when the Si devices S_3, S_4 switch, but no large inductor peak current or hard switching occurs when GaN devices are turned on.

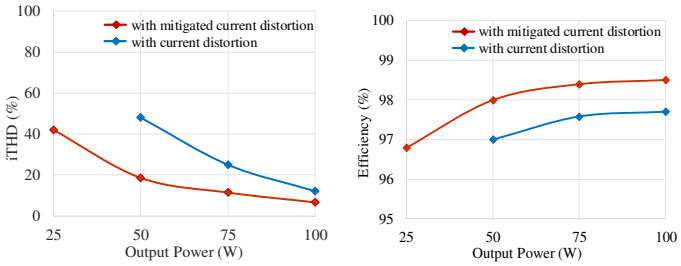
D. Comparison of the PFC Efficiency and Current THD

To further show the effectiveness of the proposed methods for reducing current distortion and power loss, the input current total harmonic distortion (iTHD) and converter efficiency are measured using a Yokogawa WT3000E power analyzer. Fig. 35 and Fig. 36 present the testing results at different loads of the two PFC prototypes. The blue curve represents the original testing result with current distortion, and the red curve is the result with the proposed methods for current distortion mitigation. As shown in Fig. 35(a), iTHD of PFC_DC is above 9.8% before mitigation. By adopting the ZCD signal time delay compensation, specified device switching sequence with blanking time, and the auxiliary circuit for current spike elimination, current THD is reduced below 5% at all tested loads. Because of the compensated ZCD signal time delay, inductor current ripple is decreased, leading to lower power loss and 99% peak efficiency. For PFC_WPT, noise immunity



(a) (b)

Fig. 35. Measured iTHD and efficiency of PFC_DC at different loads with and without the proposed mitigation methods for current distortion. (a) Measured iTHD; (b) Measured power efficiency.



(a) (b)

Fig. 36. Measured iTHD and efficiency of PFC_WPT at different loads with and without the proposed mitigation methods for current distortion. (a) Measured iTHD; (b) Measured power efficiency.

approaches including balanced IMN impedance and precision resistors in the ZCD circuit are first implemented to ensure the operation at target power and voltage ratings. Then, ZCD signal time delay compensation, specified device switching sequence, and sufficient input CM choke are employed to mitigate the current distortion. As shown in Fig. 36, in each testing loading point, the current THD is reduced by half, and converter efficiency is improved by 1% point compared to the case with current distortion.

V. Conclusions

This paper first systematically studies and addresses the current distortion issues of the GaN-based CRM totem-pole PFC converter with ZVS control. The input current is predominantly distorted by the line cycle current distortion and the current spike during the ac line zero crossing, which result from the high-frequency current ZCD signal sensing delay, high dv/dt switching noise, and switch timing asynchronization in practical implementations. Origins of current distortion are discussed, and approaches are proposed to mitigate the distortion and ensure stable operation. Implementation of the proposed methods are straightforward, and no extra control resources are required.

The current distortion and mitigation methods are validated experimentally on a 1.5 kW GaN-based CRM PFC for data centers and a 100 W CRM PFC in a GaN-based 6.78 MHz wireless charging power supply for consumer electronics. With the proposed methods, iTHD at full load is reduced from 9.8% to 3.2% for PFC_DC and from 12.12% to 6.6% for PFC_WPT. Also, converter peak power efficiency is improved from 98.8% to 99% for PFC_DC and from 97.7% to 98.5% for PFC_WPT.

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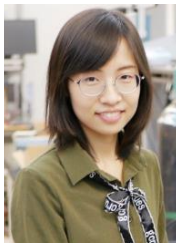

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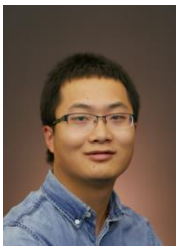

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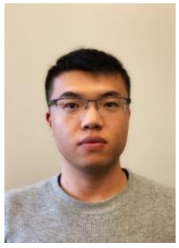

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