A GaN-Based CRM Totem-Pole PFC Converter with Fast Dynamic Response and Noise Immunity for a Multi-Receiver WPT System

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***Abstract*—The soft-switching gallium-nitride (GaN) based critical conduction mode (CRM) totem-pole power factor correction (PFC) converter is a good candidate for the front-end rectifier in wireless power transfer (WPT) applications. In multi-receiver MHz WPT systems, the PFC converter is required to have fast dynamic response and noise immunity. In this work, a GaN-based CRM totem-pole PFC converter is designed for a multi-receiver wireless charging power supply. Digital-based variable on-time control is used to achieve the zero voltage switching (ZVS) within the whole line cycle, and a voltage-loop controller with notch filters is designed to improve the transient response. The impact of high-frequency noise on the sensing signals and ZVS control are analyzed, and implementation methods are proposed to mitigate the disturbances. A GaN-based CRM totem-pole PFC that is demonstrated with 98.5% full-load efficiency is built as the first stage in the transmitter of a 100 W 6.78 MHz multi-receiver WPT system. The noise immunity of the CRM PFC is verified by testing the whole WPT system. Experimental results show that the system end-to-end efficiency at full load is 90.16%, and fast dynamic response is achieved during load variation.**

***Index Terms*—GaN, CRM, totem-pole PFC, ZVS, WPT, fast dynamic response, noise immunity**

I. Introduction

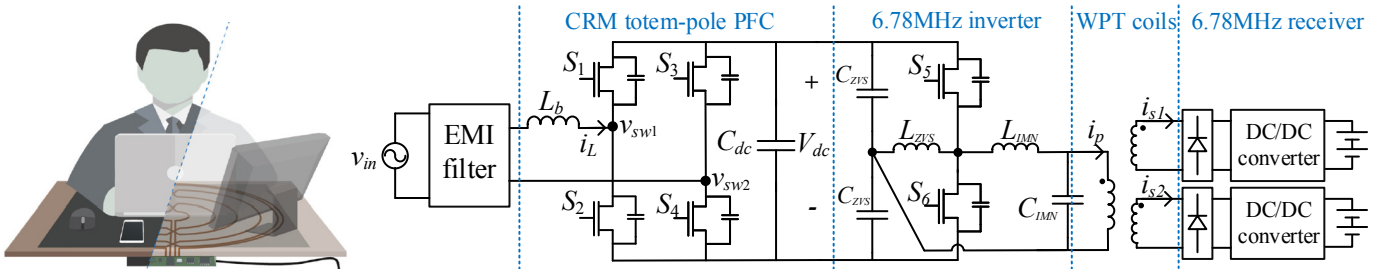
Wireless power transfer (WPT) based on MHz magnetic resonant coupling has gained increasing attention in applications like consumer electronics and electric vehicles, due to the advantages of spatial freedom, long transfer distance, and high efficiency [1], [2]. In order to maximize the end-to-end efficiency and power density, research efforts are made on transmission coil optimization [3], and advanced power conversion techniques with two-stage or single-stage transmitters [4] and receivers [5]. To also satisfy the power factor and harmonic requirements, a high-efficiency power factor correction (PFC) converter is required.

Recently, the gallium-nitride (GaN) based totem-pole PFC converter has been studied in front-end rectifiers, because of the simple topology, low conduction loss, and high utilization of devices and components [6], [7]. With the critical conduction mode (CRM) operation, zero voltage switching (ZVS) or valley swiching can be achieved [8]. To further reduce the switching loss for achieving higher efficiency and power density, ZVS control strategies are developed to realize soft switching within the whole line cycle [9]–[11]. The soft-switching CRM totem-pole PFC has been applied on MHz WPT systems and reported with $> 98\%$ high efficiency [12].

However, MHz wireless charging brings in new requirements and challenges for the GaN-based CRM totem-pole PFC design. On the one hand, for WPT systems, especially the ones allowing multiple devices to charge simultaneously, fast dynamic response is indispensable. This requirement can be realized by regulating the inverter with constant output current behavior [12], but this technique relies on a constant DC bus voltage at the input of the inverter. Also, the voltage-loop control bandwidth of the single-phase rectifier is usually designed well below the line frequency (typically < 20 Hz), which is limited by the twice-line frequency ripple on the DC bus. To improve the dynamic response during load changing, higher-bandwidth control schemes should be investigated [13], [14], and adopted in the CRM totem-pole PFC converter.

On the other hand, ZVS control of the CRM PFC requires instantaneous voltage sensing and high-frequency current sensing. In the MHz switching system, high *dv/dt* noise is easily coupled into the sensing signals electrically and magnetically [15], resulting in erroneous switching actions and fragile ZVS control [16]. The noise impact is even more severe in multi-receiver WPT systems with MHz magnetic resonant coupling and large coils. Parasitic capacitance exists between the transmitter coil and receiver coils, also between the WPT coils and the ground, which transfers the noise current from the primary side to the load side, and from the coil to the ground. Involved in the resonant tank, the noise current has 6.78 MHz resonant ripple, and can be propagated to the PFC stage and disrupt the sensing signals. Therefore, a front-end totem-pole PFC with noise immunity is required to maintain reliable ZVS control.

In this paper, a GaN-based CRM totem-pole PFC converter with fast dynamic response and low sensitivity to noise is developed for a 100 W 6.78 MHz multi-receiver wireless charging power supply in consumer electronics. Fig. 1(a)



(a) (b)

Fig. 1. (a) Example application of the multi-receiver WPT power supply; (b) GaN-based multi-receiver wireless power supply system.

presents the example application of the WPT power supply, where computer mouse, cellphone, display, and laptop are powered simultaneously on one transmission desk. Fig. 1(b) shows the circuit topology of the WPT system, which includes a two-stage transmitter consisting of a CRM totem-pole PFC and a 6.78 MHz half-bridge inverter, WPT coils, and receiver-side diode rectifiers.

The paper is organized as follows. Section II introduces the operation principle and ZVS control of the GaN-based CRM totem-pole PFC. Section III provides the digital-based variable on-time control with high bandwidth and notch filters for enhancing the transient response. In section IV, hardware implementation is introduced, high-frequency noise impacts on the sensing signals are analyzed, and solutions to mitigate the noise disturbances are proposed. Section V shows the experimental results, and section VI gives the conclusions.

II. Operation Principle of the CRM Totem-Pole PFC with Full-Line-Cycle ZVS

As shown in Fig. 1(b), for the totem-pole PFC, GaN devices S_1 and S_2 operate at high frequency, and S_3 and S_4 work at AC line frequency. During the positive half line cycle, S_4 is always on, S_3 is always off, S_2 is the active switch (AS), and S_1 is the synchronous switch (SS). During the negative half line cycle, S_3 is always on, S_4 is always off, S_1 is the active switch, and S_2 is the synchronous switch.

The operation principle of the CRM totem-pole PFC is illustrated with the theoretical operation waveforms shown in Fig. 2 and the state-plane trajectories shown in Fig. 3. Discussion here is based on the operation within the positive half line cycle, with the assumption that V_{in} is nearly-constant in one switching cycle. For the state-plane trajectories, V_{bound} is the boundary input voltage between the natural ZVS region and the non-natural ZVS region. The characteristic impedance Z_n is defined as $Z_n^2 = {}^{L_b}/_{(2C_{oss})}$, where C_{oss} is the equivalent drain-to-source capacitance of S_1 and S_2, assuming $C_{oss,S1} = C_{oss,S2} = C_{oss}$. The resonance angular frequency is designated as $w_r^2 = {}^{1}/_{(2C_{oss}L_b)}$.

As illustrated in Fig. 2, to achieve ZVS within the full line cycle, conduction time of the synchronous switch S_1 is purposely extended for $T_{ex,SS}$. In the natural ZVS region when $V_{in} \le V_{bound}$, $T_{ex,SS}$ is not needed, and S_1 is turned off at the positive-to-negative zero current crossing point, t_0.

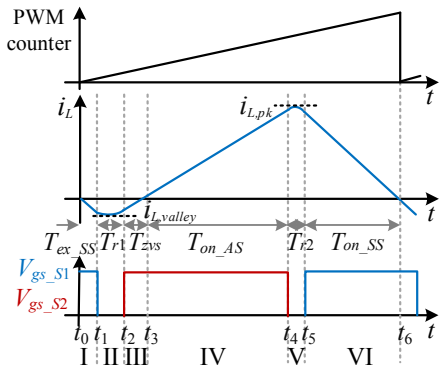
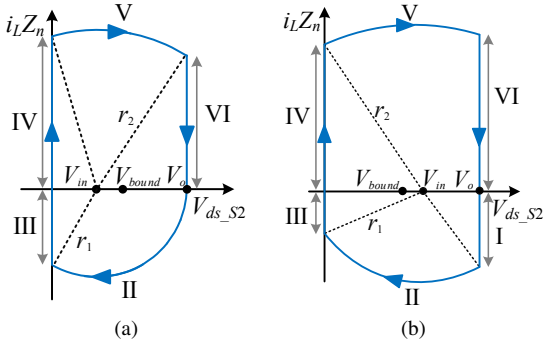


Fig. 2. Inductor current and device gate signals within one switching period in the positive half-line cycle.



(a) (b)

Fig. 3. State-plane trajectory with the full-line-cycle ZVS modulation. (a) When $V_{in} \le V_{bound}$. (b) When $V_{in} > V_{bound}$.

When $V_{in} > V_{bound}$, S_1 conduction time is prolonged until t_1 to increase the energy stored in the inductor, so that the active switch S_2 drain-to-source voltage $V_{ds,S2}$ is able to resonate to zero before turning on S_2, and ZVS is maintained.

Based on the state plane in Fig. 3, ZVS operation is achieved as long as r_1 is larger than V_{in}. Hence, the adaptive ZVS margin is defined as

$$k = \frac{r_1}{V_{in}} = \begin{cases} \frac{V_o - V_{in}}{V_{in}}, & V_{in} \le V_{bound} \\ k_0, & V_{in} > V_{bound} \end{cases} \quad (1)$$

where $V_{bound} = {}^{V_o}/_{(k_0+1)}$, and k_0 is the selected ZVS margin which is slightly larger than 1. The value of k_0 cannot be too large, because large ZVS margin means more negative inductor

current, hence larger RMS current and conduction loss. Accordingly, the extended conduction time of the synchronous switch is

$$T_{ex\_SS} = \frac{\sqrt{(k^2-1)V_{in}^2 - V_o^2 + 2V_oV_{in}}}{w_r(V_o - V_{in})} \tag{2}$$

When $V_{in} \le V_{bound}$, $T_{ex\_SS} = 0$; when $V_{in} > V_{bound}$, $T_{ex\_SS} > 0$.

Then, during the first resonant time T_{r1}, both S_1 and S_2 are off, $V_{ds,S2}$ decreases from V_o to zero, and inductor current i_L resonates through the minimum value, $i_{L,valley}$.

$$i_{L,valley} = -\frac{kV_{in}}{Z_n} \tag{3}$$

After the resonant time T_{r1}, a small ZVS time margin T_{zvs} is provided. S_1 is turned on during T_{zvs}. The inductor is then charged by the input voltage until turning off S_2 at t_4. During the second resonant time T_{r2}, $V_{ds,S1}$ decreases from V_o to zero, and i_L resonates through the peak value, $i_{L,pk}$.

$$i_{L,pk} = \frac{V_{in}}{L_b}T_{on\_AS} \tag{4}$$

With the previous resonance, S_1 is turned on with ZVS at t_5, and the inductor is discharged by the output voltage. A PWM time-based counter is reset on the positive-to-negative zero current point t_6 and starts a new switching period.

Since the resonant time intervals are very short, the inductor current can be approximated as a triangular waveform with average value $i_{L,ave} \approx {}^{(i_{L,pk}+i_{L,valley})}/_2$. Assuming $v_{in} = \sqrt{2}V_{in,rms}\sin\omega t$ and $i_{in} = \left(\sqrt{2}P_o/(\eta V_{in,rms})\right)\sin\omega t$, the active switch conduction time T_{on_AS} is given by letting $i_{in} = i_{L,ave}$.

$$T_{on\_AS} = \frac{2P_oL_b}{\eta V_{in,rms}^2} + \frac{k}{w_r} \tag{5}$$

where η is the converter efficiency, $T_{on\_c} = {}^{2P_oL_b}/\left(\eta V_{in,rms}^2\right)$ is constant at a steady-state operation, and $T_{on\_v} = {}^{k}/_{w_r}$ varies simultaneously with the the input voltage. More detailed calculations of the time intervals are available in [11].

III. Digital-Based Variable On-Time Control with Fast Dynamic Response

A. Digital-Based Variable On-Time Control

To realize the full-line-cycle ZVS, digital-based variable on-time control is implemented. Fig. 4 presents the control structure with a digital signal processor (DSP). The input voltage v_{in}, output voltage V_o, and the inductor positive-to-negative zero current point are sensed through hardware circuits. In the DSP, a proportional integral (PI) controller regulates V_o in the outer loop, and generates the on time T_{on_c} to control the peak inductor current. Meanwhile, PWM switching time intervals are calculated in real time based on the converter model and sensed voltage signals. The zero current detection (ZCD) signal is used to reset the PWM timer and limit the minimum current stress. Based on the time

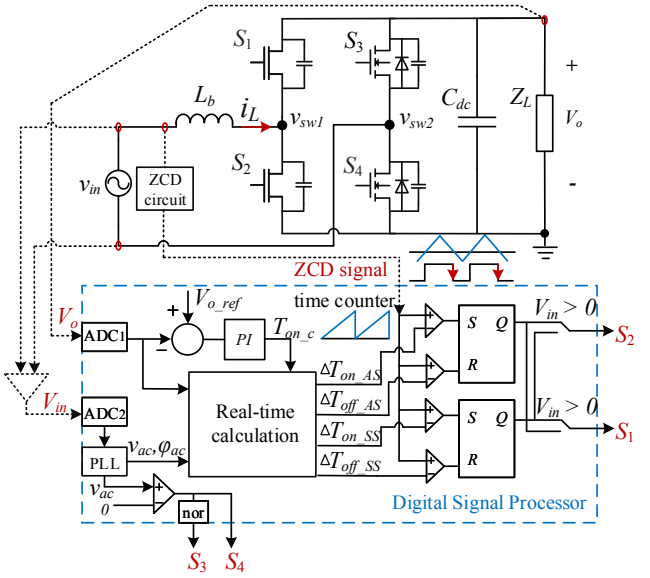


Fig. 4. Structure of the digital-based variable on-time control for the CRM totem-pole PFC.

reference, devices S_1 and S_2 are turned off and on after the associated time delays.

$$\begin{cases} \Delta T_{off\_SS} = T_{ex\_SS} \\ \Delta T_{on\_AS} = T_{ex\_SS} + T_{r1} \\ \Delta T_{off\_AS} = \Delta T_{on\_AS} + T_{zvs} + T_{on\_AS} \\ \Delta T_{on\_SS} = \Delta T_{off\_AS} + T_{r2} \end{cases} \tag{6}$$

In addition, control signals for S_3 and S_4 are based on a phase locked loop (PLL) and are switched at line frequency.

B. Voltage-Loop Controller Design with Notch Filters

As aforementioned, the peak inductor current is controlled by the on time T_{on_AS} which is composed of two parts, $T_{on\_AS} = T_{on\_c} + T_{on\_v}$, where T_{on_c} is the part generated from the low-bandwidth PI controller, and T_{on_v} is the variable part based on the real-time calculation. When $V_{in} > V_{bound}$, $T_{on\_v} = 0$ and $T_{on\_AS} = T_{on\_c}$. Hence, the voltage-loop controller is easier to be designed during the non-natural ZVS region with $V_{in} > V_{bound}$. Here, we pick the peak input voltage point to design the voltage controller.

The on-time-to-output open-loop transfer function is required for the controller design. Since $|i_{L,valley}| \ll |i_{L,pk}|$, the average inductor current can be simplified as

$$i_{L,ave} \approx \frac{1}{2}i_{L,pk} = \frac{1}{2}\frac{V_{in}}{L_b}T_{on\_c} \tag{7}$$

Applying KCL law on the output network, we get

$$C_{dc}\frac{dv_o}{dt} = i_{L,ave}d' - \frac{v_o}{R_L} \tag{8}$$

where the duty cycle $d' \approx \frac{v_{in}}{v_o}$ for the boost converter.

Implementing perturbation and linearization on (7) and (8), the small-signal result is

$$\hat{i}_{L,ave} = \frac{V_{in}\hat{t}_{on\_c} + \hat{v}_{in}T_{on\_c}}{2L_b} \tag{9}$$

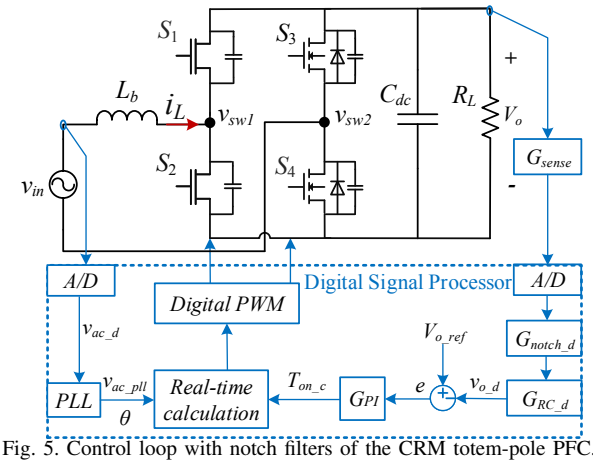


Fig. 5. Control loop with notch filters of the CRM totem-pole PFC.

$$C_{dc}V_o\frac{d\hat{v}_o}{dt} = V_{in}\hat{i}_{L,ave} + \hat{v}_{in}I_{L,ave} - \frac{2V_o\hat{v}_o}{R_L} \quad (10)$$

Inserting (9) into (10), and rearranging it in the s domain, we obtain

$$(sC_{dc}V_o + \frac{2V_o}{R_L})\hat{v}_o = \frac{V_{in}^2}{2L_b}\hat{t}_{on\_c} + (I_{L,ave} + \frac{V_{in}T_{on\_c}}{2L_b})\hat{v}_{in} \quad (11)$$

Then, the on-time-to-output transfer function is

$$G_{vt} = \frac{\hat{v}_o}{\hat{t}_{on\_c}}\bigg|_{\hat{v}_{in}=0} = \frac{V_{in}^2R_L}{4V_oL_b}\frac{1}{1+s\frac{R_LC_{dc}}{2}} \quad (12)$$

Since the open-loop transfer function has only one pole, a PI controller is enough to compensate the loop. In order to improve the transient response, higher control bandwidth is desired. To avoid the impact of the double-line frequency ripple, digital notch filters are applied on the output voltage feedback loop. Because the whole circuit operates with 60 Hz AC line input, notch filters with stop bands at 60 Hz and 120 Hz are implemented. As depicted in Fig. 5, assuming the analog-to-digital (*A/D*) conversion gain and the PWM modulation gain are cancelled out, the final loop gain of the voltage control loop is

$$T_v = G_{sense}G_{notch\_d}G_{RC\_d}G_{PI}G_{vt} \quad (13)$$

where G_{RC_d} is the digital low-pass filter for noise suppression. Fig. 6 shows the bode plot of the PFC loop gain at peak input voltage. The PI compensator is designed to have 160 Hz control bandwidth with a phase margin of 65°.

IV. Implementation Considerations for Noise Immunity

A. Hardware Implementation

A prototype of a GaN-based 100 W muiti-receiver wireless charging power supply system is developed and shown in Fig. 7. The WPT system contains a two-stage transmitter, a 0.5×0.5 m^2 transmitter desk, receiver coils, and two diode receivers. The two-stage transmitter is composed of EMI filters, a CRM totem-pole PFC converter, and a 6.78 MHz inverter with total volume at $7.4 \times 5.3 \times 1.7$ cm^3. Detailed specifications of the transmitter are listed in Table I.

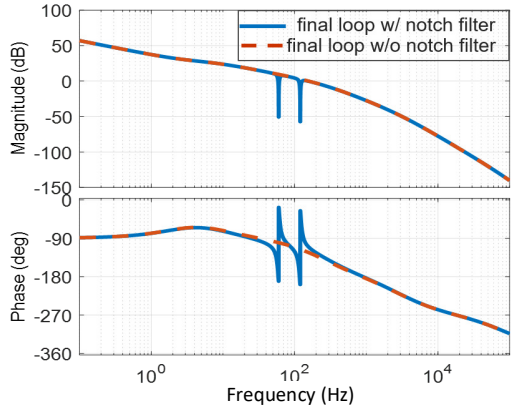


Fig. 6. Bode diagram of the CRM PFC voltage loop gain with and without notch filters.

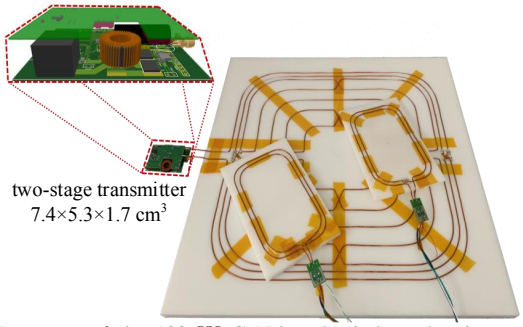
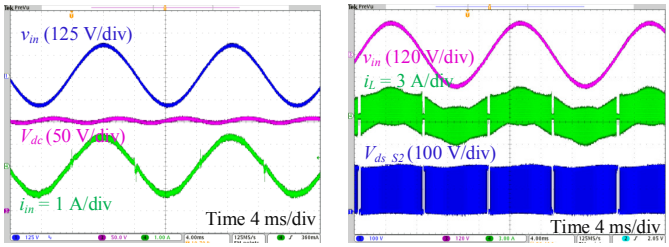


Fig. 7. Prototype of the 100 W GaN-based wireless charging system for consumer electronics.

To validate the PFC operation, 6.78 MHz inverter and WPT coils are disconnected, and the CRM PFC is first tested with a resistor load. Fig. 8 shows the full-load experimental waveforms. With the ZVS control, both the inductor current and DC bus voltage are well regulated. Based on the measurement with the power analyzer Yokogawa WT3000E, the PFC achieves 98.5% efficiency, 0.994 power factor, and 6.6% input current total harmonics distortion (THD) at full load.

TABLE I. Specifications of the transmitter for the WPT system.

Parameter	Value
Input voltage v_{in}	120 V_{ac}, 60 Hz
DC bus voltage V_{dc}	200 V_{dc}
Output power P_o	100 W
PFC switching frequency $f_{s,pfc}$	187 – 725 kHz
Inverter switching frequency $f_{s,inv}$	6.78 MHz
GaN devices $S_1 - S_4$	GS66508B, 650 V
PFC ZVS margin	$k_0 = 1.1$, $T_{zvs,min} = 50$ ns



(a) (b)

Fig. 8. Experimental waveforms of the CRM PFC at full-load without the inverter and WPT coils.

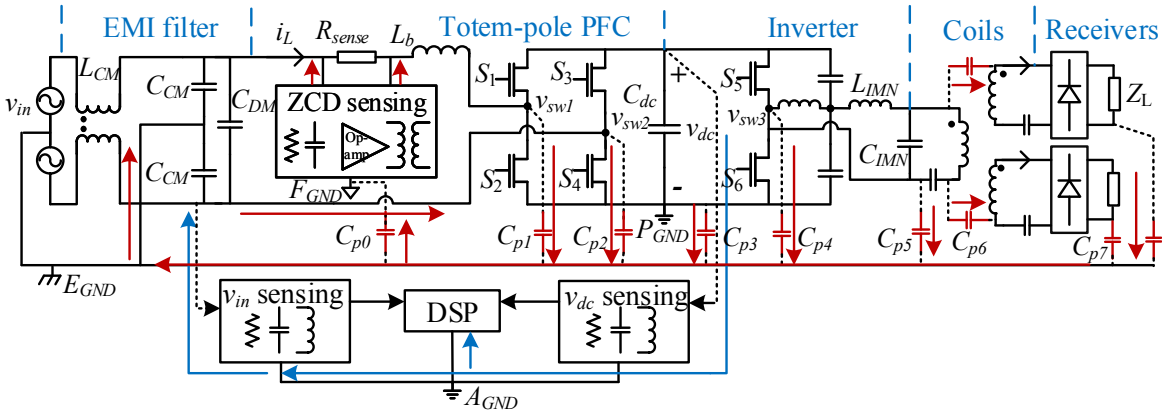
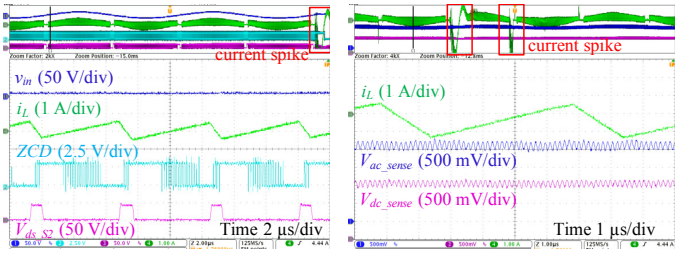
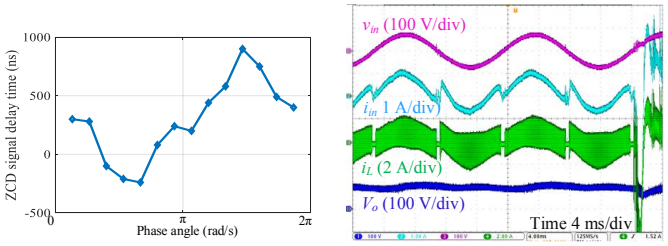


Fig. 9. Noise propagation path within the WPT system.



(a) (b)

Fig. 10. Tested PFC sensing signals with 6.78 MHz inverter and WPT coils. (a) ZCD signal with high-frequency noise. (b) Voltage sensing signals with high-frequency noise.



(a) (b)

Fig. 11. PFC testing results with 6.78 MHz inverter and WPT coils. (a) Varying and asymmetrical ZCD time delay. (b) Distorted PFC currents.

B. High-Frequency Noise Impacts on Sensing Signals

However, when connected to the 6.78 MHz inverter and WPT coils, the PFC operation degrades due to the impact of noise. As shown in Fig. 10, high-frequency noise is coupled on the ZCD signal and voltage sensing signals, leading to inaccurate PWM calculation and erroneous ZCD reset. As a result, anomalous switching actions occur, and the ZVS control becomes unstable with large current spikes.

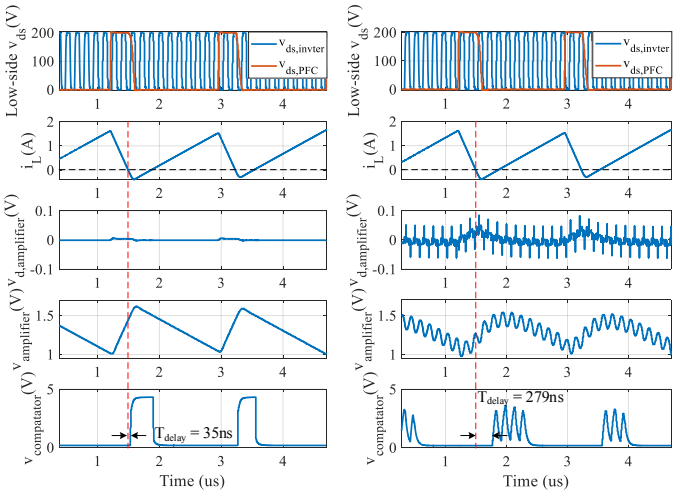
Apart from the high-frequency noise coupling, the ZCD signal has varying and asymmetrical time delay. Fig. 11(a) shows the tested ZCD signal time delay. The delay time has large line-cycle ripple and reaches up to 900 ns at the peak point. Consequently, the PFC currents are seriously distorted as presented in Fig. 11(b). Due to the noise impact, over-current protection is triggered, and the PFC is incapable of working at the target voltage and power rating.

C. Analysis of the Noise Propagation

To understand the reason for the noise impacts on sensing signals, common-mode (CM) noise propagation paths within the power supply system are analyzed, as illustrated in Fig. 9. High dv/dt noise is generated by the switching nodes v_{sw1}, v_{sw2}, v_{sw3}, and the resulting noise currents flow to the common reference ground (E_{GND}) through parasitic capacitance C_{p1}, C_{p2}, C_{p4}. Since the transmitter coil has large area, parasitic capacitance C_{p5} between the coil and ground cannot be neglected. Parasitic capacitance C_{p6} between the transmitter coil and receiver coils transfers the noise current from the primary side to the load side, and further injects the noise current into the ground via C_{p7}. The noise currents carried by C_{p6} are involved in the resonant tank of the WPT coils. Hence, the current injected to the ground through C_{p7} has 6.78 MHz resonant ripple. In addition, capacitance C_{p3} between the power ground (P_{GND}) and E_{GND} also contributes to the noise propagation.

The noise currents are then transferred to the input side, and flow back forming a complete conduction loop. Ideally, all the noise currents can be picked up by C_{CM} in the EMI filter, and the sensing circuits will not be influenced. However, constrained by the allowable leakage current [17], the total values of C_{CM} may not be sufficient to absorb all the noise current, especially the large amount of 6.78 MHz noise. So partial noise is propagated to the sensing circuits. Due to the ground connection shown in [18], sensing circuits of v_{ac} and V_{dc} share the same analog ground A_{GND}, and the high-frequency noise from the power stage is easily transferred to the voltage sensing circuits and the digital controller.

A ZCD circuit based on a sensing resistor R_{sense} is adopted, where R_{sense} is connected in series with the input power line [16]. The inductor current is detected in each switching cycle, and the ZCD circuit is very sensitive in the high-frequency environment. Although isolation is adopted to seclude the floating ground (F_{GND}), part of the noise current still flows into F_{GND} through parasitic capacitance C_{p0}, and the sensing signals are further distorted. Fig. 12 shows the simulated results of current sensing signals in the ZCD circuit. In the ideal case, the amplifier input differential signal $v_{d,amplifier}$



(a) (b)

Fig. 12. Simulated signals of the amplifier and comparator in the ZCD circuit. (a) Normal signals. (b) Distorted signals with noise impact.

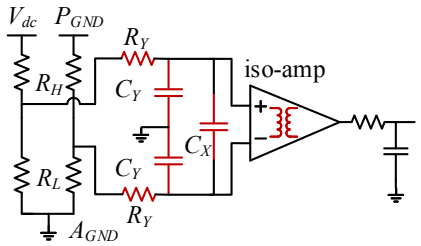


Fig. 13. Differential voltage sensing circuit with EMI filters.

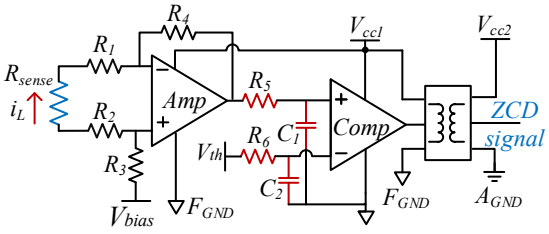


Fig. 14. ZCD circuit.

is nearly zero, and the amplifier output $v_{amplifier}$ is a clean triangular waveform following the inductor current. Accordingly, the comparator generates clean ZCD signal with small propagation delay time of 35 ns (Fig. 12(a). Nevertheless, with the noise impact, $v_{d,amplifier}$ is coupled with not only the switching noise from the switching nodes, but also the 6.78 MHz resonant ripple from the WPT coils. The CM noise is converted into differential mode (DM) noise, and $v_{amplifier}$ is distorted with high-frequency resonant ripple and a small DC bias. As a result, the ZCD signal from the comparator is noisy and has much longer time delay of 279 ns. In AC-DC operation, 60 Hz line-cycle ripple is also reflected on the noise current, and further distorts the amplifier output, leading to the line-cycle varying ZCD time delay as shown in Fig. 11(a).

D. Proposed Methods for Noise Immunity

1) Isolated Sensing Circuit with Filter

To suppress the high-frequency noise coupled on v_{ac} and V_{dc} sensing, voltage sensing circuits with EMI filters and high common-mode transient immunity (CMTI) isolated amplifiers are used, as depicted in Fig. 13. The bandwidths of the EMI filters should be designed between the voltage control bandwidth and the high switching frequency to avoid the apparent filtering delay on the feedback loop. Since the noise is predominately in the MHz in the WPT system, a filter corner frequency in a few kHz is sufficient to filter out the noise and has no impact on the feedback control. For the differential voltage sensing circuit, the voltage divider resistors should be considered in the EMI filter design. Corner frequencies of the CM and DM filters are determined as

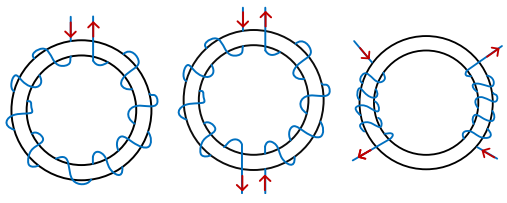
$$f_{CM} = \frac{1}{2\pi(R_H||R_L + R_Y)C_Y} \tag{14}$$

$$f_{DM} = \frac{1}{2\pi(R_H||R_L + R_Y)(C_Y + 2C_X)} \tag{15}$$

In order to avoid the erroneous ZCD signal due to the high-frequency noise, RC filters are placed on the input terminals of the comparator in the ZCD circuit, as shown in Fig. 14. Also, a symmetrical configuration with $R_5 = R_6$ and $C_1 = C_2$ is employed to balance and improve the CM impedance.

2) Balanced and High CM Impedance

To eliminate the varying ZCD time delay and prevent the CM noise from flowing to the ZCD circuit, a large and balanced CM impedance should be inserted in the middle of the system circuit. Typically, a EMI filter with larger CM choke on the DC bus is effective. However, with the limited converter size for such high-density power supply, an extra EMI filter is not desired. For the WPT application, the impedance matching network (IMN) tank can be adjusted to an L-C-L configuration instead of an L-C structure. As illustrated in Fig. 15, L_{IMN} is modified from a single inductor to a coupled inductor with the same inductance on the DM loop. To achieve higher CM impedance, a lower coupling coefficient k is realized by separating the windings to opposite ends of the low-permeability core (Fig. 15(c)). As listed in Table II, for the same core and winding wire, the CM impedance varies widely with different inductor structures.



(a) (b) (c)

Fig. 15. IMN inductor. (a) Original single L_{IMN}. (b) Coupled L_{IMN}. (c) Coupled L_{IMN} with higher CM impedance.

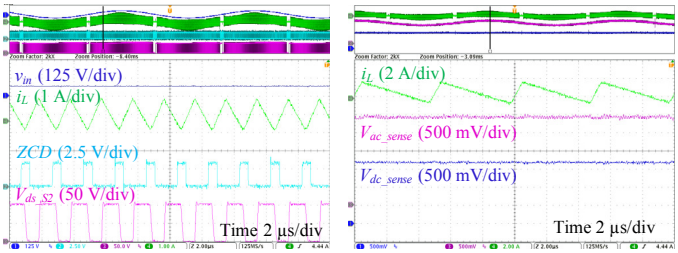
TABLE II. Impedance of the different IMN inductors

L_{IMN}	a	b	c
L_{DM}	1.68 uH	1.68 uH	1.68 uH
L_{CM1}	1.68 uH	0.55 uH	0.73 uH
L_{CM2}	0 uH	0.57 uH	0.7 uH
k	0	0.4822	0.1816

V. Experimental Verification

As previously demonstrated, combined with the 6.78 MHz inverter and WPT coils, the CRM PFC cannot operate normally because of the noise impact (Fig. 11). To enhance the operation performance, the proposed noise immunity approaches are implemented, including the isolated voltage sensing circuits, filters, and the modified IMN inductor.

Both the current and voltage sensing signals are much cleaner, and the ZCD signal varying time delay is eliminated, as shown in Fig. 16. The CRM PFC is able to operate reliably in the 6.78 MHz WPT system. Fig. 17 and Fig. 18 present the tested PFC waveforms in the full-load operation of the WPT system. With 120 V_{ac} input voltage, the PFC generates 200 V DC bus voltage, and realizes ZVS within the whole line cycle. Based on the measurement with the power analyzer Yokogawa WT3000E, the tested end-to-end power efficiency of the WPT power supply system is 90.16%.



(a) (b)

Fig. 16. Improved PFC sensing signals with 6.78 MHz inverter and WPT coils. (a) Clean ZCD signal. (b) Clean voltage sensing signals.

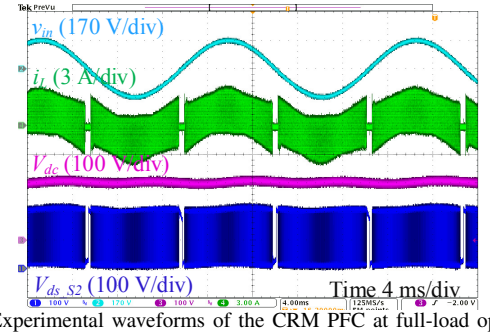
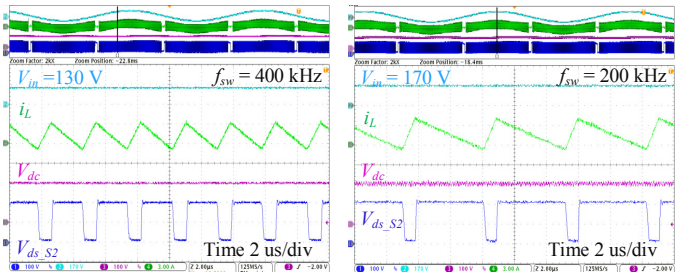


Fig. 17. Experimental waveforms of the CRM PFC at full-load operation of the 100 W 6.78 MHz WPT system.



(a) (b)

Fig. 18. Experimental switching waveforms of the CRM PFC at full-load operation of the 100 W 6.78 MHz WPT system. (a) When V_{in} = 130 V. (b) When V_{in} = 170 V.

To validate the capability of fast dynamic response, a load transient is conducted by removing one of the receivers. Fig. 19 and Fig. 20 display the tested waveforms of the CRM PFC during the transition between full load and half load, and Fig. 21 shows the transmitter coil current during the load transient. As can be seen, fast transient response is achieved with very small DC bus voltage fluctuation, and the 6.78 MHz transmitter coil current is not influenced during the process.

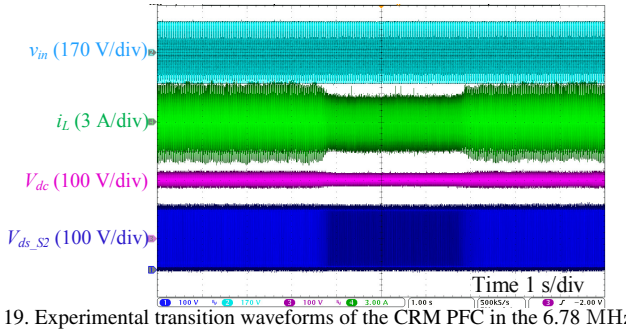
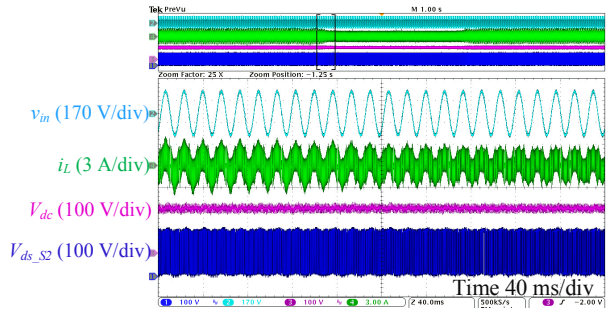
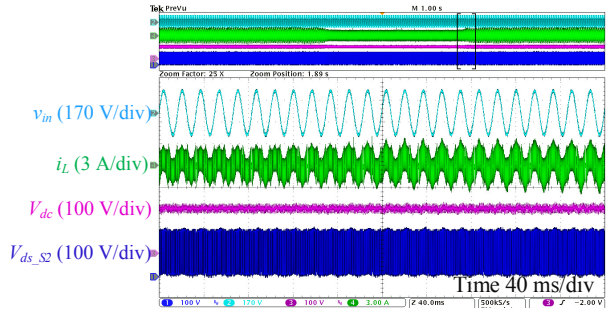


Fig. 19. Experimental transition waveforms of the CRM PFC in the 6.78 MHz WPT system during load variation between full load and half load.

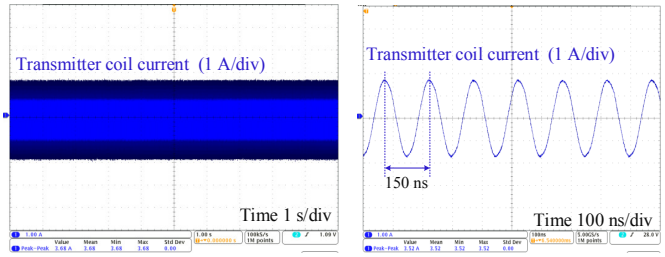


(a)



(b)

Fig. 20. Experimental transition waveforms of the CRM PFC in the 6.78 MHz WPT system. (a) From full load to half load. (b) From half load to full load.



(a) (b)

Fig. 21. Experimental transmitter coil current during load variation between full load and half load (a) Long-scale waveform. (b) Zoom-in waveform.

VI. Conclusions

A GaN-based CRM totem-pole PFC converter with ZVS control is developed for a 100 W 6.78 MHz wireless charging power supply system with multiple receivers. To meet the requirement of fast dynamic response, digital-based voltage-loop controller with high bandwidth and notch filters are employed. In order to avoid the noise impact and maintain stable ZVS control in the high-frequency environment, fully isolated sensing circuits with EMI filters are implemented, and balanced CM impedance are achieved by coupled IMN inductor. The proposed methods for fast transient response and noise immunity have the advantages of easy implementation, and do not require additional components and control. A prototype of a 100 W GaN-based 6.78 MHz WPT system is developed, and demonstrated with 90.16% end-to-end full-load efficiency. PFC operates reliably with ZVS control, and fast dynamic response is validated during load changing.

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