Development of a Converter-Based Data Center Power Emulator

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***Abstract*—Data centers have become a widespread power electronics (PE) load, with significant impact on the power grid. In order to investigate data centers' load characteristic and help evaluate the grid dynamic performance, this work develops a data center power emulator based on a reconfigurable PE converter-based hardware testbed (HTB). A complete dynamic power model is proposed which can precisely predict the data center dynamic performance. Based on the model, the data center power emulator is implemented in two voltage source inverters (VSIs) as an all-in-one load in the HTB. The proposed emulator has been verified experimentally in a regional network. Dynamic performances during voltage sag events are emulated and discussed. The emulator provides an effective, easy-to-use tool to better design the data center and study the power system.**

***Index Terms*—data center, power distribution, dynamic model, power emulator, hardware testbed, voltage sag**

I. Introduction

Data centers are indispensable for today's computing and networking society, and they have been constructed around the world. The global electricity demand by data centers has increased to 205 TWh in 2018, accounting for almost 1% of the global electricity supply [1]. Data center is also a complicated system with a high density of power electronics (PE) [2].

As a large electric load with high penetration and nonlinear performance, data center's influence on the power grid is significant. On one hand, data center exhibits dynamic server load, which results in apparent power demand fluctuations in a short time [3]. On the other hand, grid disturbances/contingencies would result in operation mode transition within the data center, leading to dynamic response on the power grid [4]. Therefore, it is important to investigate the data center load characteristics and help evaluate the grid dynamic performance and transient stability. Correspondingly, an accurate data center power model is required, and the resulting power simulator and/or emulator need to be developed.

Existing data center power models can be divided into four categories. The first type focuses on one or two aspects of the data center, such as model of server loads [5], which is incomplete to reflect the overall performance. The second kind is based on mathematical calculation, *e.g.,* a coherent data center model is proposed in [6] to capture the static operation. However, it cannot predict dynamic performances during transient conditions. The third group of models is driven by prerecorded data from a given data center [7], [8]. Such models are highly dependent on the provided data, which is usually not openly available. The last category builds models for dynamic simulation [9]. Nevertheless, the established models are oversimplified and inaccurate, *e.g.,* using simple resistive load to represent the server load. Therefore, there is a lack of data center power load model that is complete and accurate to reflect the dynamic performance.

Simulation and/or emulation platforms include digital simulation tools like PSCAD and Matlab Simulink [10], real-time digital emulators such as RTDS [11] and Opal-RT [12], and analog-based emulation platforms with down-scaled prototypes or hardware testbeds [13]. Compared with analog-based emulators, digital simulators/emulators are relatively cheaper, smaller, and easy to be installed. However, digital simulators/emulators suffer from instability and convergence issues, and ignore realistic conditions such as sensing errors, communication time delay, control bandwidth, and switching noise [14]. Although analog emulators are more expensive, bulkier, and less accessible, the testing results are more convincing and preferred for most engineers [15].

In [13], a unique hardware testbed (HTB) platform is developed in the NSF/DOE Engineering Research Center, CURENT, to overcome the issues with digital simulators and conventional analog emulators. The HTB is a multi-converter based reconfigurable real-time grid emulator, which is used to perform real power tests and emulate the power grid with broad time scales (μs to s), higher robustness, reduced computational resources, and capability of emulating precise transient response. By programming the interconnected three-phase voltage source inverters (VSIs), various power elements can be emulated, such as the generator, battery energy storage system (BESS), and power loads [16].

Based on the HTB platform, a converter-based real-time power emulator of a data center power distribution system is developed in this work. The paper is organized as follows: Section II identifies the data center system circuit and operation principle. Section III illustrates the proposed strategy for developing the data center power emulator. Section IV provides the simulation and experimental verification of the data center power emulator. Section V gives the conclusions.

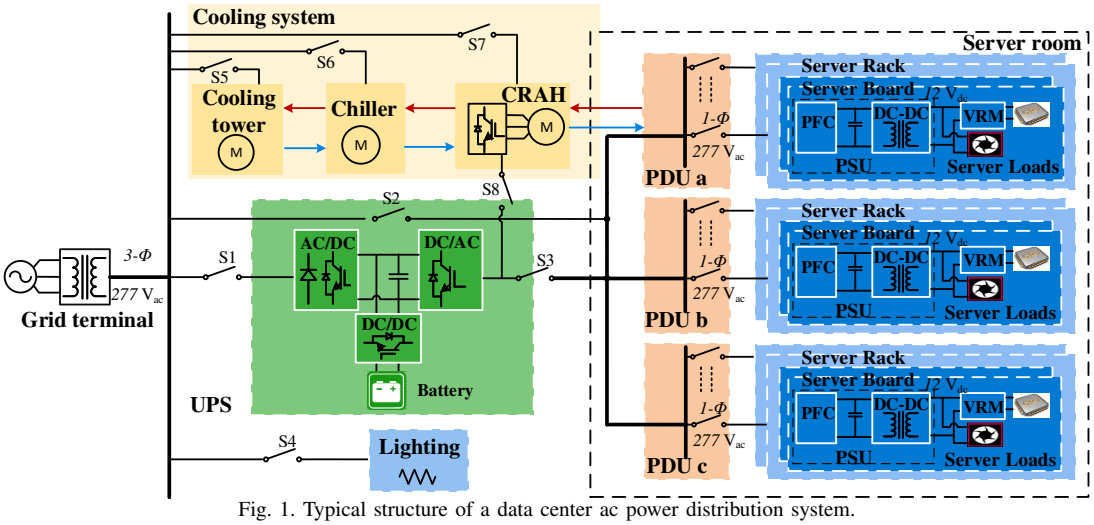


Fig. 1. Typical structure of a data center ac power distribution system.

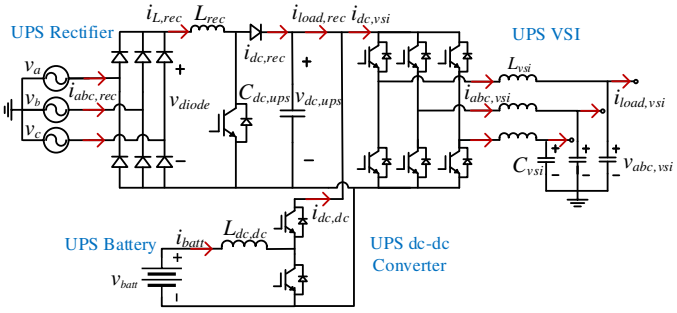
II. Data Center Circuit and Operation Principle

A. Circuit Topology and Control

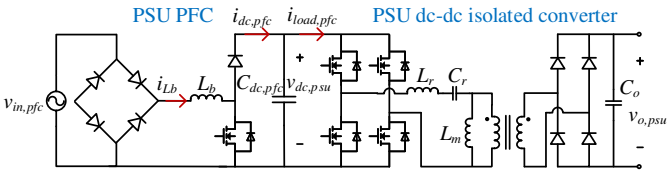
Fig. 1 shows the widely-used data center ac power distribution system [4]. The power supply system includes a centralized uninterrupted power supply (UPS), power distribution units (PDUs), rack-level power supply units (PSUs), server boards and loads. The air cooling system consists of a cooling tower, chiller, water pumps, computer room air handler (CRAH), and server room fans. Commonly-used circuit topologies and control strategies are investigated and summarized, as shown in Table I and Fig. 2.

TABLE I. Widely-used circuit topologies and control methods in data centers.

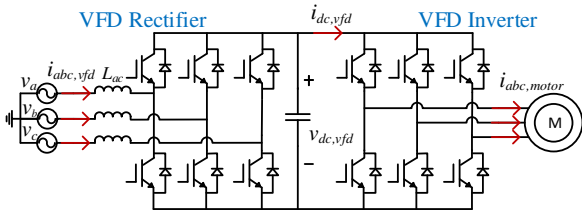
UPS front-end rectifier	
Topology	3-phase boost-type PFC rectifier [17]
Nominal voltages	3-phase 480/277 V_{ac} - 960 V_{dc}
Control method	Peak current mode control
UPS inverter	
Topology	3-phase voltage source inverter [18]
Nominal voltages	960 V_{dc} - 3-phase 480/277 V_{ac}
Control method	Dual-loop space vector control
UPS dc-dc stage	
Topology	Half-bridge dc-dc converter
Nominal voltages	600 V_{dc}-960 V_{dc}
Control method	Average current mode control [19]
UPS battery	
Battery type	Lithium-ion battery [20]
Nominal voltage	600 V_{dc} with 2 × 182 cells
PSU PFC converter	
Topology	1-phase boost PFC converter [21]
Nominal voltages	1-phase 277 V_{ac} - 480 V_{dc}
Control method	Average current mode control
PSU dc-dc isolated converter	
Topology	Full-bridge LLC converter
Nominal voltage	480 V_{dc} - 48 V_{dc}
Control method	Variable frequency control [22]
CRAH variable frequency drive (VFD) front-end rectifier	
Topology	3-phase active boost rectifier
Nominal voltages	3-phase 480/277 V_{ac} - 800 V_{dc}
Control method	Dual-loop space vector control
CRAH VFD inverter	
Topology	3-phase voltage source inverter
Control method	Constant V/Hz control [23]



(a) UPS circuit.



(b) PSU circuit.



(c) VFD-based motor circuit.

Fig. 2. Circuit topologies of the power converters in the data center system.

B. System Operation Principle

In order to maintain reliable server operation and improve the system power usage effectiveness (PUE), data centers are normally implemented with multi-mode operation [24]. In this work, three widely-used operation modes are employed.

- *Normal eco mode* : When the utility power is within the acceptable limits, the server loads are directly supported by the utility power through PDUs and PSUs. The UPS is bypassed and operated at light load (*i.e.,* 1% load).

TABLE II. Data center operation modes in different voltage levels.

No.	Operation mode	$V_{t,pu}$	$t_{transition}$	S_1	S_2	S_3	S_4	S_5	S_6	S_7	S_8
0	Normal eco mode	0.9 - 1.1	N/A	on	on	off	on	on	on	on	off
1	Double conversion mode	0.7 - 0.9	500 ms	on	off	on	on	on	on	on	off
2	Battery mode	≤ 0.7	20 ms	off	off	on	on	off	off	off	on

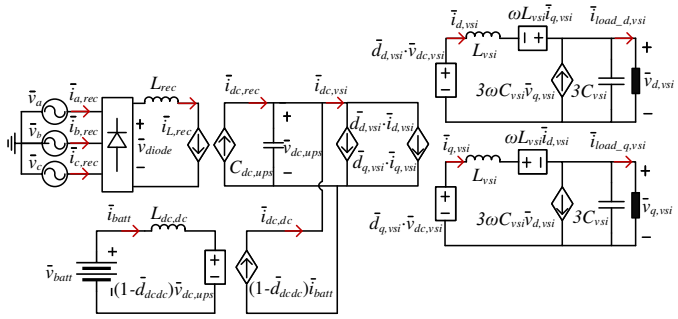


Fig. 3. UPS average model.

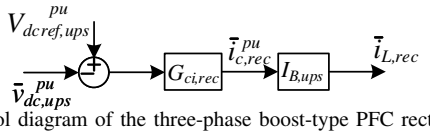


Fig. 4. Control diagram of the three-phase boost-type PFC rectifier in UPS.

- *Double conversion mode* : When the utility voltage is not within the allowed range but still within the UPS input range, the UPS switches online to regulate the power and supply the server loads.
- *Battery mode* : When power failure or severe grid interruption occurs, the UPS is disconnected from the grid and the backup battery provides the dc power to the inverter. Server loads are continually supplied by the UPS until utility power is restored.

During severe power disruption, the cooling system is disconnected from the grid, and the CRAH is carried by the UPS backup power to keep air circulation until the ac source is restored [25]. Also, the information technology (IT) equipment input power should be in the safe area as stipulated in the information technology industry council (ITIC) [26]. Considering the ITIC standard and commercial applications, an operation principle in response to voltage levels are identified, as presented in Table II.

III. Development of Data Center Power Emulator

A. Nonlinear Average Modeling

An average model that neglects switching ripple is built for the data center system identified in Section II.

1) UPS Model

The UPS contains a front-end boost power factor correction (PFC) rectifier, a VSI, a dc-dc converter, and a battery pack for energy storage. In continuous conduction mode (CCM) operation, the average model of the UPS is derived, as shown in Fig. 3. Peak current mode control is adopted in the UPS rectifier (Fig. 4), and dual-loop space vector control is employed in the UPS VSI (Fig. 5).

During the normal eco mode and double conversion mode, the UPS dc-link voltage $v_{dc,ups}$ is regulated by the rectifier,

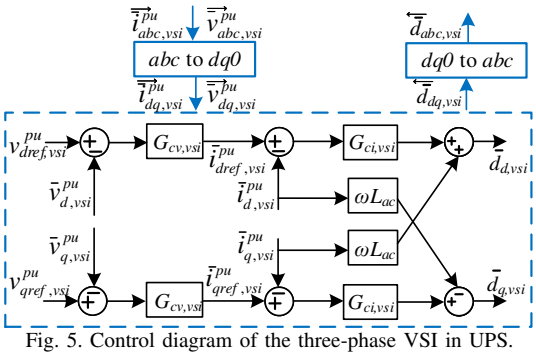


Fig. 5. Control diagram of the three-phase VSI in UPS.

and the dc-dc converter is responsible for charging or discharging the battery. As elaborated in Fig. 6, the inductor average current is regulated with a proportional integrator (PI) controller, and the current reference is determined by a charging/discharging algorithm (Algorithm 1). When the system operates in battery mode, the rectifier is turned off, and the dc-dc converter needs to control the battery discharging and regulate $v_{dc,ups}$ with an outer voltage loop, as shown in Fig. 7.

Algorithm 1: Battery charging and discharging

Input:
$P^{pu}_{ref,batt}$: battery active power reference in pu;
$\bar{v}^{pu}_{batt}$: battery pack terminal voltage in pu;
SOC : battery SOC;
Output:
$\bar{i}^{pu}_{batt\_ref}$: current reference for dc-dc converter in pu;
Procedure:
if $P^{pu}_{ref,batt} > 0$ **then**
  if $SOC > SOC_{min}$ **then**
    $\bar{i}^{pu}_{batt\_ref} = P^{pu}_{ref,batt} \div v^{pu}_{batt}$; *// battery is discharged*
  else
    $\bar{i}^{pu}_{batt\_ref} = 0$;
else if $P_{ref,batt} < 0$ **then**
  if $SOC < SOC_{max}$ **then**
    $\bar{i}^{pu}_{batt\_ref} = P^{pu}_{ref,batt} \div \bar{v}^{pu}_{batt}$; *// battery is charged*
  else
    $\bar{i}^{pu}_{batt\_ref} = 0$;
else
  $\bar{i}^{pu}_{batt\_ref} = 0$; *// battery stands by*

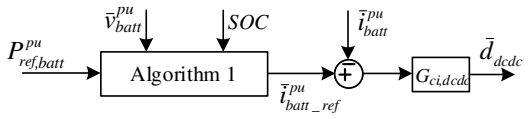


Fig. 6. Average current mode control of the dc-dc converter in UPS.

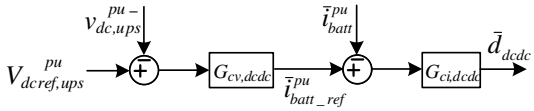
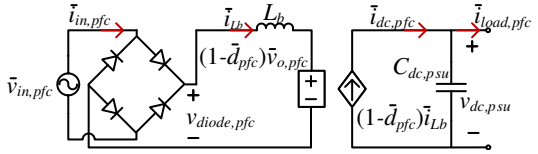
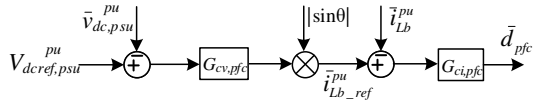


Fig. 7. Dual-loop control of the dc-dc converter during battery mode.



(a) PFC average model.



(b) PFC control diagram.

Fig. 8. Average model and control diagram of the PSU PFC converter.

The UPS battery pack is composed of two-paralleled battery strings of 182 Li-ion battery cells. The equivalent Li-ion battery circuit and mathematical equations used in [27] are adopted to model the battery's charging/discharging performance. With the current controlled by the dc-dc converter, the battery's state-of-charge (SOC) is calculated based on the coulomb counting (CC) method [28], as expressed in

$$SOC_{cell} = SOC_0 - \frac{\int_0^t \bar{i}_{cell} dt}{Q_{cell}} \tag{1}$$

2) PSU Model

The PSU front-end PFC rectifier is used to improve the power factor (PF) and regulate the dc bus voltage. In CCM operation with average current mode control, the average model of the PFC converter is presented in Fig. 8(a). Fig. 8(b) shows the control structure of the PFC converter. The outer voltage loop is designed with slow bandwidth (typically < 20 Hz) to avoid the influence of the double-line frequency ripple. The inner current loop compensates the average inductor current to achieve unity PF, and the control bandwidth is much faster.

LLC resonant converter is popular in the isolated dc-dc stage owing to the high-efficiency operation with wide input variation. Variable frequency control with voltage controlled oscillator (VCO) is normally used to regulate the output voltage [22]. Modeling of the LLC converter is nontrivial, since the traditional average model is not adaptable for high-frequency resonant circuit operating at 50 kHz $-$ 200 kHz. Compared with the PFC slow voltage loop (typically $<$ 20 Hz), the LLC converter has much faster control bandwidth usually at 1 kHz $-$ 5 kHz, which is fully decoupled from the PFC stage in the control perspective. In addition, in the low-frequency range within the control bandwidth, the LLC converter has a negative input impedance and behaves like a constant power load [29]. Therefore, in the model, the LLC converter is simplified as a controlled power load depending on the server load.

3) Cooling System Model

Motors are the predominant electrical components in the cooling system. In the model, an aggregated grid-connected induction motor is used to represent the cooling tower, chiller, and water pumps. The dynamic motor model illustrated in [23] is adopted to obtain the transient behaviors.

As shown in Fig. 2(c), the CRAH is modeled by a two-stage variable frequency drive (VFD) based motor. Average model in dq coordinates of the three-phase rectifier and VSI is adopted [18]. Traditional dual-loop space vector control is used in the rectifier, and constant volt-per-hertz (V/Hz) control is employed in the VSI to drive the induction motor [23].

4) Server and Thermal Load Model

Various linear and nonlinear power models have been developed to model the server load [30]. In this work, the server power consumption is estimated based on the linear model with server utilization rate, as

$$P_{server} = P_{idle} + (P_{rated} - P_{idle}) u_{server} \tag{2}$$

where P_{idle} is the power consumed in idle mode, P_{rated} is the server power rating, and u_{server} stands for the server utilization which varies from 0% to 100%. Assuming load balancing is realized, the total server load is predicted as

$$P_{tot,server} = N_{rack} N_{server} P_{server} \tag{3}$$

where N_{rack} and N_{server} represent the number of racks and the number of servers per rack, respectively.

Different models are developed to estimate the thermal load in data centers [31]. In this work, a bottom-up cooling power load model is built based on approaches used in [6], [32]. Server fans' power is first estimated based on the server load, and power consumption of the CRAH, chiller, water pumps, and cooling tower can be predicted based on the thermal load of the front stage. In this way, once u_{server} is given, the total cooling system load can be calculated.

B. Generalized Discrete Modeling

To be compatible with the HTB, the data center emulator is achieved by local VSIs, and all data center model and control functions are implemented in the VSI digital signal processor (DSP). Therefore, the nonlinear average model should be transformed into discrete-time version by digitization, and a generalized model with explicit input variables and output variables is required to coordinate all power stages under different operation cases.

1) Digitized Model in Discrete-Time Equation

The whole nonlinear average model is digitized with sampling period at $T_s = 0.2$ ms, and transformed into discrete-time equations. For closed-loop controls, the PI controllers are expressed in the form of

$$\begin{cases} e[x] = Y_{ref}^{pu}[x] - \bar{y}^{pu}[x-1] \\ \bar{s}_c^{pu}[x] = k_p e[x] + \sum_0^x k_i e[x] T_s \end{cases} \tag{4}$$

where $\bar{y}^{pu}$ is the controlled parameter, $e[x]$ is the error from the reference value $Y_{ref}^{pu}[x]$, k_p, k_i are PI parameters, and $\bar{s}_c^{pu}[x]$ is the control signal.

The UPS rectifier model in discrete-time equation is:

$$\begin{cases} \bar{i}_{L,rec}[x] = \bar{i}^{pu}_{c,rec}[x] I_{B,ups} \\ \bar{v}_{diode}[x] = \max\{\bar{v}_{ab,rec}[x], \bar{v}_{ac,rec}[x], \ldots, \bar{v}_{cb,rec}[x]\} \\ \bar{v}_{dc,rec}[x] = \dfrac{T_s}{C_{dc,ups}}\left(\dfrac{\bar{v}_{diode}[x]\bar{i}_{L,rec}[x]}{\bar{v}_{dc,rec}[x-1]} - \bar{i}_{load,rec}[x-1]\right) \\ \qquad\qquad + \bar{v}_{dc,rec}[x-1] \end{cases} \tag{5}$$

$$\begin{cases} if \;\; \bar{v}_{diode}[x] = \bar{v}_{ab,rec}[x] \\ \bar{i}_{a,rec}[x] = \bar{i}_{L,rec}[x],\ \bar{i}_{b,rec}[x] = -\bar{i}_{L,rec}[x],\ \bar{i}_{c,rec}[x] = 0; \\ if \;\; \bar{v}_{diode}[x] = \bar{v}_{ac,rec}[x] \\ \bar{i}_{a,rec}[x] = \bar{i}_{L,rec}[x],\ \bar{i}_{b,rec}[x] = 0,\ \bar{i}_{c,rec}[x] = -\bar{i}_{L,rec}[x]; \\ if \;\; \bar{v}_{diode}[x] = \bar{v}_{bc,rec}[x] \\ \bar{i}_{a,rec}[x] = 0,\ \bar{i}_{b,rec}[x] = \bar{i}_{L,rec}[x],\ \bar{i}_{c,rec}[x] = -\bar{i}_{L,rec}[x]; \\ if \;\; \bar{v}_{diode}[x] = \bar{v}_{ba,rec}[x] \\ \bar{i}_{a,rec}[x] = -\bar{i}_{L,rec}[x],\ \bar{i}_{b,rec}[x] = \bar{i}_{L,rec}[x],\ \bar{i}_{c,rec}[x] = 0; \\ if \;\; \bar{v}_{diode}[x] = \bar{v}_{ca,rec}[x] \\ \bar{i}_{a,rec}[x] = -\bar{i}_{L,rec}[x],\ \bar{i}_{b,rec}[x] = 0,\ \bar{i}_{c,rec}[x] = \bar{i}_{L,rec}[x]; \\ if \;\; \bar{v}_{diode}[x] = \bar{v}_{cb,rec}[x] \\ \bar{i}_{a,rec}[x] = 0,\ \bar{i}_{b,rec}[x] = -\bar{i}_{L,rec}[x],\ \bar{i}_{c,rec}[x] = \bar{i}_{L,rec}[x]; \end{cases} \tag{6}$$

where $\bar{i}^{pu}_{c,rec}[x]$ comes from the digitized controller.

The UPS VSI model in discrete-time equation is:

$$\begin{cases} \overrightarrow{\bar{i}_{dq,vsi}}[x] = \dfrac{T_s}{L_{vsi}}\bar{v}_{dc,vsi}[x-1]\overrightarrow{\bar{d}_{dq,vsi}}[x] - \dfrac{T_s}{L_{vsi}}\overrightarrow{\bar{v}_{dq,vsi}}[x-1] \\ \qquad + \begin{bmatrix} 1 & \omega T_s \\ -\omega T_s & 1 \end{bmatrix}\overrightarrow{\bar{i}_{dq,vsi}}[x-1] \\ \overrightarrow{\bar{v}_{dq,vsi}}[x] = \dfrac{T_s}{C_{vsi}}\overrightarrow{\bar{i}_{dq,vsi}}[x-1] - \dfrac{T_s}{C_{vsi}}\overrightarrow{\bar{i}_{load\_dq,vsi}}[x-1] \\ \qquad + \begin{bmatrix} 1 & \omega T_s \\ -\omega T_s & 1 \end{bmatrix}\overrightarrow{\bar{v}_{dq,vsi}}[x-1] \\ \bar{i}_{dc,vsi}[x] = \overrightarrow{\bar{d}_{dq,vsi}}^{T}[x]\overrightarrow{\bar{i}_{dq,vsi}}[x-1] \end{cases} \tag{7}$$

where $\overrightarrow{\bar{d}_{dq,vsi}}[x]$ comes from the digitized controller.

The UPS dc-dc converter model in discrete-time equation is:

$$\begin{cases} \bar{i}_{batt}[x] = -\dfrac{T_s}{L_{dc,dc}}(1 - d_{dcdc}[x])\bar{v}_{dc}[x-1] \\ \qquad + \dfrac{T_s}{L_{dc,dc}}\bar{v}_{batt}[x-1] + \bar{i}_{batt}[x-1] \\ \bar{i}_{dc,dc}[x] = (1 - d_{dcdc}[x])\bar{i}_{batt}[x] \end{cases} \tag{8}$$

where $d_{dcdc}[x]$ comes from the digitized controller. The discrete Li-Ion battery model used in [33] is adopted.

The combined UPS model in discrete-time equation is: during the normal mode and double conversion mode,

$$\bar{v}_{dc,ups}[x] = \frac{T_s}{C_{dc,ups}}(\bar{i}_{dc,rec}[x] + \bar{i}_{dc,dc}[x] - \bar{i}_{dc,vsi}[x]) \tag{9}$$

during the battery mode,

$$\bar{v}_{dc,ups}[x] = \frac{T_s}{C_{dc,ups}}(\bar{i}_{dc,dc}[x] - \bar{i}_{dc,vsi}[x]) \tag{10}$$

The single-phase PFC rectifier model in discrete-time equation is:

$$\begin{cases} \bar{v}_{diode,pfc}[x] = |\bar{v}_{in,pfc}[x]| \\ \bar{i}_{Lb}[x] = -\dfrac{T_s}{L_b}(1 - d_{pfc}[x])\bar{v}_{dc,psu}[x-1] \\ \qquad + \dfrac{T_s}{L_b}\bar{v}_{diode,pfc}[x] + \bar{i}_{Lb}[x-1] \\ \bar{v}_{dc,psu}[x] = \dfrac{T_s}{C_{dc,psu}}(1 - d_{pfc}[x])\bar{i}_{Lb}[x] \\ \qquad - \dfrac{T_s}{C_{dc,psu}}\bar{i}_{load,pfc}[x-1] + \bar{v}_{dc,psu}[x-1] \\ \bar{i}_{load,pfc} = \frac{N_{s,psu}P_{server}[x]}{\bar{v}_{dc,psu}[x]} \end{cases} \tag{11}$$

where $d_{pfc}[x]$ is determined by the digitized controller, and $N_{s,psu}$ is the number of servers supplied by one PSU.

The VFD rectifier model in discrete-time equations is:

$$\begin{cases} \overrightarrow{\bar{i}_{dq,vfd}}[x] = -\dfrac{T_s}{L_{vfd}}\bar{v}_{dc,vfd}[x-1]\overrightarrow{\bar{d}_{dq,vfd}}[x] \\ \qquad + \dfrac{T_s}{L_{vfd}}\overrightarrow{\bar{v}_{dq,vfd}}[x-1] + \begin{bmatrix} 1 & \omega T_s \\ -\omega T_s & 1 \end{bmatrix}\overrightarrow{\bar{i}_{dq,vfd}}[x-1] \\ \bar{v}_{dc,vfd}[x] = \dfrac{T_s}{C_{dc,vfd}}\overrightarrow{\bar{d}_{dq,vfd}}^{T}[x]\overrightarrow{\bar{i}_{dq,vfd}}[x-1] \\ \qquad - \dfrac{T_s}{C_{dc,vfd}}\bar{i}_{dc,vfd}[x-1] + \bar{v}_{dc,vfd}[x-1] \end{cases} \tag{12}$$

where $\overrightarrow{\bar{d}_{dq,vfd}}[x]$ comes from the digitized controller.

Based on the constant V/Hz control, the VSI output voltage $v_{dq\_vsi,vfd}$ is proportional to the reference rotation angular frequency $\omega_{m\_ref,vfd}$ that is determined by the required air flow rate.

$$\begin{cases} v_{d\_vsi,vfd}[x] = 0 \\ v_{q\_vsi,vfd}[x] = \omega_{m\_ref,vfd}[x]\frac{PV_b}{2\omega_b} \end{cases} \tag{13}$$

For the induction motors, the discrete model developed in [34] is employed.

2) Generalized Model

A generalized model with a top-level control is proposed for the data center power emulator, as illustrated in Fig. 9. The model starts with the terminal voltage v_t and grid frequency f, and the top-level control determines the operation mode according to the level of v_t. v_t and operation mode are then passed down to the following power stages. For each stage model, the input variable is the output voltage from the former stage, and the output variable is the calculated input current, which will be passed up to the former stage. In different operation modes, voltage and currents are calculated following the specific paths which are distinguished in different colors. Finally, the top-level control updates the grid terminal current i_t, and starts the next cycle of calculation. In the hardware implementation, one sampling period T_s on the DSP corresponds to one cycle through the model.

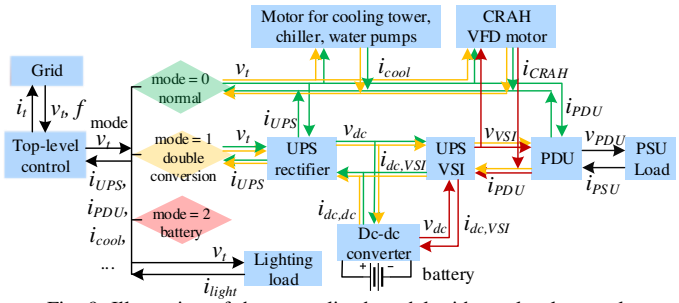


Fig. 9. Illustration of the generalized model with top-level control.

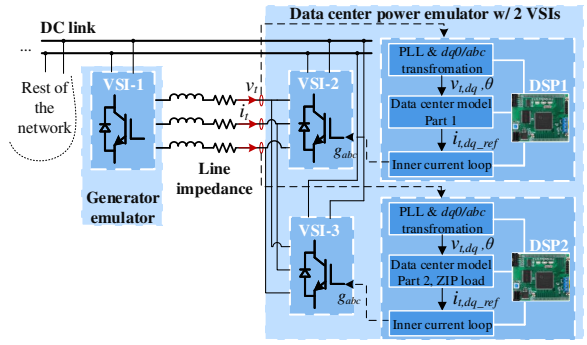


Fig. 10. Physical structure of the data center emulator on the HTB.

C. Hardware Implementation

The emulator is implemented on the HTB, where power components can be flexibly emulated by programming the interconnected three-phase VSIs [13]. A local network consisting of three VSIs in one cabinet is used for the data center emulator verification, as illustrated in Fig. 10. VSI-1 is implemented as a generator emulator to represent the grid power source that is connected to the emulator through a line impedance. The data center is emulated by two VSIs, where VSI-2 is embedded with models of UPS, PDUs, PSUs, and CRAH, and VSI-3 is installed with the aggregated induction motor model for cooling tower, chiller, and water pumps. In each of the load VSIs, the conditioning function, the data center model, and the VSI inner current loop are embedded in one DSP. The conditioned terminal voltage $v_{t,dq}$ is sent to the load model to generate the reference current i_{t,dq_ref}, which is used to produce PWM signals and control the VSI. Table III shows the specifications of the VSIs under test.

TABLE III. Specifications of the VSIs under test.

Parameters	Values
Dc link voltage	200 V
Switching frequency	10 kHz
Power rating	2 kW
Line impedance	1.8 mH
Base power under test	500 W

IV. Simulation and Experimental Emulation

A. System Definition and Scaling

A scaled data center ac power distribution system is defined according to the circuits, controls, and operation principle identified in Section II. Table IV presents the system configuration and parameters, and Table V shows the detailed design of power components. To verify the proposed data center model and emulator, simulation model of the defined data center system is built in Matlab Simulink, and the data center power emulator is implemented in the HTB with the regional network illustrated in Fig. 10.

TABLE IV. Defined data center configuration.

Parameters	Values
Intel Xeon 5500 processor	$P_{idle} = 10$ W
	$P_{rated} = 130$ W
Number of servers per rack, N_{server}	20
Number of racks, N_{rack}	3
Server room $\triangle T_{air,server}$	13.5 °C
Server fan E97379-001	$P_{rated,fan} = 13.8$ W
nominal fan air flow rate	$f_{0fan} = 0.0304$ m^3/s
CRAH rated power	$P_{rated,CRAH} = 2$ hp
CRAH fan nominal speed	$\omega_{0rm,CRAH} = 188.5$ rad/s
Chiller rated power	$P_{rated,chiller} = 2$ hp
Pump rated power	$P_{rated,pump} = 2$ hp
Cooling tower rated power	$P_{rated,CRAH} = 2$ hp
Chiller water $T_{wcold,chiller}$	16 °C
Cooling tower water $T_{wcold,CT}$	29.44 °C
Water flow rate	$f_w = 8.2 \times 10^{-4}$ m^3/s
System power rating	$P_{rated} = 15.068$ kW

TABLE V. Design parameters of power components.

UPS	
Power rating	10 kW
Dc-link capacitor	$C_{dc,ups} = 1$ mF
Rectifier boost inductor	$L_{rec} = 10$ mH
VSI inductor	$L_{vsi} = 2.3$ mH
VSI output capacitor	$C_{vsi} = 1$ nF
Dc-dc Converter inductor	$L_{dc,dc} = 300$ µH
Rectifier PI controller	$k_{p\_v,rec} = 4.07, k_{i\_v,rec} = 84.9$
VSI voltage PI controller	$k_{p\_v,vsi} = 1.16, k_{i\_v,vsi} = 219.9$
VSI current PI controller	$k_{p\_i,vsi} = 0.217, k_{i\_i,vsi} = 21.73$
Dc-dc voltage PI controller	$k_{p\_v,dcdc} = 114, k_{i\_v,dcdc} = 9499.6$
Dc-dc current PI controller	$k_{p\_i,dcdc} = 0.01, k_{i\_i,dcdc} = 5.06$
PFC	
Power rating	1.5 kW
Boost inductor	$L_b = 476$ µH
Dc output capacitor	$C_{dc,psu} = 1100$ µF
Voltage PI controller	$k_{p\_v,pfc} = 2.44, k_{i\_v,dcdc} = 33$
Current PI controller	$k_{p\_i,pfc} = 0.5, k_{i\_i,dcdc} = 13222$
CRAH VFD	
Power rating	1.5 kW
Dc-link capacitor	$C_{dc,vfd} = 837$ µF
Ac-side inductor	$L_{vfd} = 7.4$ mH
Voltage PI controller	$k_{p\_v,vfd} = 210.76, k_{i\_v,vfd} = 27021$
Current PI controller	$k_{p\_i,vfd} = 0.12, k_{i\_i,vfd} = 44.78$
Induction motor	
Power rating	2 hp
Mutual inductance	$L_m = 0.9446$ H
Leakage inductance	$L_{ls} = L_{lr} = 21.77$ mH
Stator resistance	$R_s = 2.368\ \Omega$
Rotor resistance	$R_r' = 6.21\ \Omega$
Inertia	1 s

B. Dynamic Performance during Voltage Sag Events

Voltage sag is one of the most common grid disturbances, which are demonstrated to show the dynamic response of the data center load. Fig. 11-Fig. 13 present the simulation and experimental results during different voltage sag events. Waveforms in p.u. values including the terminal voltage magnitude $V_{t,pu}$, terminal active power and reactive power $P_{t,pu}$, $Q_{t,pu}$, PSU ac input voltage $V_{ac\_PSU,pu}$, and PSU dc bus voltage $V_{dc\_PSU,pu}$ are displayed and compared.

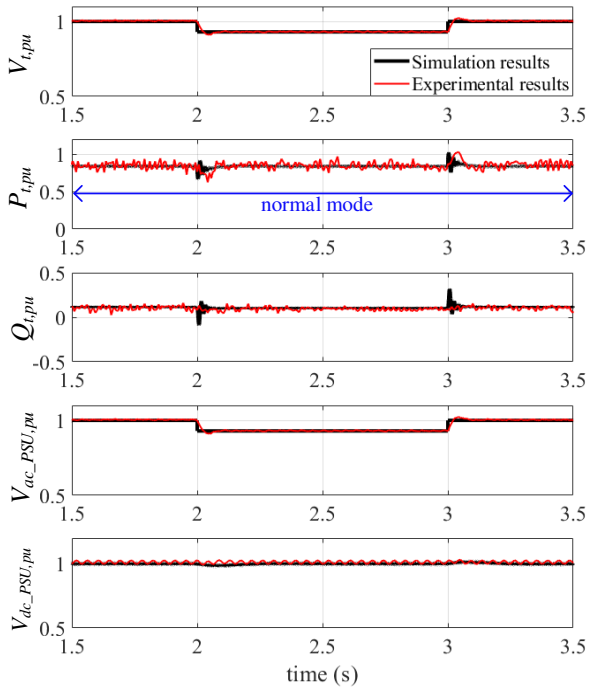


Fig. 11. Experimental emulation and simulation results of the data center power system with 7% terminal voltage sag for 1 s.

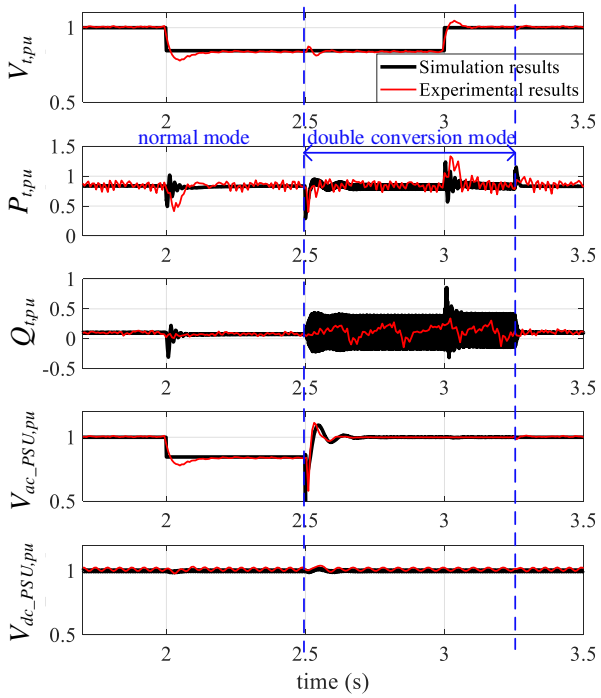


Fig. 12. Experimental emulation and simulation results of the data center power system with 26% terminal voltage sag for 1 s.

Fig. 11 shows the case when the terminal voltage has a 7% voltage drop. Since the terminal voltage does not exceed the allowable input range, the data center system works in normal mode all the time. However, dynamic response occurs when $V_{t,pu}$ changes, mainly due to the dynamic changes of the induction motor in the cooling system.

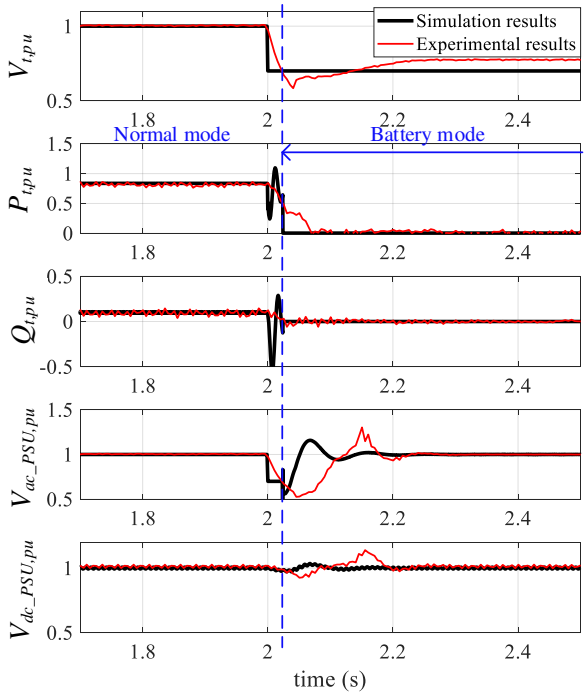


Fig. 13. Experimental emulation and simulation results of the data center power system with $>$ 30% terminal voltage sag.

When a 26% voltage sag occurs, as shown in Fig. 12, the data center changes from normal eco mode to double conversion mode after 500 ms at $t = 2.5$ s. At the same time, the UPS switches from very light load to carry the heavy server loads, leading to a transient response with an abrupt power variation and slight $V_{t,pu}$ fluctuation. At both the beginning and end of the voltage sag, the data center performs transient power change due to the sudden voltage variation. In comparison with the simulation results, the emulated voltage sag is more realistic where the grid voltage gradually drops or increases, instead of a sharp change in the simulation. Correspondingly, the power dynamic responses are different. Also, because of the limited data recording precision, $Q_{t,pu}$ high-frequency ripple during the double conversion mode is not reflected in the experimental result, but the low-frequency waveform is presented. In general, the experimental emulation is consistent with the simulated model, which verifies the accuracy of the power emulator.

Fig. 13 shows a more severe voltage sag with votlage drop $>$ 30%. To protect PSUs and maintain normal server operation, data center load is disconnected from the grid in 20 ms after the sag occurs, and the UPS battery switches in to continuously support the load. Consequently, $P_{t,pu}$ and $Q_{t,pu}$ drop to zero after the load shedding. Because the local network is not stiff enough, V_t oscillates some after the load shedding and is not as low as the initial value. Compared with the simulation, the gradually dropped terminal voltage in the emulation is more realistic because the voltage sag caused by the circuit fault or other contingencies is not instantaneous in practice. For all sag events, the PSU dc voltage is held at its nominal level to maintain the normal operation of server loads.

V. Conclusions

In this work, a data center power emulator is developed based on the HTB platform. A complete data center power model is proposed, and a generalized discrete model is derived to help implement the emulator, serving as an all-in-one load. Compared with the traditional hardware-based emulator, the proposed emulator is less expensive, more flexible and accessible, and capable of predicting the dynamic power performance. The power emulator has been verified in a regional power network in the HTB, and transient characteristics during voltage sag events are demonstrated. The data center power emulator can also be installed in different bus terminals of the HTB to perform various local or large-scale power system experiments. Therefore, the proposed data center power emulator provides an effective, accurate, and easy-to-use alternative to physical data center prototype for power system study.

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