Power Emulator of Variable Speed Drive with Grid Frequency Support in Multi-Converter Based Power Grid Emulation System

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Abstract—Variable speed drives (VSDs) have been gaining more popularity in recent years, since they not only improve the motor load performance, but also can provide grid frequency support after a grid disturbance. However, the existing open loop grid frequency control scheme restricts the power support performance provided by VSDs. In this paper, a closed loop primary frequency support scheme adopted by the VSD is proposed for grid frequency enhancement. Additionally, a real-time power emulator for a passive-front-end VSD using a three-phase voltage source converter (VSC) is developed, which is used for analog testing environment. The developed VSD load emulator demonstrates an accurate dynamic performance without sacrificing the computational resources and simulation time. The accuracy of the VSD load emulator has been verified by experimental results. Furthermore, the grid frequency support provided by VSD loads is performed in the multi-converter based hardware test-bed (HTB) by using the proposed VSD power emulator.

Index Terms—variable speed drive, diode rectifier, primary frequency support, hardware test-bed

I. Introduction

Induction motors are used in a wide range of industries, such as oil, mining, power, marine, and wastewater. Meanwhile, variable speed drives (VSD) have been widely applied to control induction motors because the power electronics (PE) based VSD can accurately regulate the motor rotating speed according to the requirement of the customers. So VSD has been gaining popularity in recent years considering its benefits on performance improvement and energy saving. Furthermore, the VSD has the potential to enhance the power grid stability since the VSD regulated motor loads can be designed to provide grid frequency support by flexibly adjusting the load power consumption. Specifically, non-critical loads, such as pumps and fans, are suitable to provide grid support since temporarily adjusting the rotating speed does not affect the corresponding primary production process [1]. However, in the existing literature discussing the VSD load frequency support, only the induction motor open loop control scheme is adopted by the VSD controller design, *e.g.,* the widely used constant volt-per-hertz control, which is also referred to as constant V/f control.

Applying the open loop constant V/f control to the VSD is cost-effective because: (1) an advanced microprocessor is not required to achieve the simple open loop control function; (2) less electrical sensors are needed since no feedback information is used in the control loop. However, the constant V/f control limits the accuracy of the VSD performance, so the VSD frequency support function is compromised. For example, as discussed in [2]–[4], an overshoot on the load power consumption is observed if the slew rate of the motor speed reference is large. Meanwhile, the critical parameters of the constant V/f controller can not be adjusted according to the load real-time performance, which is a general disadvantage of the open loop controller. Therefore, adopting a more advanced control scheme is a reasonable way to improve the VSD frequency regulation performance.

Electric loads can significantly influence the grid dynamic performance as stated above, so an accurate dynamic load model promotes the effectiveness of the power grid research. Conventional electromagnetic transient (EMT) models of PE-based devices can accurately reflect the corresponding dynamic performance [5], [6], but they are not suitable for the large-scale power network analysis considering the computational capability. As a result, the PE-based devices are represented by the static model in digital simulation tools in most cases. Meanwhile, although the dynamic load representation in the transient stability simulators has been investigated by the NERC Load Modeling Task Force [7], the dynamic
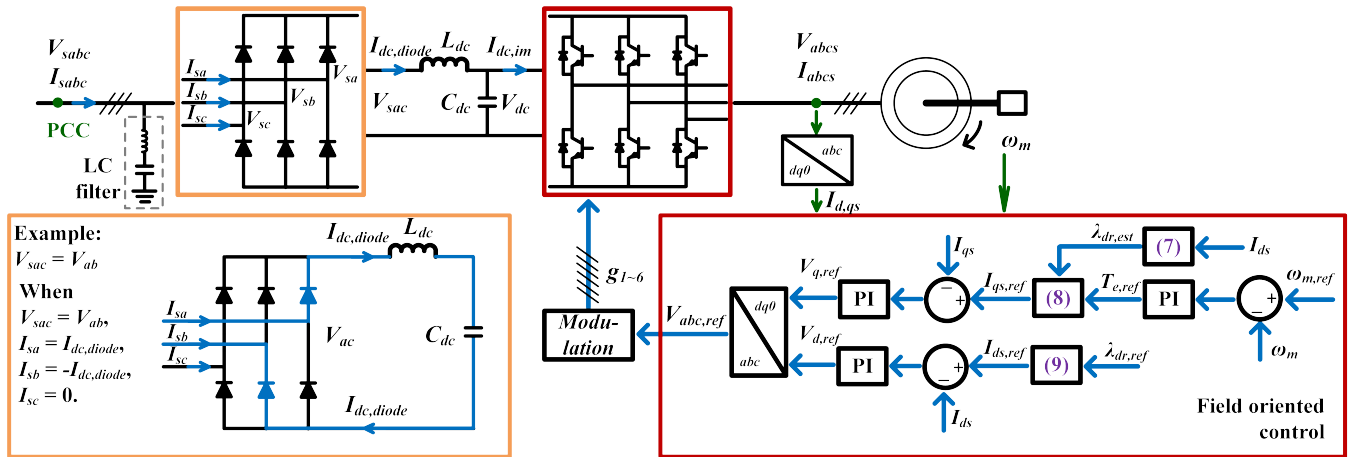
Fig. 1. VSD system circuit topology and control algorithm.

performance of PE-based loads has not been emphasized yet.

Considering that complicated electrical models are computationally prohibited by digital simulation tools, analog experimental platforms can be selected for power network transient studies due to their excellent performance on the accuracy, numerical robustness, and the wide time scale compared with digital simulations. In [8], [9], a multi-converter based hardware test-bed (HTB) has been proposed as a real hardware environment which is utilized to perform studies of the transmission level grid with real power flow, communication, and monitoring implementation. In the HTB, modular three-phase voltage source converters (VSCs) are used to emulate the electrical components in the power network, including the synchronous generator [10], transmission lines [11], static and dynamic loads [12], [13], etc. Multiple power grid scenarios can be performed and analyzed with specifically designed emulators, *e.g.,* the transmission network fault scenarios [14], the prolonged grid voltage depression due to air conditioner motor stall [15], etc.

However, the lack of VSD load emulator, which is designed to mimic the practical dynamic performance of VSD loads, limits the study of the corresponding frequency support performance in the power network. In the previous research in terms of the HTB power emulator development, load emulators related to the induction motor and the diode-front-end rectifier have been proposed. In [12], [15], load emulators specifying the characteristics of induction motor load and the motor-drive-regulated air conditioner have been developed. Also, the power emulator characterizing the three-phase diode rectifier connected with a resistor load is introduced in [16]. But there is still a gap between the VSD performance representation and the emulator models mentioned above: (1) the characterization of inverter-based motor drive has not been investigated yet; (2) the VSD load components are not effectively connected, including the front-end rectifier, the back-end inverter, and the motor load. So it is of critical importance to develop the VSD power emulator which is able to reflect the dynamic performance of the VSD regulated motor load, as well as the

corresponding impact on the power grid.

Therefore, the three-phase VSC based power emulator of a VSD regulated load is proposed in this paper, which characterizes the dynamic performance of a passive-front-end VSD connected induction motor driving a pump/ fan type of load. Furthermore, the closed loop primary frequency support scheme adopted by the VSD is proposed for grid frequency enhancement. The structure of the paper is organized as follows: Section II introduces the topology and modeling procedure of the VSD based motor load studied in this paper. The proposed frequency regulation scheme is also introduced. Section III presents the power emulator physical structure, and the dynamic performance of the proposed emulator demonstrates a good agreement with that of the equivalent load model created in PSCAD/EMTDC. The effectiveness of the frequency support provided by the VSD based motor load is verified by experimental results in the HTB using the proposed power emulator.

II. MODELING ALGORITHM OF PASSIVE-FRONT-END VSD POWER EMULATOR

A. VSD System Circuit Topology

In this paper, the passive-front-end VSD model adopted by the HTB load emulator is illustrated in Fig. 1. The VSD system includes a three-phase induction motor and a variable frequency power supply, which consists of a three-phase diode-front-end rectifier and a fully controlled three-phase full-bridge inverter back-end. The full-bridge diode rectifier electric circuit topology is illustrated in the upper side yellow box in Fig. 1. The diode rectifier is directly connected to the point of common coupling (PCC), of which the current and voltage are denoted by V_{sabc} and I_{sabc}.

B. Representation of Diode Rectifier

In the VSD system, the diode rectifier converts the three-phase ac power supply to provide a stable dc voltage V_{dc} for the next power stage, along with the dc filter inductor L_{dc} and energy storage capacitor C_{dc}. Compared with the diode bridge

model which has been derived in [17], the whole VSD load model in this text is derived based on the load bus terminal voltage V_{sabc}, ignoring the impact of the transmission line impedance. So the previous model algorithm, which relies on the dynamic of line impedance, is not suitable anymore. So a new diode bridge model algorithm for the HTB emulator is proposed as follows:

- The diode rectifier model is simplified based on the assumption that the diode switch in the rectifier is ideally disconnected from the circuit when turned off, and ideally connected when turned on with a forward voltage drop V_{diode}.
- As illustrated in Fig. 1, the voltage after the diode bridge, which is represented by V_{sac}, specifies the maximum line-to-line voltage of V_{sabc}. So $i_{dc,diode}$, which represents the current flowing from the diode bridge into C_{dc}, can be expressed as:

$$\frac{di_{dc,diode}}{dt} = \frac{V_{sac} - 2 \cdot V_{diode} - V_{dc}}{L_{dc}} \quad (1)$$

Meanwhile, the V_{dc} across the C_{dc} can be expressed as:

$$C_{dc}\frac{V_{dc}}{dt} = i_{dc,diode} - i_{dc,im} \quad (2)$$

where $i_{dc,im}$ represents the dc current flowing directly to the inverter and bypassing the C_{dc}.

- The diode bridge is under normal operating condition when $i_{dc,diode} > 0$. However, the diode bridge is disconnected from the rest of the power network when $i_{dc,diode}$ drops to 0 since it does not allow for the regenerative power (reverse power flow). I_{sabc} is determined by $i_{dc,diode}$ under normal operation as expressed in (3):

$$I_{sk} = i_{sgnk} \cdot i_{dc,diode}, \quad (k = a, b, c) \quad (3)$$

where i_{sgnk} represents the direction of I_{sabc} according to V_{sac}. When $i_{sgnk} = 1$, the corresponding phase k current is equal to $i_{dc,diode}$, while when $i_{sgnk} = -1$, the phase k current is opposite to $i_{dc,diode}$. The phase k has no current flowing through when $i_{sgnk} = 0$. According to the operating principle of diode front end rectifier, the diode switches which connect to the most positive and most negative source side ac voltage turn on to make up a complete current flow path. So the diode switch turn-on sequence is decided by the ac voltage source V_{sac}. An example explaining how I_{sabc} is related to V_{sac} and $I_{dc,diode}$ is illustrated in the lower side yellow box from Fig. 1, and more detailed information is listed in Table I.

TABLE I. Relation between i_{sgnk} and V_{max}.

V_{max}	V_{ab}	V_{ac}	V_{bc}	V_{ba}	V_{ca}	V_{cb}
i_{sgna}	1	1	0	-1	-1	0
i_{sgnb}	-1	0	1	1	0	-1
i_{sgnc}	0	-1	-1	0	1	1

- The LC passive filter is connected in parallel to the diode front end rectifier at the ac bus terminal to reduce the load current total harmonic distortion (THD). Aside from improving the power quality, the filter capacitor is also designed to provide a considerable amount of reactive power to adjust the local power factor. The reactive power support of the LC passive filter usually accounts for a larger portion compared with the impact of the load current THD reduction, so the reactive power provision is used to characterize the LC filter function in the HTB load emulator design:

$$Q_{flt} = \sum V_{s,rms}^2 / Z_{flt,k} \quad (4)$$

where Q_{flt} represents the reactive power provided by the passive filter, $V_{s,rms}$ represents the RMS value of the voltage source, $Z_{flt,k}$ represents the impedance of the LC filter.

Q_{flt} characterizes the total reactive power support by the passive filters connected to the VSD front end according to (4). In this paper, the impact of the VSD reactive power consumption is not emphasized since the grid frequency support function mainly involves the dynamic adjustment of the active power consumption. Therefore, Q_{flt} is regarded as a static value when considering the overall impact of the VSD load in the following sections.

C. Modeling of Back-end Inverter

The back-end rectifier is designed to provide voltage support to the motor load, which is denoted as V_{abcs} in Fig. 1. Compared with the VSD open loop control algorithm, the sophisticated closed loop control algorithms provide more accurate regulation of the motor load dynamic performance. Practically, the field-oriented control (FOC), the direct torque control (DTC), and the constant slip current control are commonly adopted by the induction motor drive. The common characteristics of these closed loop controllers is the motor drive is regulated to perform as a torque transducer of which the electromagnetic torque T_e is instantaneously equal to the T_e command approximately, which is denoted as $T_{e,ref}$. In this paper, the rotor-flux-oriented FOC is selected to regulate the induction motor, as illustrated in the lower side red box from Fig. 1.

For a given magnitude of flux linkage, T_e is maximized when the flux linkage and current vectors are perpendicular to each other. The objective of the FOC is to maintain such characteristics during the transient condition. Therefore, the following two operating conditions are required to be satisfied:

$$\lambda_{qr} = 0 \quad (5)$$

$$I_{dr} = 0 \quad (6)$$

where λ_{qr} represents the q-axis rotor flux linkage, and I_{dr} represents the d-axis rotor current. The first condition can be satisfied by a suitable choice of reference frame, and the second condition is satisfied by forcing the d-axis stator current to be constant. The mathematical expression of the motor electrical relation is significantly simplified according to (5) and (6).

The main principle of FOC is achieving the $T_{e,ref}$ by regulating the induction motor stator current I_{abcs}, which is also referred to as I_{dqs} in dq coordinates. As illustrated in Fig. 1, the I_{ds} and I_{qs} are regulated by PI controller following reference $I_{qs,ref}$ and $I_{ds,ref}$ respectively. By observing the motor control scheme illustrated in Fig. 1, the $T_{e,ref}$ is determined by a negative feedback outer loop controller, which provides $T_{e,ref}$ by regulating the motor rotating speed ω_m using a PI controller. The mathematical expressions presented in Fig. 1 are respectively expressed in (7) to (9), reflecting the motor electrical relation following the FOC requirements in (5) and (6). The detailed derivation can be found in [18].

$$\lambda_{dr,est} = L_m \frac{I_{ds}}{1 + (L_{rr}/R_r)s} \tag{7}$$

$$I_{qs,ref} = \frac{2L_{rr}T_{e,ref}}{3pL_m\lambda_{dr,est}} \tag{8}$$

$$I_{ds,ref} = \frac{\lambda_{dr,ref}}{L_m} \tag{9}$$

where L_m represents the magnetizing inductance, L_{rr} represents the total rotor inductance, R_r represents the rotor resistance, and λ_{dr} represents the d-axis rotor flux linkage. It should be noticed that λ_{dr} is equivalent to the flux linkage reference $\lambda_{r,ref}$ according to (5).

The basic configuration of the back-end inverter is the three-phase full bridge IGBT inverter, which is illustrated inside of the upper red box in Fig. 1. The full bridge IGBT inverter model is based on the inverter average model ignoring the dynamics of the switching devices. So the dynamic performance of the back-end inverter is mainly modeled by the corresponding control scheme. Therefore, the FOC scheme introduced in (7) $\sim$ (9) and Fig. 1 plays a critical role in the modeling of the back-end inverter. Detailed information related to the power emulator modeling of the three-phase full bridge IGBT inverter is introduced in [19]–[21].

D. Modeling of Induction Motor and Connected Fan/ Pump Load

The induction motor power emulator model, which has been proposed in [12], is employed by the VSD load model discussed in this paper. The detailed information about how the induction motor is modeled is not shown here, considering the length of the paper. As stated in Section I, the fan/ pump type of load is suitable for providing grid frequency support since temporarily adjusting the ω_m will not impact the primary production process. Ignoring the induction motor friction loss, the load torque T_L of load/ pump can be expressed below in p.u. value:

$$T_{L,pu} = \omega_{m,pu}^2 \tag{10}$$

where $T_{L,pu}$ and $\omega_{m,pu}$ represents the T_L and ω_m in p.u. value respectively.

E. Modeling Procedure of VSD Connected Motor Load

As presented above, the VSD load model consists of three major parts: the diode-front-end rectifier, the back-end inverter,

and the motor load. Each part represents a distinct dynamic performance, so it is critical to connect them together effectively when developing the VSD emulator model.

These three major sections are coordinated according to the VSD power emulator modeling procedure illustrated in Fig. 2. The modeling process illustrated in the yellow solid box represents the nth computational cycle in the power emulator microprocessor. The VSD model first starts from the VSD inverter back-end with the electrical components modeled from the last computation cycle, including V_{dc}, motor current consumption I_{ds}, I_{qs}, and ω_m. Next, the inverter back-end model provides updated motor stator voltage, V_{ds} and V_{qs}, to the induction motor and the connected load model. The electric variables related to the motor dynamic operation are updated at this step, including I_{ds}, I_{qs} and ω_m. At last, the updated I_{ds} and I_{qs} is sent to the diode rectifier model where the load current consumption I_{sabc} at the ac side is determined based on the updated I_{dc} and terminal voltage V_{sabc}.
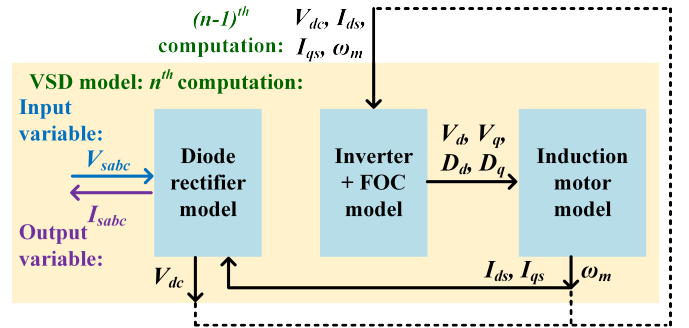

Fig. 2. VSD load emulator modeling procedure.

F. VSD Primary Frequency Control Scheme

According to Fig. 3, the grid frequency deviation Δf is measured and introduced to the motor speed reference $\omega_{m,ref}$. The $\omega_{m,ref}$ with respect to the Δf is expressed as:

$$\Delta f = f - f_{nom} \tag{11}$$

$$\omega_{m,ref} = K_f \cdot \Delta f + \omega_{m,ini} \tag{12}$$

where f represents the grid frequency, f_{nom} represents the nominal grid frequency, K_f represents the coefficient of frequency control scheme, and $\omega_{m,ini}$ represents the initial rotor speed before the grid disturbance.

The VSD load power regulation principle following the Δf is elaborated below: When the f decreases, the $\omega_{m,ref}$ will decrease proportional to Δf following (12). The coefficient K_f represents the extent of load response to the Δf. When the motor load starts to decelerate, the kinetic energy stored in the rotating mass will be released to provide a sudden active power injection to the grid, which is similar to the conventional inertial response provided by the generator and motor rotating mass. After the grid is stabilized, the ω_m is lower than the $\omega_{m,ref}$ due to the Δf and K_f, thus the VSD load power consumption is lower than that before the grid disturbance, *i.e.,* when $\omega_m = \omega_{m,ini}$. This will help mitigate the grid frequency

deviation from f_{nom} when subjected to a grid disturbance, which is similar to the effect of primary frequency control. The operating condition when f increases due to grid disturbance can be explained similarly.
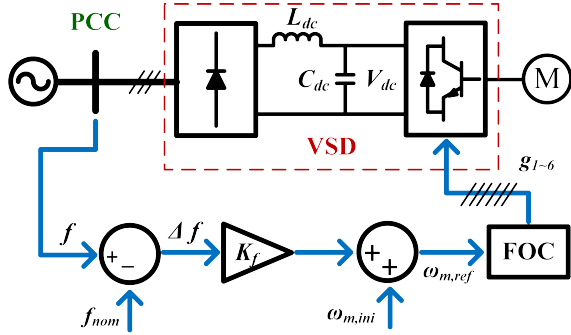

Fig. 3. VSD frequency support control diagram.

III. EXPERIMENTAL RESULTS

A. Power Emulator Physical Structure

As mentioned in Section I, the HTB is composed of multiple three-phase VSC based emulators, which can be flexibly programmed according to the specific function of the emulated electrical component. Fig. 4 specifies the electric connection and design principle of the power emulator.

The microprocessor applied in the power emulator is a TI DSP TMS320F28335. The VSD model is embedded in the DSP according to (1) $\sim$ (12) by the explicit Runge-Kutta 4th order method, which is used to solve the ordinary differential equation in the discrete fashion. The v_{sabc} represents the bus voltage at the terminal of the load emulator. The v_{sabc} is measured by the load emulator DSP, and then regarded as the terminal voltage of the VSD load, which is equivalent to V_{sabc} in Fig. 1 and Fig. 2.

As illustrated in Fig. 4, the DSP generates the current reference $I_{sdq,ref}$ according to the v_{sabc} following the modeling procedure illustrated in Fig. 2, then the VSC gate signals g_{abc} are generated based on $I_{dq,ref}$ through a current control loop and modulation process as illustrated in the solid grey box in Fig. 4. The $I_{sdq,ref}$ is the dq coordinate expression of I_{sabc}, which is illustrated in Fig. 1.

B. Experimental Verification of VSD Emulator

The EMT model of the VSD load following the configuration illustrated in Fig. 1 has been developed in PSCAD/EMTDC as the benchmark model to evaluate the accuracy of the proposed HTB power emulator model. The VSD load critical parameters are listed in Table. II. The accuracy of the emulator is evaluated by comparing the experimental results with the simulation results of the VSD benchmark model.

The VSD dynamic performance subject to $\omega_{m,ref}$ variation has been tested using the proposed VSD load emulator. A constant voltage supply is used to provide V_{sabc} for the load emulator. Fig. 5(a) shows the VSD dynamic performance when
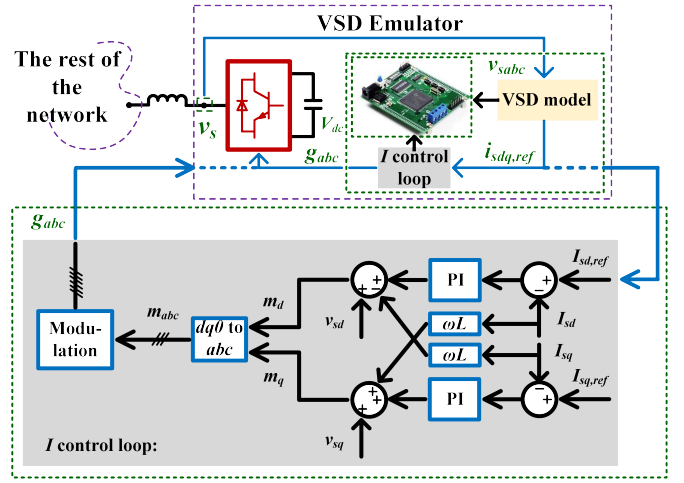

Fig. 4. VSD emulator physical configuration and control diagram.

TABLE II. VSD load model parameters.

Parameters	Value	Parameters	Value
front-end rectifier			
V_{diode}	0.8 V	L_{dc}	1.2 mH
C_{dc}	5 mF	$V_{s,base}$	574 V
back-end inverter			
K_{iT}	26	K_{pT}	13
K_{iI}	28.3018	K_{pI}	1.101
$\lambda_{r,ref}$	0.96 Wb	K_f	5
induction motor			
P_{rate}	37.3 kVA	V_{rate}	460 V
ω_{rate}	377 rad/s	H_{IM}	3 s
pole pair	1	R_s	0.0153 p.u.
R_r	0.0508 p.u.	L_{ls}	0.0532 p.u.
L_{lr}	0.0532 p.u.	L_m	2.306 p.u.

$\omega_{m,ref}$ increased from 0.7 p.u. to 0.8 p.u. during time = 1 s $\sim$ 6 s. The red curves represent the VSD emulation results in HTB, while the blue curves represent simulation results of the equivalent benchmark model.

Similarly, Fig. 5(b) shows the dynamic process of the $\omega_{m,ref}$ decreasing from 0.7 p.u. to 0.6 p.u. during time = 1 s $\sim$ 6 s. As illustrated in Fig. 5, ω_m, T_e and VSD power consumption are tested and recorded respectively. By observing the test results of the above two $\omega_{m,ref}$ variation process, it can be concluded that the dynamic performance of the VSD power emulator and that of the benchmark model shows a good agreement with each other, verifying that the VSD emulator model can accurately represent the dynamic performance of the realistic VSD load.

C. Grid Frequency Support provided by VSD

A simplified microgrid is built in the HTB testing platform serving as the test environment for the proposed VSD frequency regulation scheme. The microgrid topology is illustrated in Fig. 6 [22]. The VSDs are connected at Bus 2,
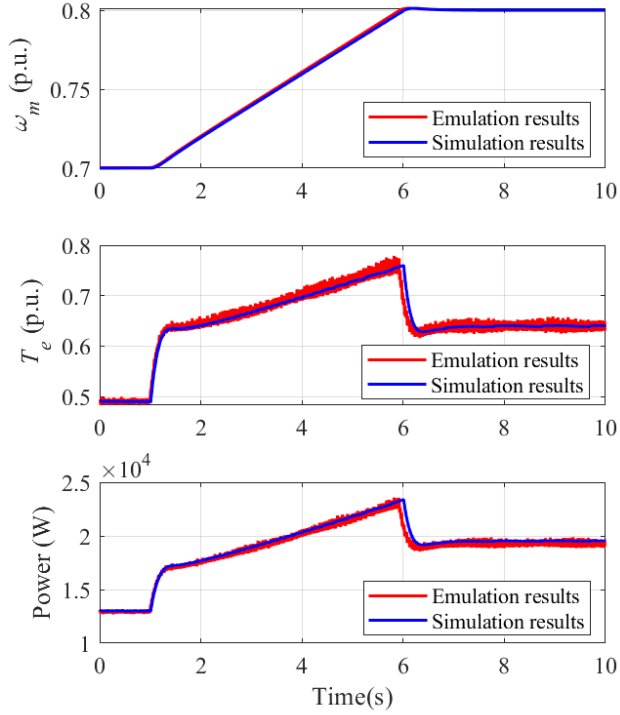
(a) VSD response to $\omega_{m,ref}$ increase.
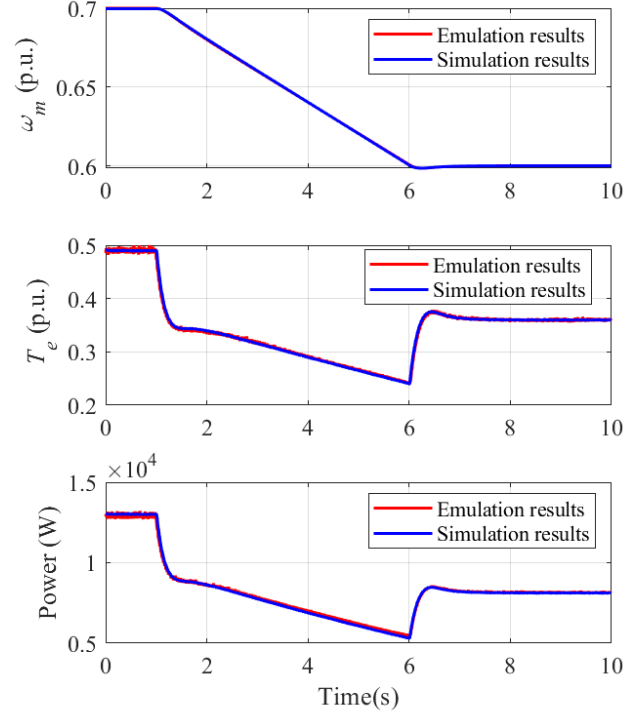
(b) VSD response to $\omega_{m,ref}$ decrease.

Fig. 5. Comparison of VSD dynamic performance between the benchmark model and developed power emulator.

Bus 5, and Bus 8, while the rest of the loads are constant PQ loads. The load connected to each Bus n is denoted as L_n. All VSD loads have the potential of providing grid frequency support following the control scheme illustrated in Fig. 3. The power supply of the microgrid is located at Bus 8, which is denoted as G_8. To simplify the microgrid model, the dynamic performance of G_8 is equivalent to a synchronous generator model with relatively small inertia constant. The generator secondary frequency regulation is ignored since only the primary frequency support function is emphasized in this paper. The power flow of generator and load at steady state are listed in Table III.
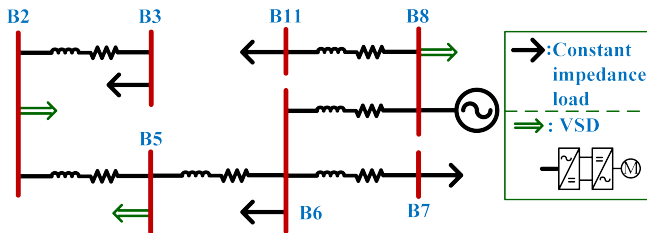

Fig. 6. Microgrid topology under testing.

The grid disturbance experimental results are illustrated in Fig. 7, where the power grid frequency deviation Δf is created by increasing or decreasing the active power consumption of the constant PQ load in the microgrid. In the load decrease

TABLE III. Microgrid static power flow profile.

Generator/ Load	Active power flow (p.u.)	Generator/ Load	Active power flow (p.u.)
G_8	1.25	L_6	0.2
L_2	0.15	L_7	0.2
L_3	0.2	L_8	0.15
L_5	0.15	L_{11}	0.2

event, the active power consumption of L_3 and L_6 decreased by 0.4 p.u. in total, while in the load increase event, the L_3 and L_6 increased by 0.4 p.u. in total. Three cases are emulated with the proposed VSD emulator for each frequency event: 1) Case 1 is represented by blue curves where no frequency support control is provided by VSDs in the microgrid. 2) Case 2 is represented by red curves. In this case, 50% of VSD loads at each Bus (Bus 2,5, and 8) follow the frequency support scheme as illustrated in Fig. 3, while the remaining 50% of the VSD loads do not provide frequency support. 3) Case 3 is represented by green curves where all VSD loads in the power network follow the frequency support scheme. As illustrated in 7(a) and Fig. 7(b), the grid disturbance that leads to the frequency deviation occurs at t = 1.7 s, and lasts until the end of the test. No secondary frequency control is provided since we only emphasized the impact of primary frequency control

in this paper. It can be concluded by observing simulation results that the frequency support provided by VSD loads presents a significant impact compared with the case where no support is involved:

- The Δf is mitigated with VSD loads providing frequency support. In three cases illustrated in Fig. 7, the amount of VSD loads adopting frequency support control scheme is 0%, 50%, and 100% respectively, which account for 0%, 18%, and 36% of the total load power consumption in the microgrid. With the increasing amount of responsive load, the Δf after grid stabilization decreases. This is because that the VSD loads can provide equivalent primary frequency support function by adopting the frequency support scheme. Therefore, the responsive VSD loads have the potential of enhancing the grid stability, which can help the grid less rely on the generation power reserve.

- The rate of change of frequency (RoCoF) and frequency nadir f_{nadir} decrease with increasing the penetration level of responsive VSD loads. The VSD load can rapidly respond to Δf due to being driven by PE interfaces, so a mitigation of power grid RoCoF is observed which is attributed to the fast absorption/ release of the VSD load active power. Therefore, the grid frequency stability is improved with mitigated RoCoF and f_{nadir}.
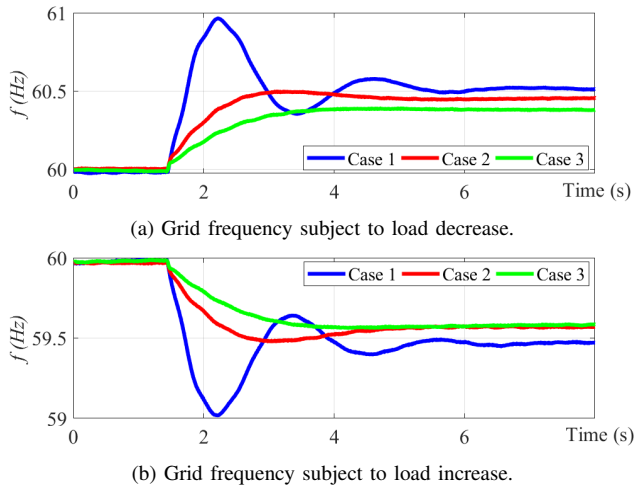

(a) Grid frequency subject to load decrease.

(b) Grid frequency subject to load increase.

Fig. 7. Grid frequency under different grid disturbance.

IV. Conclusion

In this paper, a three-phase VSC based power emulator characterizing the passive-front-end VSD is developed, which can accurately mimic the dynamic performance of the VSD load during different operating conditions without sacrificing the testing time length and computational resources. Additionally, the grid frequency support control by VSD is proposed in this paper, which provides active power by regulating ω_m according to the grid frequency deviation Δf. Experiments are performed on a simplified microgrid which is built in the HTB testing platform, with the proposed VSD power emulator

mimicking the corresponding frequency support function. The experimental results show that the VSD with frequency support control presents a positive impact on the grid frequency stabilization, including mitigating the RoCoF and f_{nadir}, as well as providing equivalent primary frequency support. Therefore, the effectiveness of the proposed frequency support scheme is verified.

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