Building Common-Mode Analytical Model for Dual Active Bridge Incorporating with Different Modulation Strategies

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***Abstract*—The modulation strategies of Dual-Active-Bridge (DAB) including single-phase-shift (SPS), dual-phase-shift (DPS) and triple-phase-shift (TPS) have been proposed to optimize the efficiency, eliminate the reactive power and release the current stress. While the previous literature focuses on the accurate loss model in steady states or small-signal analysis for dynamic response, the common-mode model has been largely ignored. The main contribution of this paper then is to propose an analytical common-mode model for DAB, which considers the common-mode (CM) parasitic capacitors including those of grounded heatsink and transformer windings. Based on such model, the common-mode performance is compared among different modulation strategies. The impact of two H-bridge on the input and output common-mode voltage has been addressed. A prototype based on SiC devices is used to verify the proposed analytical mode under SPS, DPS and TPS. It is found that while TPS improves the light-load efficiency it introduces the worst CM noise. Influence of the ZVS current setting on the CM performance is also discussed.**

***Index Terms* — Common-mode voltage, parasitic capacitance, Zero-Voltage-Switching, phase-shift control, wide-bandgap device, dual active bridges.**

NOMENCLATURE

DAB	Dual-Active-Bridge
WBG	Wide-band gap
TIM	Thermal interface material
SPS	Single-Phase-Shift
DPS	Dual-Phase-Shift
SDPS	Secondary-side-Dual-Phase-Shift
PDPS	Primary-side-Dual-Phase-shift
MPS	Multiple-Phase-Shift
ZVS	Zero-Voltage-Switching
P#	Primary side switches
S#	Secondary side switches
v_{AB}	Output voltage of primary-side H-bridge
v_{CD}	Output voltage of Secondary-side H-bridge
v_{AM}	Common-mode voltage at the first phase leg at primary side
v_{BM}	Common-mode voltage at the second phase leg at primary side
v_{CN}	Common-mode voltage at the first phase leg at secondary side
v_{DN}	Common-mode voltage at the second phase leg at secondary side
i_{Ls}	Primary-side leakage inductor current
L_s	Primary-side reflected leakage inductance
C_{ps}	Equivalent parasitic capacitance between primary and secondary sides of the transformer

I. INTRODUCTION

Dual active bridge (DAB) consists of two H-bridge connected through a high-frequency transformer [1], which has been widely used in many applications, such as photovoltaic inverter [2] and electric vehicle (EV) on-board charger (OBC) [3-5] thanks to its bidirectional power transfer capability and control flexibility. Most DAB researchers focus on the modulation strategy to extend the ZVS range [6-8], suppress the maximum switching current [9, 10] and eliminate the reactive power [11, 12]. One exemplary modulation strategy of DAB is the phase shift control, in which all switches are driven with 50% duty cycle. The power regulation is then realized by optimizing phase angles between different phase legs in DAB [13]. The traditional modulation strategy is SPS control [14], which only changes the phase shift between primary and secondary sides. SPS is easy to use and has high efficiency with ZVS particularly at heavy load, acceptable current stress and relatively low reactive power when the output-input voltage gain is close to one [1]. To get the better performance throughout the wide power and voltage range, DPS has been developed, particularly to maintain ZVS and restrict the switching current at the medium load [15, 16]. TPS, on the other hand usually is implemented at the light load or even no-load condition, which can also secure ZVS for all switches [17, 18]. Instead of fulfilling the ZVS requirement, EPS [19] and TZM [20] modulation focus more on eliminating the reactive power and releasing the current stress. Based on modulation strategies mentioned above, MPS is developed to integrate different modulation strategies benefiting the whole operation range [4, 18]. Hybrid modulation strategies utilizing the phase shift control and duty cycle control can also get the similar performance as the traditional phase shift control [21, 22], but it introduces too many control variables, which complicates the design and analysis.

While all modulation strategies mentioned above focus on the steady-state performance, to seek the influence of different modulation strategies on the dynamic response, the small signal model of DAB is also proposed in [23]. In [24], the delay effect caused by the digital control is proposed, which provides an accurate analytical model considering the control bandwidth.

However, one research element largely ignored in DAB research is the common-mode (CM) performance, which is extremely important in nearly all power electronics systems. For example, if using the DAB converter in EV OBCs, the system need comply with conducted EMI specifications listed in CISPR 25/EN 55022 [25]. For IT and multimedia equipment, CISPR 32/EN 55022 [26] provides the standard of the conducted EMI emission. With various EMI standards available, a CM analytical model of DAB is necessary to estimate the CM behavior with different modulation strategies.

The mechanism of common-mode voltage (CMV) generation is discussed in [27, 28], concluding that two H-bridges are the CMV sources. The transient processes caused by switching actions coupled with common-mode parasitic capacitors then excite the common-mode current (CMI) [29-31]. Such capacitance includes the winding capacitance of the high frequency transformer in regular isolated DC-DC converters [32] and the parasitic capacitance of the grounded heatsink [31], all providing the path for CMI. When building the analytical model of CMV in DAB converters, we should include all two H-bridges and all potential parasitic capacitors at the same time. More importantly, such analytical model should be able to quantify the CM performance under different modulation strategies. which, however, has not been addressed either.

Finding the CM research of DAB converter is rarely mentioned, this paper aims to build its CM analytical model particularly for the heatsink-grounded prototype. In Section II, the CM parasitic capacitors including those of switches caused by grounded heatsink and transformer windings are discussed. The detailed derivation of the analytical CMV model is provided in Section III. With such analytical model, the CM performance of different modulation strategies, i.e., SPS, DPS and TPS are fully studied in Section IV. Experiment results to verify the proposed CM model are shown in Section V, indicating that 1) SPS has the best CM performance while TPS has the worst, even though SPS will lose the ZVS at light load, and 2) larger ZVS current setting under the same control strategy tends to worsen the CM performance, though it secures ZVS more. Section VI is the conclusion.

II. Consideration of Parasitic Capacitance in DAB Common-mode Analysis

In the DAB converter, switching actions at H-bridge generate high frequency voltage pulses, which act as CMV sources. The parasitic capacitance then provides the CMI path. In this section, the parasitic capacitance at different positions will be discussed.

A. Active Switches

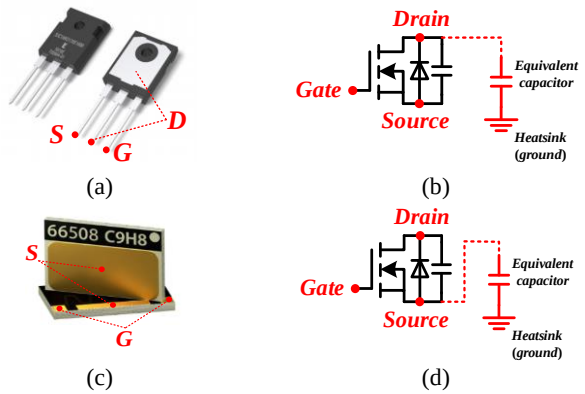


Fig. 1. Equivalent parasitic capacitor of different switches to heatsink: (a) TO-247 package switch; (b) the equivalent capacitor to ground in TO-247 package [33]; (c) GS66508T [34]; (d) the equivalent capacitor to ground of GS66508T.

For majority of discrete devices, thermal pads are not only for the heat dissipation but also connected to drain or source of switches. In a cooling system, thermal interface materials (TIMs) are inserted between the thermal pad and heatsink, which has high dielectric constant. The TIM should also be as thin as possible aiming at low thermal resistance, which then introduces the capacitance to between D/S to the heatsink. To dissipate the heat effectively and realize the high-power density, the heatsink can be connected to the converter case, which is usually grounded for the safety concern. In some designs the enclosure can be directly used as the heatsink, which makes the overall parasitic capacitance between the switch thermal pad and ground considerable. Two WBG devices are shown in Fig. 1. TO-247 is a commonly used package for SiC power MOSFETs, as shown in Fig. 1 (a). The thermal pads are connected to drain of the device, yielding an equivalent parasitic capacitor between drain and ground, as shown in Fig. 1 (b). In Fig. 1 (c), a top-cooled GaN device has the thermal pad connected to the source of the device, yielding the equivalent capacitor between the source and ground.

B. Transformer

In DAB, between two H-bridges lays a high frequency transformer for the galvanic isolation, power transfer and voltage gain, which, however, also provides the path for the CMI between the primary side and the secondary side. Assuming the parasitic capacitance is distributed evenly between the primary and the secondary windings, as shown in Fig. 2 (a) [35], we then can simplify the transformer model as Fig. 2 (b) [36, 37].

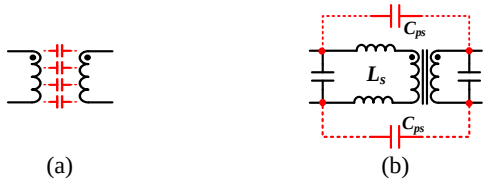


Fig. 2. Transformer considering parasitics in the CM analysis: (a) the distribution of the parasitic capacitance between primary side and secondary side of the transformer: (b) the transformer model with parasitics.

Here four equivalent capacitors are employed. The capacitance of primary-side winding or secondary-side winding is for the differential mode only. The capacitance between primary side and secondary side is CM capacitance. It acts as a "bridge" to couple the CM loops at both sides. In addition, if the parasitic capacitance between PCB polygon and ground is large enough, it can also provide the CMI path.

C. General CM Parasitic Capacitance in DAB

In CM discussion, the frequency domain analysis is mainly based on the spectrum from kilo-Hz to mega-Hz. In this frequency domain, the impedance of the DC-link capacitor is quite small, which can be regarded as short-circuit in CM loops. Hence in the DAB converter, there are six networks formed by active switches and transformer, which include primary-side DC-link, secondary-side DC-link and four mid-points of phase legs, as shown in Fig. 3. Also, the equivalent parasitic capacitance, $C_{i\#}$ and $C_{o\#}$, in the input source and load is considered to form CM loops in DAB. The CMV across $C_{i\#}$ and $C_{o\#}$ can represent the influence of the DAB converter on input source and load. When testing the prototype under certain EMI standards, the equivalent parasitic capacitance can be replaced by those inside LISNs, e.g., 50Ω and series capacitance. In this

paper, only equivalent parasitic capacitance is used to build the analytical CM model without considering the impact of LISNs.

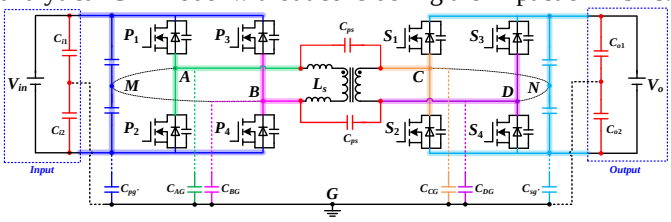


Fig. 3. General parasitic capacitance from topology to ground in DAB converter.

To analyze the CM performance in DAB converter, the topology shown in Fig. 3 can be further simplified as Fig.4. The differential-mode (DM) components are removed. The DC-link capacitors, transformer windings and DC sources are removed from the CM topology. Phase legs are replaced with the high frequency voltage sources caused by switching actions.

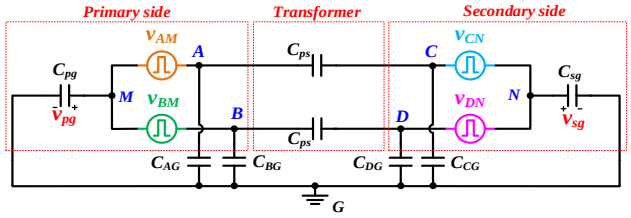


Fig. 4. General common-mode topology of the DAB converter.

Because $C_{pg'}$, C_{i1} and C_{i2} are all connected to the primary-side DC-link, in CM topology they are paralleled. Such scenario applies to the secondary-side DC-link. C_{pg} and C_{sg} in Fig. 4 are

$$\begin{cases} C_{pg} = C_{pg'} + C_{i1} + C_{i2} \\ C_{sg} = C_{sg'} + C_{o1} + C_{o2} \end{cases}. \tag{1}$$

v_{pg} across the primary-side DC-link and ground is CMV applied to the input source of DAB converter, which determines the CM performance. v_{sg} across the secondary-side DC-link and ground is CMV applied to the load. M and N points in Fig. 3 and Fig. 4 are the virtual middle points of DC-link and output capacitors, respectively. The CM topology shown in Fig. 4 can be used for general DAB CM analysis, which includes all potential parasitic capacitance from prototype to ground in different networks. For primary side, the parasitic capacitance from DC-link to ground is C_{pg}, and the parasitic capacitance from phase-leg mid-point to ground is C_{AG} and C_{BG}. For secondary side, the parasitic capacitance from output to ground is C_{sg}, and the parasitic capacitance from phase-leg mid-point to ground is C_{CG} and C_{DG}. The winding capacitance between primary side and secondary side is C_{ps}. The definitions of different symbols in Fig. 4 are present in TABLE I.

Table I General CM Parasitic Capacitance in DAB

Names of Capacitance	Symbol
Phase-leg Mid-point to Ground (Primary)	C_{AG}, C_{BG}
Phase-leg Mid-point to Ground (Secondary)	C_{CG}, C_{DG}
DC-link to Ground (Primary)	C_{pg}
DC-link to Ground (Secondary)	C_{sg}
Primary side to secondary side (Transformer)	C_{ps}

In Section II, general CM capacitors in DAB converter are introduced. The simplified CM topology is proposed to derive the analytical model of the DAB converter in next section.

III. Generalized Common-mode Voltage Model

According to the general CM topology in Fig. 4, the CM analytical model for DAB converter is derived in the following content. To quantify the voltage distributed across both input and output capacitors, Superposition Theorem is employed in Fig. 5. Four CMV sources act in the circuit separately, as shown in Fig. 5. The final voltage distributed across each capacitor is then the sum of the four individual circuits.

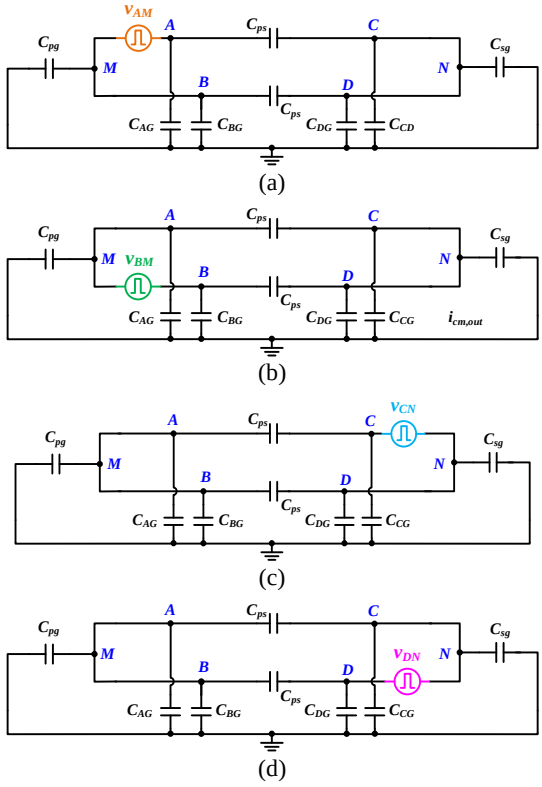


Fig. 5. Decomposed circuit with Superposition theorem: (a) CM loop with first phase leg at the primary side; (b) CM loop with second phase leg at the primary side; (c) CM loop with first phase leg at the secondary side; (d) CM loop with second phase leg at the secondary side.

For each circuit in Fig. 5, Thevenin's Theorem is used to abstract the equivalent voltage source and series impedance. For example, in Fig. 6 (a) to quantify the CMV across the input parasitic capacitors, the circuit is summarized as a two-port network between M and G. Then according to the Thevenin's theorem, the equivalent voltage source and series impedance are abstracted as Fig. 6 (b) and (c). Here C_1 in the figure is

$$C_1 = C_{sg} + C_{CG} + C_{DG} \tag{2}$$

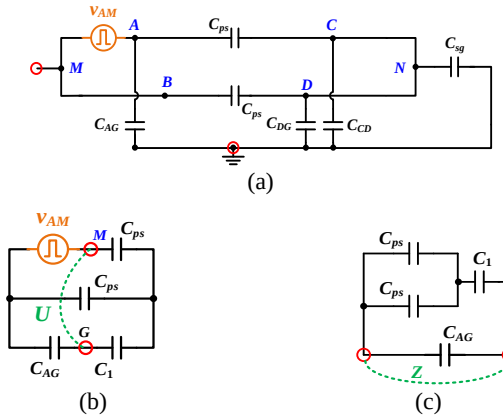


Fig. 6. Thevenin's theorem application: (a) Two-port network; (b) equivalent voltage source; (c) equivalent impedance.

The open-loop output voltage U of the two-port network in Fig. 6 (b) is

$$U = v_{AM}\frac{2C_{AG}C_{ps}+C_{AG}C_{CG}+C_{AG}C_{DG}+C_{AG}C_{sg}+C_{ps}C_{CG}+C_{ps}C_{DG}+C_{ps}C_{sg}}{2C_{AG}C_{ps}+C_{AG}C_{CG}+C_{AG}C_{DG}+C_{AG}C_{sg}+2C_{ps}C_{CG}+2C_{ps}C_{DG}+2C_{ps}C_{sg}}. \quad (3)$$

The internal impedance Z of the two-port network in Fig. 6 (c) is

$$Z = \frac{2C_{ps}+C_{CG}+C_{DG}+C_{sg}}{\omega(2C_{AG}C_{ps}+C_{AG}C_{CG}+C_{AG}C_{DG}+C_{AG}C_{sg}+2C_{ps}C_{CG}+2C_{ps}C_{DG}+2C_{ps}C_{sg})}. \quad (4)$$

The CMV across the input capacitors can then be formulated as (5), with all variables provided in (6).

$$v_{pg} = P_1 v_{AM} + P_2 v_{BM} + S_1 v_{CN} + S_2 v_{DN} \quad (5)$$

$$\begin{cases} P_1 = \dfrac{2C_{AG}C_{ps}+(C_{AG}+C_{ps})(C_{CG}+C_{DG}+C_{sg})}{(C_{AG}+C_{BG}+C_{pg}+2C_{ps})(C_{CG}+C_{DG}+C_{sg})+2C_{ps}(C_{AG}+C_{BG}+C_{pg})} \\ P_2 = \dfrac{2C_{BG}C_{ps}+(C_{BG}+C_{ps})(C_{CG}+C_{DG}+C_{sg})}{(C_{AG}+C_{BG}+C_{pg}+2C_{ps})(C_{sCG}+C_{DG}+C_{sg})+2C_{ps}(C_{AG}+C_{BG}+C_{pg})} \\ S_1 = \dfrac{C_{ps}(C_{CG}-C_{DG}-C_{sg})}{(C_{AG}+C_{BG}+C_{pg}+2C_{ps})(C_{CG}+C_{DG}+C_{sg})+2C_{ps}(C_{AG}+C_{BG}+C_{pg})} \\ S_2 = \dfrac{C_{ps}(C_{DG}-C_{CG}-C_{sg})}{(C_{AG}+C_{BG}+C_{pg}+2C_{ps})(C_{CG}+C_{DG}+C_{sg})+2C_{ps}(C_{AG}+C_{BG}+C_{pg})} \end{cases} \quad (6)$$

With the same calculation procedure, the voltage across the output capacitors is then shown in (7), and the variables are provided in (8).

$$v_{sg} = P_3 v_{AM} + P_4 v_{BM} + S_3 v_{CN} + S_4 v_{DN} \quad (7)$$

$$\begin{cases} P_3 = \dfrac{C_{ps}(C_{AG}-C_{BG}-C_{pg})}{(C_{CG}+C_{DG}+C_{sg}+2C_{ps})(C_{AG}+C_{BG}+C_{pg})+2C_{ps}(C_{CG}+C_{DG}+C_{sg})} \\ P_4 = \dfrac{C_{ps}(C_{BG}-C_{AG}-C_{pg})}{(C_{CG}+C_{DG}+C_{sg}+2C_{ps})(C_{AG}+C_{BG}+C_{pg})+2C_{ps}(C_{CG}+C_{DG}+C_{sg})} \\ S_3 = \dfrac{2C_{CG}C_{ps}+(C_{CG}+C_{ps})(C_{AG}+C_{BG}+C_{pg})}{(C_{CG}+C_{DG}+C_{sg}+2C_{ps})(C_{AG}+C_{BG}+C_{pg})+2C_{ps}(C_{CG}+C_{DG}+C_{sg})} \\ S_4 = \dfrac{2C_{DG}C_{ps}+(C_{DG}+C_{ps})(C_{AG}+C_{BG}+C_{pg})}{(C_{CG}+C_{DG}+C_{sg}+2C_{ps})(C_{AG}+C_{BG}+C_{pg})+2C_{ps}(C_{CG}+C_{DG}+C_{sg})} \end{cases} \quad (8)$$

(5) and (7) are the analytical CMV model for DAB converter, which is derived from the general CM topology shown in Fig. 4. In equations, the CMVs at input and output are both decided by all four CMV sources.

Based on (6) and (8), the variables at both sides have similar expressions. When the primary-side full bridge has the symmetric layout for two legs, which means C_{AG}=C_{BG}, P_1 is equal to P_2 and P_3 is equal to P_4. A same conclusion applies to the secondary side. Hence the input and output CMV are

$$\begin{cases} v_{pg} = P_1(v_{AM}+v_{BM})+S_1(v_{CN}+v_{DN}) \\ v_{sg} = P_3(v_{AM}+v_{BM})+S_3(v_{CN}+v_{DN}) \end{cases}. \quad (9)$$

Variables in the simplified equations are then

$$\begin{cases} P_1 = P_2 = \dfrac{2C_{AG}C_{ps}+(C_{AG}+C_{ps})(2C_{CG}+C_{sg})}{(2C_{AG}+C_{pg}+2C_{ps})(2C_{CG}+C_{sg})+2C_{ps}(2C_{AG}+C_{pg})} \\ S_1 = S_2 = \dfrac{-C_{sg}C_{ps}}{(2C_{AG}+C_{pg}+2C_{ps})(2C_{CG}+C_{sg})+2C_{ps}(2C_{AG}+C_{pg})} \end{cases} \quad (10)$$

$$\begin{cases} P_3 = P_4 = \dfrac{-C_{pg}C_{ps}}{(2C_{CG}+C_{sg}+2C_{ps})(2C_{AG}+C_{pg})+2C_{ps}(2C_{CG}+C_{sg})} \\ S_3 = S_4 = \dfrac{2C_{CG}C_{ps}+(C_{CG}+C_{ps})(2C_{AG}+C_{pg})}{(2C_{CG}+C_{sg}+2C_{ps})(2C_{AG}+C_{pg})+2C_{ps}(2C_{CG}+C_{sg})} \end{cases} \quad (11)$$

To verify the proposed general CM topology for DAB converter with analytical model in (5) and (7), a DAB prototype is set up with parameters shown in TABLE II.

Table II Information of the Prototype

Names	Values
Leakage inductance reflected to the primary side (L_s)	18.7μH
Transformer turn ratio (n)	2:1
Switching frequency (f_s)	100kHz
Primary side switches (P#)	SCT3030KL
Secondary side switches (S#)	SCT3022ALHR
Paralleled switches	2

After including parasitic capacitances in the DAB converter, the topology with different CM capacitors is shown in Fig. 7. C_{p1} is the parasitic capacitance between the polygon of primary side DC+ and ground, and C_{p4} is the parasitic capacitance between primary side DC- and ground. C_{p2}, C_{p3}, C_{p5} and C_{p6} are the parasitic capacitance from switches to ground via the heatsink. C_{s1} is the parasitic capacitance between secondary side DC+ polygon and ground, and C_{s4} is the parasitic capacitance between secondary side DC- and ground. C_{s2}, C_{s3}, C_{s5} and C_{s6} are the parasitic capacitance from switches to ground via the heatsink. C_{ps} is the equivalent winding capacitance between the primary and secondary side of the transformer. Other parasitics such as inductance (nH) and resistance (mΩ) caused by PCB traces have little influence on the CM performance in the high frequency domain compared with capacitance above (pF), which are ignored in this paper.

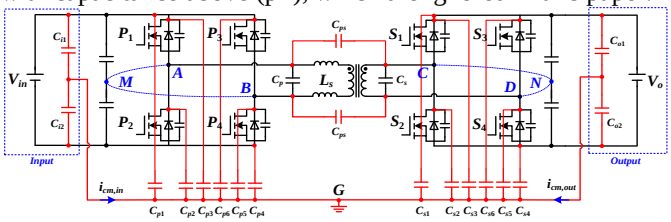


Fig. 7. Common-mode loops in the DAB converter.

With TO-247 SiC MOSFETs, the CM capacitance of the switches is between the drain and the ground. All parasitic capacitance providing paths for CMI in the prototype is summarized in TABLE III. The figure of the prototype will be shown in Section V.

Table III Summary of Parasitic Capacitance

Names of Capacitance	Symbol	Values
Drain to Ground (Primary)	$C_{p2,\,3,\,5,\,6}$	200pF
Drain to Ground (Secondary)	$C_{s2,\,3,\,5,\,6}$	160pF
DC+ or DC- to Ground (Primary)	$C_{p1,\,4}$	300pF
DC+ or DC- to Ground (Secondary)	$C_{s1,\,4}$	220pF
Primary side to secondary side (Transformer)	C_{ps}	37.5pF
Equivalent capacitance (Input)	$C_{i\#}$	100pF
Equivalent capacitance (Output)	$C_{o\#}$	100pF

Furthermore, all the capacitances in generalized model are

$$\begin{cases} C_{pg} = C_{i1} + C_{i2} + C_{p1} + C_{p3} + C_{p4} + C_{p6} = 1200\,pF \\ C_{AG} = C_{p2} = 200\,pF \\ C_{BG} = C_{p5} = 200\,pF \\ C_{sg} = C_{o1} + C_{o2} + C_{s1} + C_{s3} + C_{s4} + C_{s6} = 960\,pF \\ C_{CG} = C_{s2} = 160\,pF \\ C_{DG} = C_{s5} = 160\,pF \end{cases} . \tag{12}$$

Considering the parameters mentioned in Table.III, the analytical CMV model particularly to our built prototype at the input and output sides is formulated as

$$\begin{cases} v_{pg} = 0.1409(v_{AM} + v_{BM}) - 0.0159(v_{CN} + v_{DN}) \\ v_{sg} = -0.0199(v_{AM} + v_{BM}) + 0.1449(v_{CN} + v_{DN}) \end{cases} . \tag{13}$$

Although in the past, some qualitative analysis indicates the high frequency switching actions of four phase legs are the excitations of the DAB CMV and CMI, (5) and (7) quantify the input and output CMVs and indicates CMVs are determined by the primary and secondary H-bridges together. The high frequency voltage generated by each bridge leg is a two-level waveform. By summing all of them together, the input and output CMV can be a multi-level waveform. According to P_1, P_2, S_3 and S_4 in (6) and (8), the parasitic capacitance from middle point of the bridge leg to the ground caused by the heatsink provides the path for CMI at the primary side or secondary side. The winding capacitance of the transformer make the CM loops at both sides coupled together. Last but not the least, from the equation (13), the input CMV is dominated by the primary side H-bridge and the output CMV is dominated by the secondary side H-bridge, respectively, another major finding of this paper.

In phase-shift control algorithms of the DAB, the phase angles between different phase legs are implemented, which can shape the waveform in (12) drastically. Based on the analytical model developed in this Section, the input and output CM behaviors of the DAB can be quantified when imposing various phase angles in SPS, DPS and TPS modulation strategies, which is the main content of Section IV.

IV. Consideration of Common-Mode Voltage Based on Multiple Phase-Shift Modulations

With the quantified CMV at input and output presented in Section III, this section will investigate various impact factors of CM performance of the DAB converter, mainly the phase shift and ZVS current.

A. Modulation Strategies in DAB

For phase shift controls, when the inner phase shift is applied to H-bridge, its output voltage becomes a symmetric three-level waveform. For other hybrid modulation strategies, the output voltage of the H-bridge is an asymmetric three-level waveform. While different modulation strategies change the outlook of the CMV, this paper particularly focus on SPS, DPS and TPS, as shown in Fig. 8.

For the SPS control, there is no inner phase shift at either primary side or secondary side in Fig. 8 (a), which means theoretically there is no CMV source existing. In Fig. 8 (b), when the input voltage is higher than the reflected output voltage, the inner phase shift is implemented at the primary side H-bridge (PDPS). Hence the CMV source is generated by the primary-side H-bridge. If the inner phase shift is only implemented at the secondary side (SDPS), the CMV source only appears at the secondary side, as shown in Fig.8 (c). In TPS control, both sides have inner phase shifts contributing to the CMV and CMI, as shown in Fig. 8 (d). All CMV is shown as the last plot of each figure. It remains the same for hybrid modulation strategies.

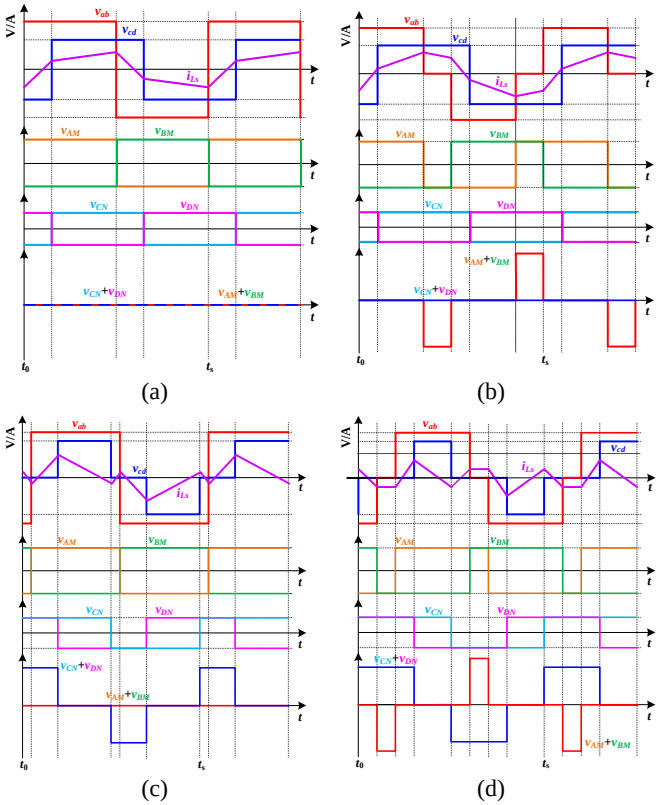


Fig. 8. Switching waveforms of different modulations: (a) SPS; (b) PDPS; (c) SDPS; (d) TPS.

Based on the analytical mode in Section III, for DPS control, the input and output CMV should be three-level waveforms,

which is the proportion of the output voltage of the H-bridge at primary side or secondary side. When using TPS control, the input and output CMV should be five-level waveforms, which are combinations of the output voltage of the primary side and secondary side H-bridges.

An Ltspice simulation model is built to verify the analysis above, with the simulation result shown in Fig. 9. The input voltage is 400V, the output voltage is 150V and the power rating is 500W, which for a 20kW DAB is very light load. Hence TPS modulation strategy is carried out in the simulation model. Both primary-side and secondary-side H-bridges act as CMV sources. The pulses only appear when there is zero platform at output voltage of either H-bridge. The voltage across the equivalent common-mode capacitors in input voltage source and load is five-level, which is decided by the primary side and secondary side H-bridges together. The common-mode loops of both sides are coupled through the equivalent CM capacitor of the transformer. The voltage values of such five-level waveforms are also marked in Fig. 9. Based on the equation (12) in Section III, with 400V input voltage and 150V output voltage, the CMV at the input and output caused by the primary side H-bridge is calculated as 56.36V and 7.95V, respectively. The CMV at output caused by the secondary side H-bridge should be 2.38V and 21.73V. All numbers are aligned with the simulation result shown in Fig. 9.

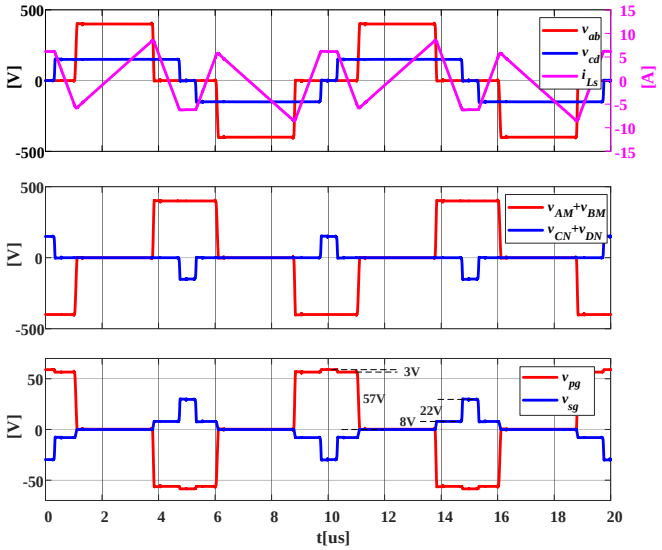


Fig. 9. Ltspice simulation result of input and output CMV in TPS modulation @ input voltage 400V, output 150V and 500W.

B. ZVS Realization in DAB

With a certain prototype of the DAB converter, the three-level waveform generated by H-bridge at both sides can decide the common-mode performance. As shown in previous sections, input voltage, output voltage and modulation strategies decide the voltage levels of different plateaus across the parasitic capacitors. The rising and falling edges of the CMV introduces the CMI flowing through parasitic capacitors. On the other hand, most of existing modulation strategies put ZVS on the high priority, which helps to increase efficiency and eliminate crosstalk between two complementary switches at the same leg. This is particularly important in the applications of WBG devices, which are operated at higher switching frequency and have higher switching-on loss than the switching-off loss, if ZVS is lost. Since such ZVS happens exactly at the edges of H-bridge output voltage, the influence of ZVS realization on CM performance of the DAB is also studied in this paper.

The voltage waveform between two middle points of H-bridge and the corresponding CMV is shown in Fig. 10 (a). The rising edges and the falling edges in each time intervals represent the moments when ZVS transitions happen to charge and discharge the switch output capacitors in the same phase leg, as shown in Fig. 10 (b). Here the leakage inductor of the transformer plays an essential role. The energy exchange between switch output capacitors, leakage inductor, input and output voltage sources occur in such transient process. Typically, the inductor should storage enough energy to help finish the ZVS transition within one dead time.

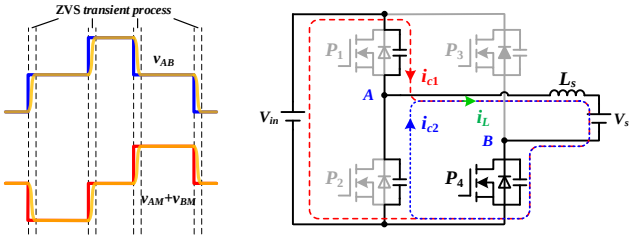


Fig. 10. ZVS transient process: (a) Output voltage of H-bridge and corresponding CMV; (b) ZVS transition loop in the H-bridge.

When designing the modulation strategies for the DAB converter, a certain principle should be followed to reach the optimized performance. Usually, to improve the efficiency, ZVS for all switches should be secured. Hence the initial inductor current which discharges the switch Coss should carefully considered. The ZVS current should large enough to complete the discharging process. The detailed analysis and modeling of the ZVS transition has already been discussed in [38]. A higher inductor current ensures ZVS and accelerates the transition time, which means rising and falling edges shown in Fig. 10 (a) can be finished in shorter time intervals.

Fig. 11 (a) shows the result of Ltspice simulation based on the DAB converter with parasitic capacitors, using the same simulation parameters of Fig.9. With the same TPS modulation algorithm [17] but different ZVS current, the output CMI is different. By controlling the phase shifts between different bridge legs, the transformer current at different switching actions can be adjusted to the desired value, and the power transfer can also be regulated. In both simulations, all switches realize ZVS. However, at 6A ZVS current, the CMI at the output has a higher peak value compared with the simulation under 3A ZVS current. The zoomed-in waveform at the first rising edge is shown in Fig. 11 (b). The transition time with 6A ZVS current is also much shorter than 3A. If we simply treat the parasitic capacitance of the common-mode loop as constant at different frequency, the charge flowing through the parasitic capacitors should remain unchanged, as shown in (14)

$$Q_1 = \int_0^{t_1} i_{cm1} dt = Q_2 = \int_0^{t_2} i_{cm2} dt \tag{14}$$

, where Q_1 and Q_2 are the charge exchange during the switching action in CM capacitance, and i_{cm1} and i_{cm2} are the CM current

flowing through LISNs. The ZVS transition happens when the inductor current charges and discharges the Coss in the bridge legs. With higher ZVS current, the charging and discharging process can be accelerated, which means higher dv/dt across the CM parasitic capacitors. In spectrums of the CMI in Fig. 11 (b), the current in red (with 6A ZVS current) should have larger components at high frequency domain, which might bring more challenges to the CM choke design [39].

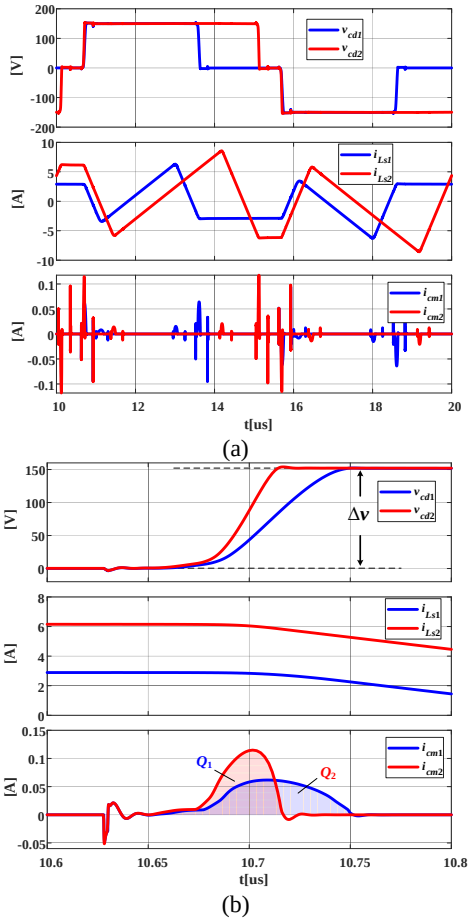


Fig. 11. Ltspice simulation based on different ZVS current: (a) switching waveform; (b) zoomed-in waveform in ZVS transient process.

As a summary, different modulation strategies in the DAB converter result in different common-mode performance. If the output voltage of H-bridge is a three-level voltage waveform, it can impact both input and output common voltage. For phase shift control, as long as there is an inner phase between two phase legs, it can generate CMV. SPS theoretically will not have CMV. In DPS and TPS control, both primary side and secondary side H-bridge can contribute to the CMV at either input or output, coupled by the parasitic capacitance of the transformer between primary side and secondary side. The primary side H-bridge has the major impact on the input common-mode performance, and the secondary side H-bridge plays a major role at output. Besides, the high ZVS current in many modulation strategies is beneficial to the ZVS realization but worsens the CM performance.

V. Experiment Verification

To verify the proposed DAB common-mode model in Section III and the influences of different modulation strategies on CM performance in Section IV, an experiment set-up is built, which is shown in Fig. 12. The components and parasitic parameters are provided in Table II and Table III. All the parasitic capacitances are measured with the impedance analyzer KEYSIGHT-E4990A at the switching frequency. The switch parasitic capacitance is measured from drain to heatsink before attaching the prototype to the copper plate, which are $C_{p2,\,3,\,5,\,6}$ and $C_{p2,\,3,\,5,\,6}$. The transformer parasitic capacitance C_{ps} are measured between the dotted terminals, which is independent from the prototype. Once the PCB board is attached to the copper plate with the stainless-steel standoff, the DC-link capacitances are measured without transformer connections. Then the transformer should be installed, and the heatsink should be connected to the copper plate.

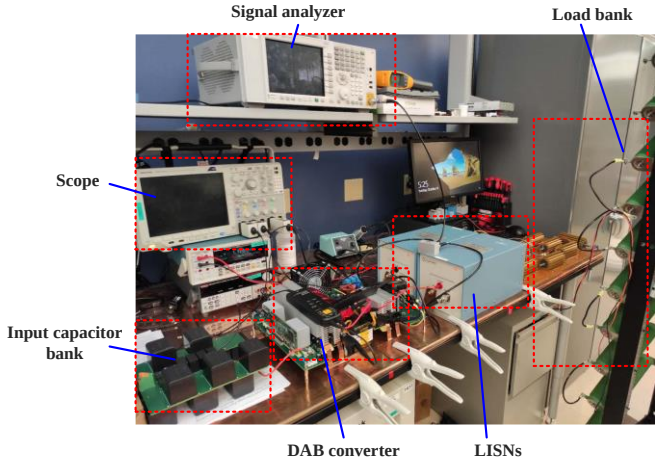


Fig. 12. Experimental set-up.

All experiments can be divided into two main parts. First, to verify the proposed common-mode model in Section III, the input and output common-mode voltage are measured. 100pF capacitors are added between the positive line and ground, the negative line and ground at both input and output to serve as the parasitic capacitors in source and load. Then the common-mode performance under different modulation strategies is measured with LISNs. The experiments with different ZVS current are implemented to compare the common-mode performances. Because of the symmetric structure of DAB, to simplify the test procedure, only the output common-mode performance is measured.

A. Testing the CMV

In Fig. 13 (a) and (b), the output CMV is measured under TPS and DPS modulation, respectively, when the input voltage is 400V and the output voltage is 150V. In TPS modulation, the output voltage of the primary side and secondary side H-bridge are both three-level waveforms. According to the analysis in Section IV, the output common-mode voltage should be a five-level waveform. Based on the equation (7) in Section III, the voltage rating should be 7.95V and 21.73V. The pulse width should be corresponding to zero plateaus of the output voltage of H-bridges. The voltage waveform in Fig. 13 (a) is consistent with the proposed analysis. For DPS modulation in Fig. 13 (b),

only the output voltage of the H-bridge at the primary side is three-level waveform. The output common-mode voltage should be a three-level waveform with a 7.95V platform. All voltage values shown in Fig. 13 (a) and (b) are consistent with the calculation result in the analytical model.

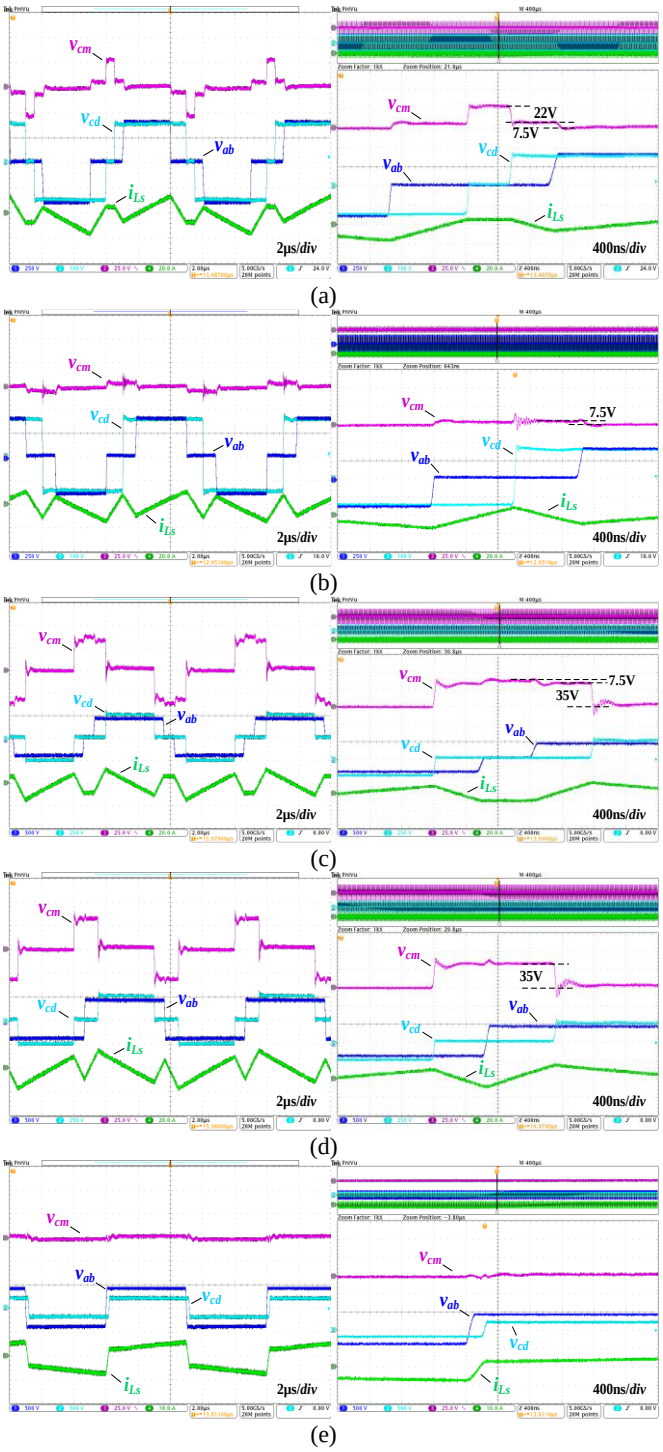


Fig. 13. Common-mode voltage in different modulation strategies: (a) TPS @ 150V output voltage: (b) PDPS @ 150V output voltage; (c) TPS @ 250V output voltage; (d) SDPS @ 250V output voltage; (f) SPS.

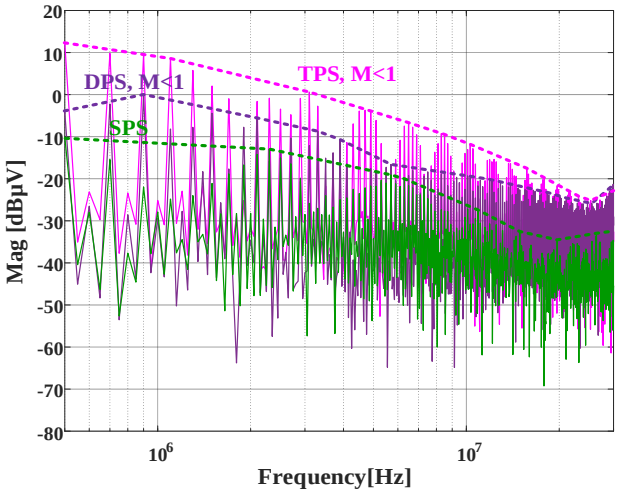
When the output voltage is 250V, the experimental result is shown in Fig. 13 (c) and (d). In TPS modulation, the output CMV is also five-level, where the platform caused by the H-bridge at the secondary side should be 36.22V based on the analytical model in Section III, which does not have significant difference from the tested waveform. In DPS modulation, only the H-bridge at the secondary side has the inner phase shift, which can generate three-level CMV at output. In Fig. 13 (e), SPS modulation is implemented under 200V output voltage. There is nearly no CMV at the output side.

The voltage rating of the CMV sources depend on the input and output voltage. The comparisons of CMV between the calculation based on analytical model proposed and the experiment under different voltage rating are shown in TABLE IV.

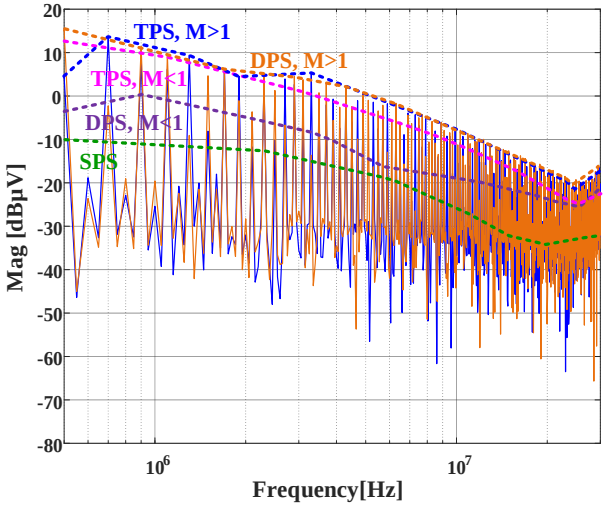
Table IV Secondary-side CMV Comparison between Analytical Model and Experiment

Modulation Strategy	Voltage Rating (V)	Platforms of output CMV	
		Calculation (V)	Experiment (V)
TPS	V_{in} 400/ V_o 150	7.95 / 21.73	≈ 7.5 / 22
	V_{in} 400/ V_o 250	7.95 / 36.22	≈ 7.5 / 35
PDPS	V_{in} 400/ V_o 150	7.95 / --	≈ 7.5 / --
SDPS	V_{in} 400/ V_o 250	-- / 36.22	≈ -- / 35
(SPS)	V_{in} 400/ V_o 190	0	≈ 0

Furthermore, the spectrums of the output CMV in Fig. 13 are plotted in Fig. 14. M here is the voltage gain, which is input voltage divided by the reflected output voltage. When M>1, the spectrums of TPS and DPS modulation are similar, since the inner phase shift is added to the secondary H-bridge which dominates the output CMV. When M<1, e.g., output voltage of 150V, the spectrum of TPS modulation has much higher amplitude than that of DPS, given that the secondary-side H-bridge does not contribute to the CMV at DPS control while both side H-bridge contribute to CMV at TPS control. Regardless, SPS always has the lowest amplitude. Here dashed lines represent the amplitude envelope of the CMV components.



(a)



(b)

Fig. 14. CMV spectrums of different modulation strategies: (a) TPS, PDPS and SPS when M<1; (b) all discussed modulation strategies.

To verify the accuracy of measured parasitic capacitances and the proposed general CM topology, the comparisons of the CMV distribution between the simulation model used in Fig. 9 which is built up according to the parameters of the prototype and the experiments are shown in Fig. 15. The input voltage is 200V, and the output voltage is 75V, where TPS modulation is applied. The static steady DM switching waveforms are shown in the first two sub-figures. All the CM voltages across the parasitic capacitors in the proposed general topology are measured and provided in red. The corresponding simulation results in Ltspice are shown in blue. The simulation model is also used to verify the derivation of the generalized CMV model proposed in this paper. The experiment results in Fig. 15 are consistent with the simulation results. The result indicates the accuracy of the measured parasitic capacitances and the proposed CM topology.

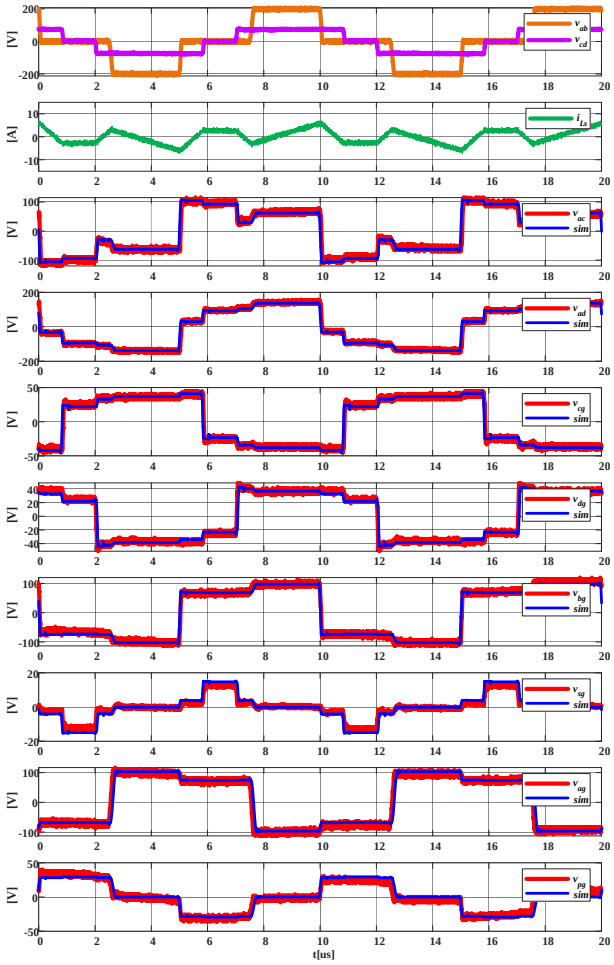


Fig. 15. The comparison of the CMV distribution between experiments and simulation model.

B. *Testing the CMI*

To further verify the analysis in Section IV, Line Impedance Stabilization Networks (LISNs) are used in experiments to measure the CMI under different modulation strategies. The overall layout of the experimental setup with LISNs is shown below.

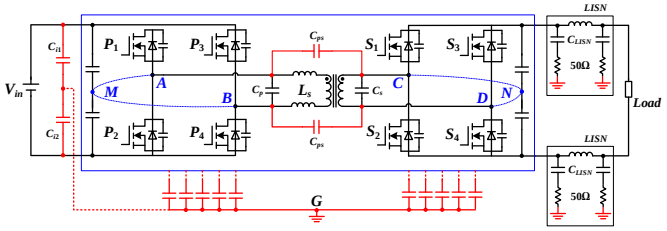


Fig. 16. Prototype structure with LISNs.

With the connection of LSINs, the analytical model for DAB converter should be further modified. The equivalent capacitance in input source or load should be replaced with impedance of LISNs which is composed of the impedance of C_{LISN} and 50Ω resistance in (15).

$$\omega C_{o\#} = \omega C_{LISN} + 50\Omega \ . \tag{15}$$

The spectrums of CMI under the different modulation strategies tested with LISNs have similar trend as the spectrums of the CMV discussed above, as shown in Fig. 17 (a) and (b).

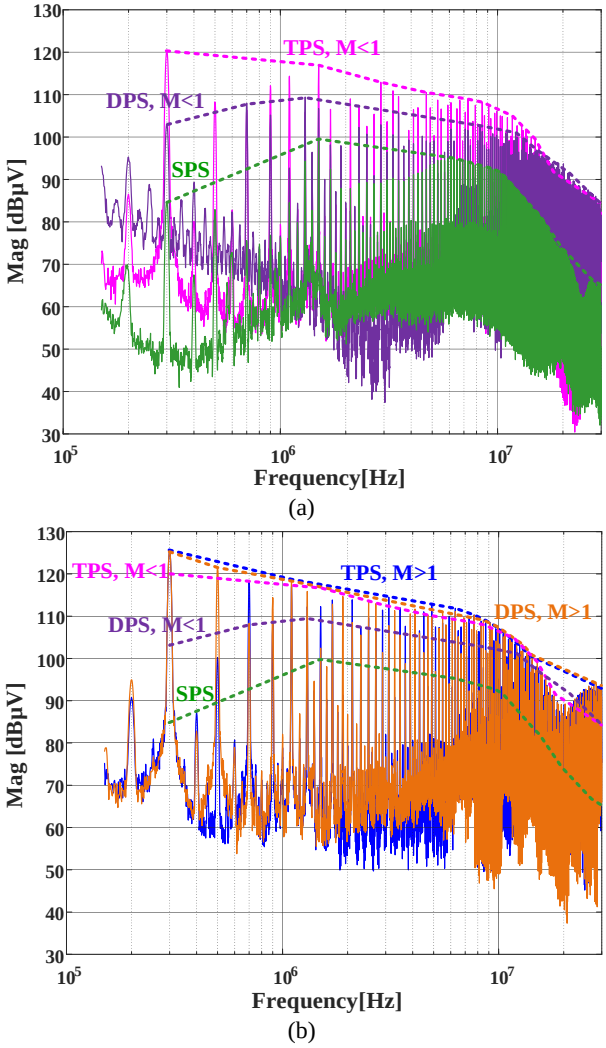


Fig. 17. CMI spectrums of different modulation strategies tested with LISNs: (a) TPS, PDPS and SPS when M<1; (b) all modulation strategies.

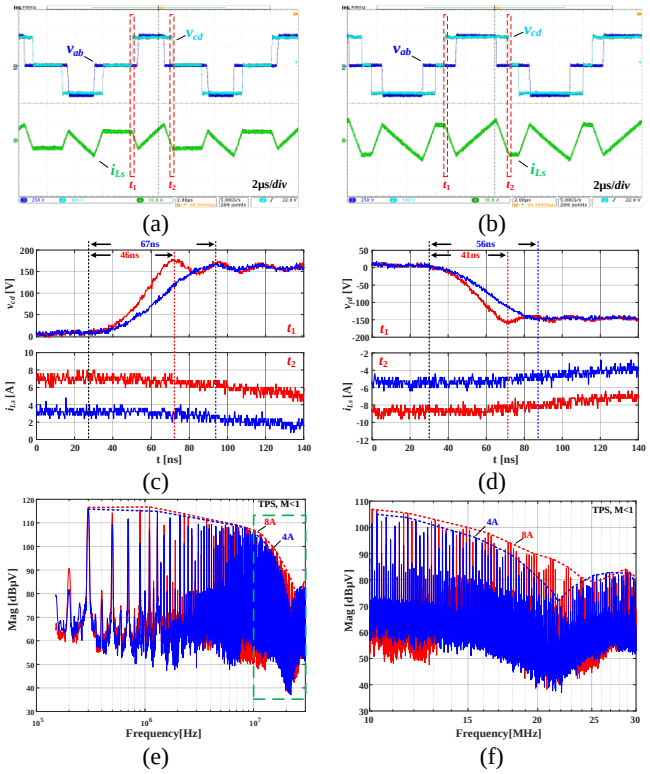


Fig. 18. Experiments with different ZVS current in TPS modulation when M<1: (a) switching wave with 4A ZVS current; (b) switching waveform with 8A ZVS current; (c) zoomed-in waveform of (a); (d) zoomed-in waveform of (b); (e) spectrum of output CMI; (f) zoom-in CMI spectrum.

Fig. 18 and Fig. 19 shows the experimental results of CMI under different ZVS current and output voltage. Here the secondary side H-bridge plays the main role for the output CMI, which mainly happens at the rising edge and the falling edge of the output CMV. Fig. 18 (a) is the switching waveform with 4A ZVS current. Fig. 18 (b) is the switching waveform based on 8A ZVS current. Fig. 18 (c) and (d) are rising and falling edges of the H-bridge output voltage at the secondary side, respectively, which can be an indicator of the ZVS transient process. With high ZVS current, the transition time is much shorter, which according to the analysis in Section IV the CMI should have larger components at high frequency region. Such assumption has been validated by experimental results shown in Fig. 18 (e) and (f). In Fig. 19, the input voltage is kept being 400V and the output voltage is adjusted to 250V. The rising edge of the secondary H-bridge output voltage happens at the peak current, which is mainly decided by the load. The falling edges in Fig. 19 (d) are corresponding to 4A and 8A ZVS current. Hence, at high frequency region in Fig. 19 (f) the CMI spectrum with 8A ZVS current still has higher amplitude than that with 4A ZVS current.

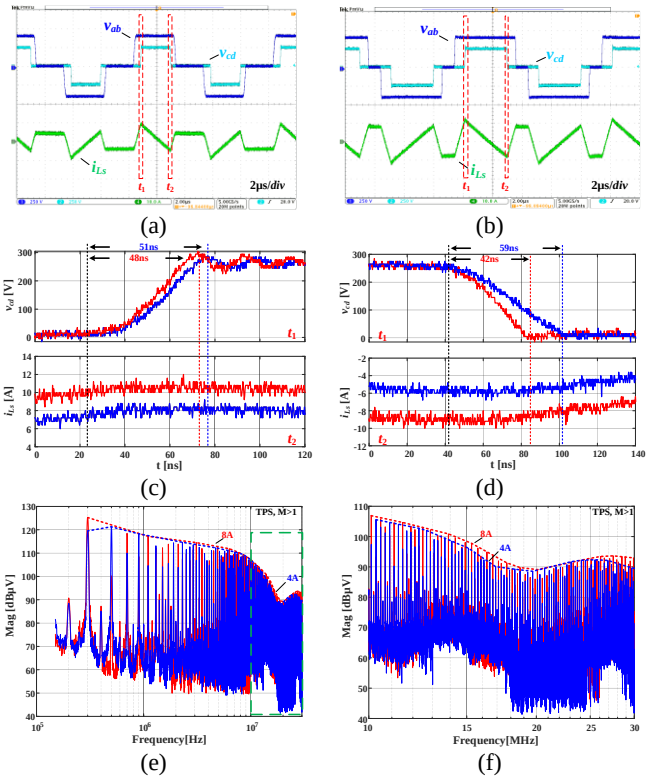


Fig. 19. Experiment with different ZVS current in TPS modulation when M>1: (a) switching wave with 4A ZVS current; (b) switching waveform with 8A ZVS current; (c) zoom-in waveform of (a); (d) zoom-in waveform of (b); (e) spectrum of output CMI; (f) zoom-in CMI spectrum.

VI. Conclusion

In this paper, the analytical CMV model of the DAB converter considering different parasitic capacitance is built. The input and output CMV are derived. With the proposed calculation, its CM performances under different modulation strategies are also quantified and compared. As long as the output voltage of the H-bridge in DAB is a three-level waveform, CMV is generated. The primary side H-bridge dominates the input CMV, and the secondary side H-bridge dominates the output CMV. The parasitic capacitor between the primary and the secondary sides of the transformer couples the common-mode loops of both sides together.

For phase shift controls, TPS control with inner phase shift at both primary and secondary side has the worst common-mode performance. DPS control with inner phase shift at either the primary or the secondary side also has the considerable CMI flowing through the input or the output. SPS theoretically does not have CMV. The proposed analytical model is validated by the experiment with the CMV and CMI measured at the output under different modulation strategies. In addition, when adjusting the transformer current to fulfill the ZVS requirement, higher ZVS current can ensure the realization of ZVS and accelerate the transient process. However, it makes the common-mode performance worse at high frequency region.

The proposed analytical model and the comparison of CM behaviors between different modulation strategies can provide the guideline when designing a CM chock for a DAB converter. In addition, other parameters of the prototype, such as transformer turn ratio, can be further tuned to suppress the CMI when considering the CM behavior at input or output. The modulation strategies can also be optimized not only focusing on efficiency and electronic stress, but also taking the CM behavior into consideration. This will be our future research work.

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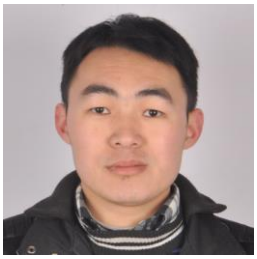

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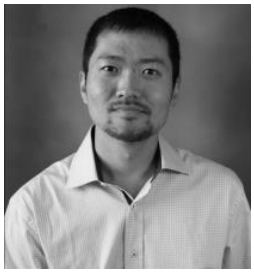

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