Overcurrent Capability Evaluation of 600 V GaN GITs under Various Time Durations

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***Abstract*— This work evaluates the overcurrent capability of 600V Gallium Nitride (GaN) Gate Injection Transistor (GIT) under different time durations and initial junction temperatures in a non-destructive approach. Setups and procedures are established to control drain current, time duration and junction temperature. The degradation of the device is examined after each overcurrent test. Gate-to-source voltage, drain-to-source voltage and drain current are measured for each test. Based on the test results, maximum withstand current, *It*-curve, I^2t-curve, and maximum withstand energy are determined for 600V GaN GIT. The results can be applied to the design of GaN-based converters for transient and overload conditions, as well as dc solid-state circuit breakers.**

Keywords—Gallium Nitride (GaN), overcurrent, solid-state circuit breaker.

I. Introduction

Featuring low specific on-state resistance, fast switching speed and near-zero reverse recovery, emerging GaN power devices have been recently studied intensively and applied to various power electronic systems [1, 2]. One important characteristic of power devices is overcurrent capability for short duration, since overcurrent often occurs during overload and transient states of the converters. In fact, power converters for applications such as uninterruptible power supply (UPS) for datacenters and solid state circuit breakers (SSCB) require intense overload capability that need to be considered when selecting power semiconductor devices and converter topologies [3-7].

In the literature, surge current capability of GaN devices in the third quadrant has been experimentally determined under half ac line cycle, e.g. 10 ms [8]. Similar work has also been conducted for SiC MOSFETs [5] and diodes [9]. To determine the dc overcurrent capability of devices, some of existing work use the safe operation area and electrothermal modeling [10-12]. In [12], the dc overcurrent capability of SiC MOSFET was tested, and the impacts of different thermal management were demonstrated. The test also used electrothermal model of the device and the maximum junction temperature was limited to 175 °C. Some other work studied the short circuit capability of GaN transistor, up to 14 µs. However, there is a lack of research on testing the dc overcurrent capability of GaN transistors at time duration from 10s of ms to several seconds, which is an important consideration for SSCB application. Since the device can withstand temperature variation above 200 °C [13, 14], it is necessary to reveal the dc overcurrent capability of the devices based on the test results.

To address the above issue, this paper presents a test method to evaluate the overcurrent capability of a top-cooled GaN GITs rated at 600V and 31A (IGOT60R070D1) in a non-destructive approach. The test results reveal the current and energy limits of the devices under different time durations and initial junction temperatures. The experimental results are also compared with the calculated results using electrothermal modeling.

II. Test Setup and Consideration

A. Test circuit and setup

The circuit used for overcurrent capability test and photos of the circuit are shown in Fig. 1 and Fig. 2, respectively. The circuit consists of a dc source, load resistor (R) and its equivalent series inductance (ESL), freewheeling diode (D_f), shunt resistor for current measurement (R_{sh}), device under test (DUT) and protection circuit for DUT. Passive voltage probes are used to measure drain-source voltage (V_{ds}) and gate-source voltage (V_{gs}) of DUT. A small PCB was added to facilitate the connection between DUT and curve tracer.

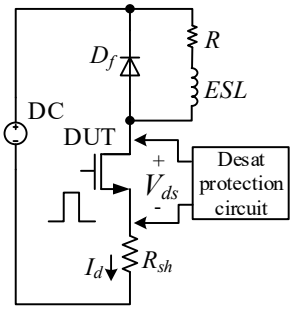


Fig. 1. Dc overcurrent capability test circuit for GaN transistor.

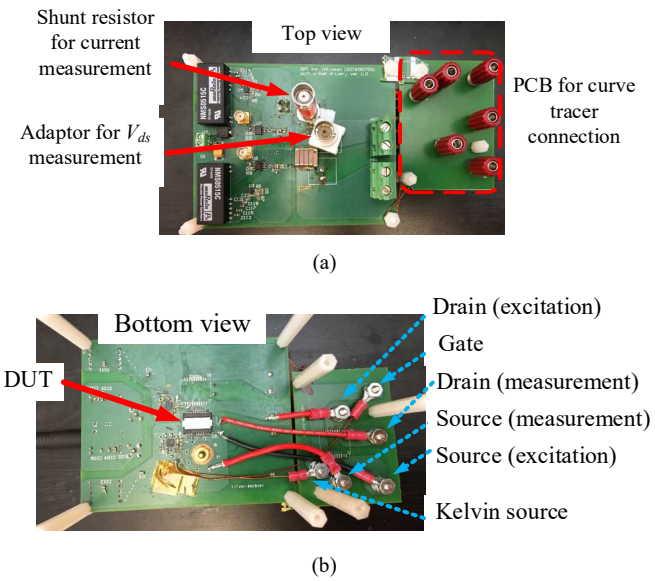


Fig. 2. Dc overcurrent capability test board, (a) top view; (b) bottom view.

The test setup is shown in Fig. 3. Since overload condition can occur at various junction temperatures in practical applications, the initial junction temperature (T_{j0}) of DUT is controlled from 25 °C to 150 °C in the test, with step size of 25 °C. Before each test, a hotplate is used to heat up the device to the desirable initial junction temperature. To transfer the heat from hotplate to DUT, a small copper block is soldered to the exposed metal heatslug of the DUT, and attached to the surface of hotplate using silicone gel. The correlation between the temperature setting of the hotplate and the initial junction temperature is summarized TABLE I.

TABLE I. CORRELATHIP BETWEEN JUNCTION TEMPERATURE AND HOT PLAT TEMPERAGURE

Junction temperature of devices (°C)	Temperature setting of hot plate (°C)
25	25
50	55
75	85
100	120
125	145
150	175

In the test, a single pulse is used to turn on DUT and the current in the circuit is determined by dc voltage and load resistor. The pulse is generated by the function generator, and durations were selected to be 10 ms, 20 ms, 100 ms, 1 s and 3 s. For each pulse duration, the test starts with relatively low dc voltage and current. Drain current is slowly increased by adjusting the dc voltage, until the maximum withstand current is reached. The dc current in the last successful test is recorded as the maximum overcurrent capability of the DUT.

Another procedure in the test is to examine the degradation status of the devices, since each test causes thermal stress to the devices. In this study, curve tracer is used to measure the static characteristics of DUT before and after each overcurrent test. The connection between the test board and the curve tracer is shown in Fig. 4.

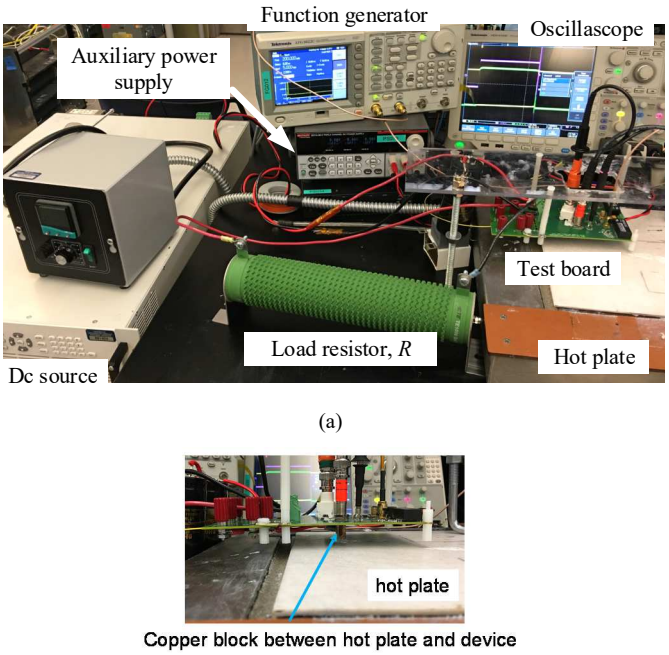


Fig. 3. Dc overcurrent capability test setup, (a) Overview; (b) heatsink transfer between hotplate and DUT.

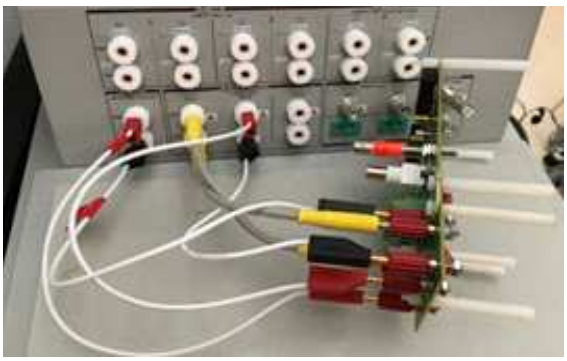


Fig. 4. Connection between test board and curve tracer for static characterization.

B. *Protection scheme for the test setup*

There are two objectives for the protection circuit of DUT: 1) it allows DUT to operate close to the limit, and 2) it protects DUT from degradation or failure.

To observe the device behaviors and waveforms at device limit, protection scheme was not removed. A turn-on pulse of 10 ms was applied to the DUT, and dc current was set to 41 A. The waveforms are shown in Fig. 5. Since this current and time duration exceed the limitation of DUT, the device saturates at about 9.9 ms. Drain-source voltage of DUT rapidly increases to the voltage of dc source (~200V). After the saturation, gate oscillation occurs and drain current of DUT drops to zero. It takes less than 10 µs from v_{ds} reaching 10V to the onset of gate oscillation. This time period is much shorter than the pulse durations considered in the test (10 ms ~ 3 s). Therefore, setting

desat protection with relatively high threshold voltage of 10 V has minimal impact on the test results of overcurrent capability, while it can also prevent the gate oscillation and potential failure of device.

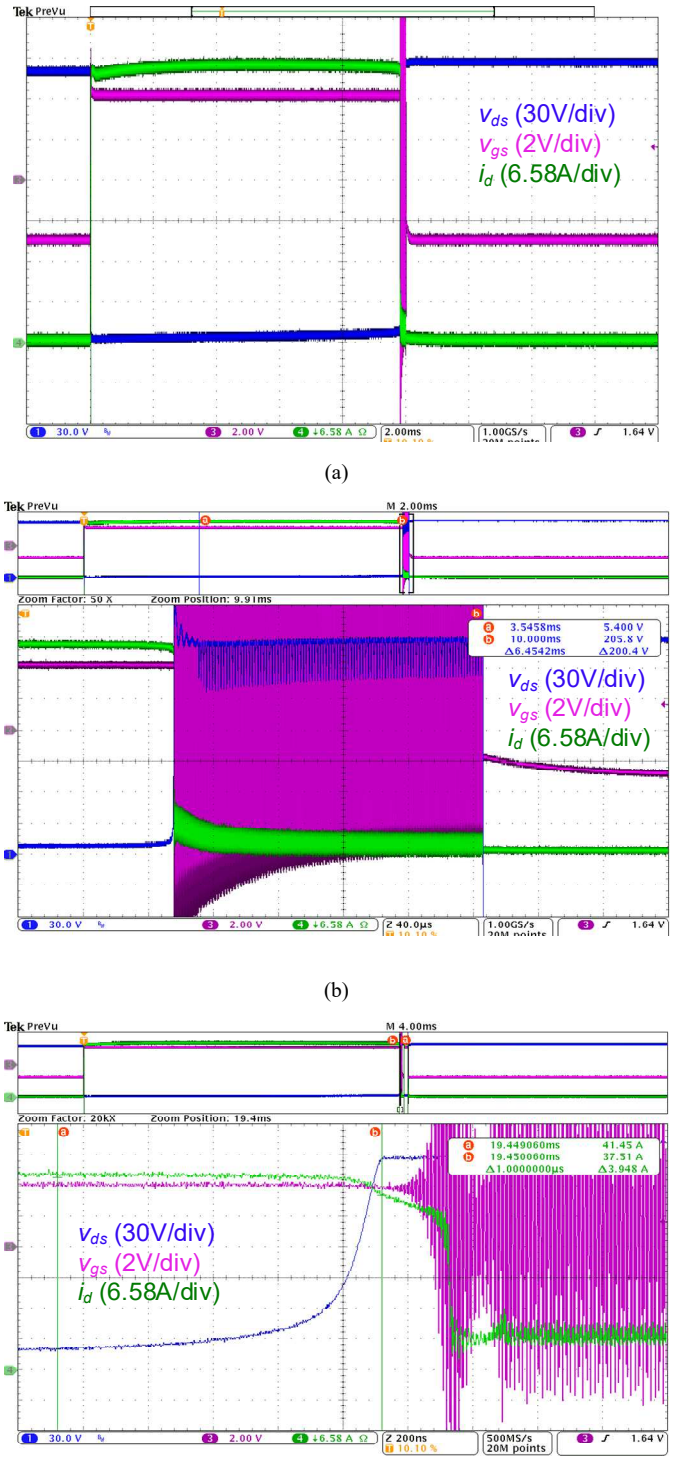


Fig. 5. Waveforms of high-current test without using desat protection, 2 ms/div; (b) zoomed-in view, 40 µs/div; (c) further zoomed-in view, 200 ns/div. Blue: drain-source voltage of DUT (30V/div), magenta: gate-source voltage of DUT (2V/div), and green: drain current of DUT (6.58A/div).

III. Experimental Results and Analysis

A. Experimental Results

The tests were conducted for five different pulse durations (10 ms, 20 ms, 100 ms, 1 s and 3 s), and the junction temperature before test ranges from 25 °C to 150 °C. The highest currents that do not trigger desat protection are plotted in Fig. 6, and the energy dissipated in the devices are summarized in Fig. 7.

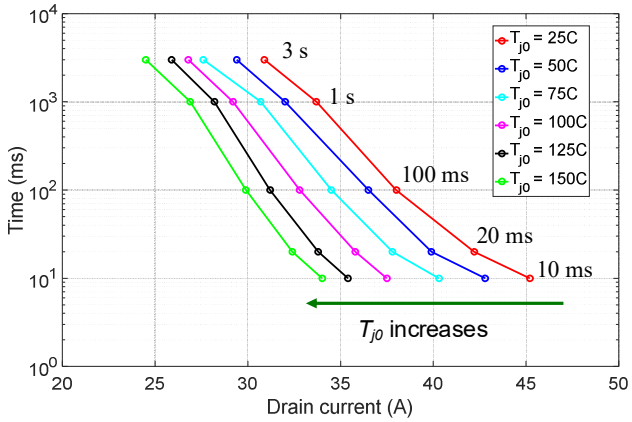


Fig. 6. Maximum withstand current of DUT at different initial junction temperatures and pulse durations.

Since the internal structure of the device is unknown to authors, the internal thermal distribution in the device is not investigated in this work. It can be observed that under the same pulse duration, the maximum withstand current of DUT depends on the T_{j0}, but energy is almost the same under different T_{j0}. This indicates that overcurrent capability of DUT can be limited by the local hotspot at temperatures much higher than 150 °C. As gate-source voltage oscillation occurs after the device saturates, one possibility is overheat of gate area [15].

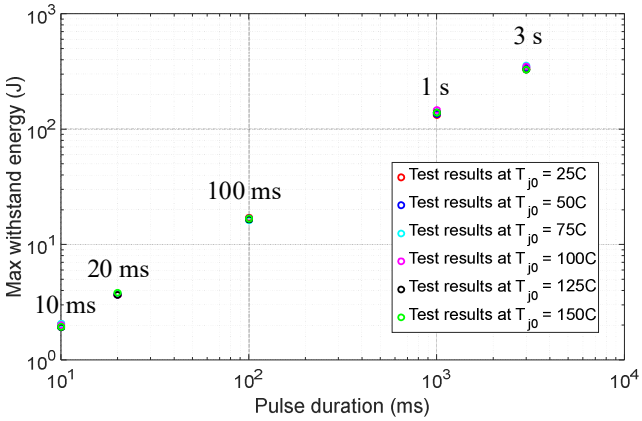


Fig. 7. Maximum withstand energy at different initial junction temperatures and pulse durations.

For converter and SSCB applications, if high precision measurements of drain-source voltage and drain current are both available, the energy of the devices can be calculated, and protection can be implemented based on the maximum withstand energy of devices. In case the drain-source voltage is

not available, overcurrent capability needs to be determined based on current measurement. The overcurrent capability in terms of It and I^2t integral is shown in Fig. 8 and Fig. 9.

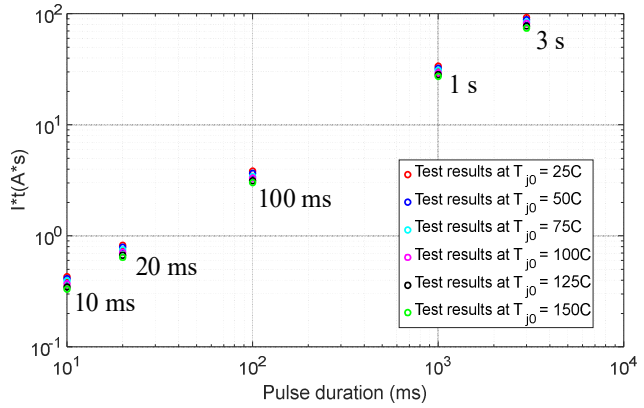


Fig. 8. It curve at different initial junction temperatures and pulse durations.

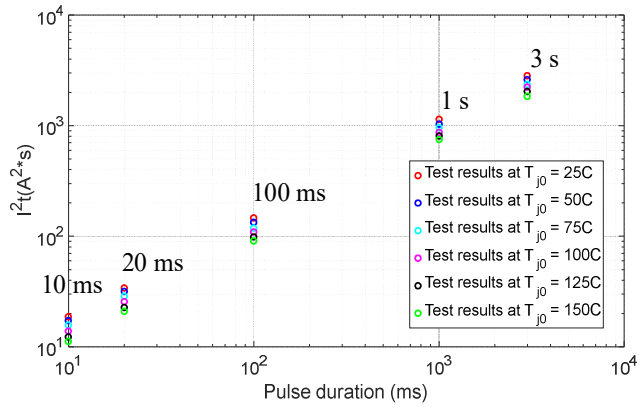
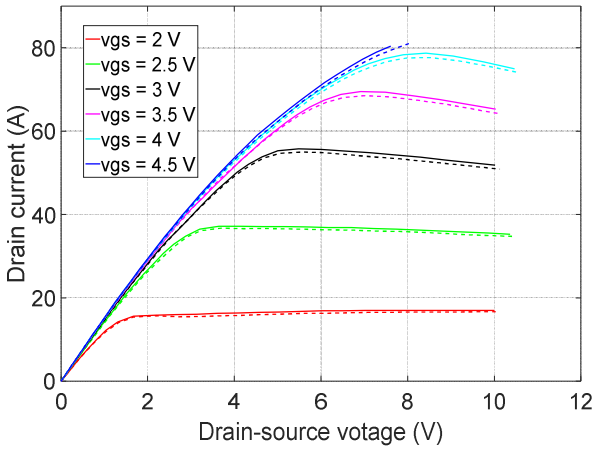
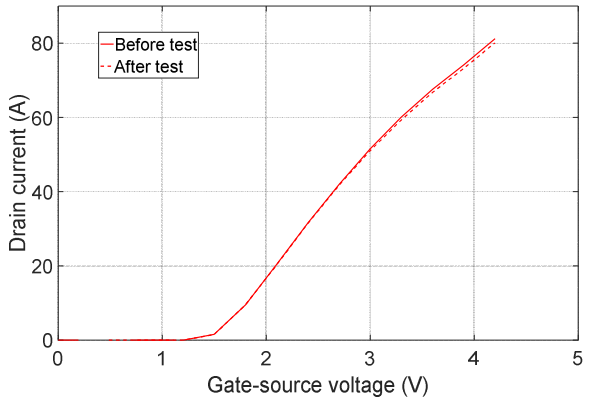


Fig. 9. I^2t curve at different initial junction temperatures and pulse durations.

To examine the degradation of the device, the static characteristics was conducted after each overcurrent test. And the results were compared with the static characteristics obtained before any overcurrent test. The characteristics of DUT before the test, and after all the tests are summarized in Fig. 10. Consistent static characteristics indicate that the DUT was not degraded in the test [16].



(a)



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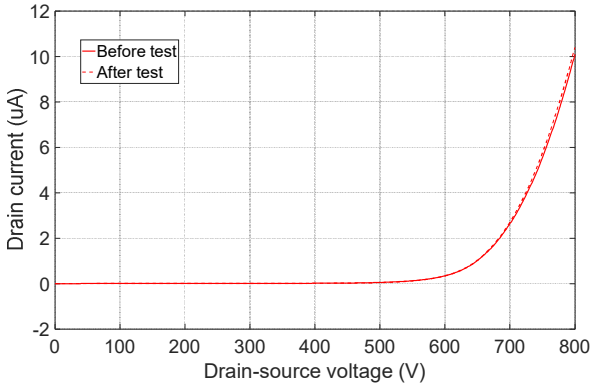


(c)

Fig. 10. Static characteristics of DUT before the test and after all the tests, (a) output characteristics I_d - V_{ds}, (b) Transfer characteristics, I_d - V_{gs}, (c) Leakage current, I_d - $V_{ds,off}$. solid lines: before the test, dashed lines: after all the tests.

B. *Comparison with Electrothermal Modeling*

Another feasible method to determine the overcurrent capability is to use electrothermal model. The thermal and electrical characteristics of the device at junction temperatures up to 150 °C can be extracted from the datasheet or static characterization. This includes the on-state resistance of the device (R_{dson}) and transient thermal impedance (Z_{thJC}). Considering that the R_{dson} depends on both junction temperature and drain current, the relationship between I_d and T_j at the end of a given pulse duration (T_p) is

$$T_j(T_p) = T_{case} + Z_{thJC}(T_p)\frac{\Delta t \sum_{n=0}^{n=\frac{T_p}{\Delta t}-1} I_d^2 R_{dson}(I_d, T_j(n\Delta t))}{t}. \quad (1)$$

where Δt is sufficiently small, and $T_j(0)$ is the initial junction temperature.

For a given maximum junction temperature ($T_{j,max}$) and T_p, $I_{d,max}$ can be calculated by

$$T_{j,max} = T_{case} + Z_{thJC}(T_p)\frac{\Delta t \sum_{n=0}^{n=\frac{T_p}{\Delta t}-1} I_{d,max}^2 R_{dson}(I_{d,max}, T_j(n\Delta t))}{t}. \quad (2)$$

In the calculation, the case temperature was assumed constant as the time durations are relatively short. The calculated results are plotted in Fig. 11. The initial junction temperature in the calculation is limited to 125 °C as the maximum junction temperature is 150 °C. The overcurrent capability of the device is identical when time duration is above 1 s, because the transient thermal impedance of the device reaches steady state after 1 s.

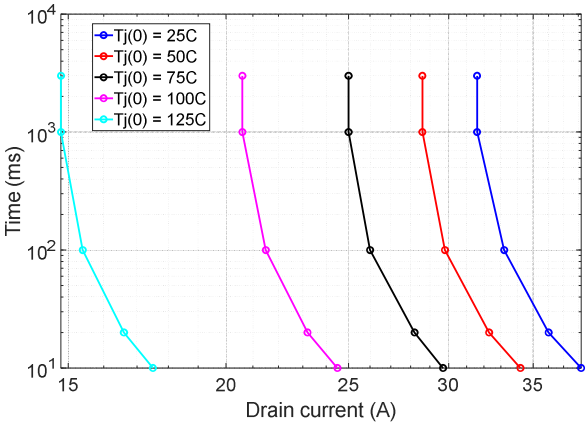
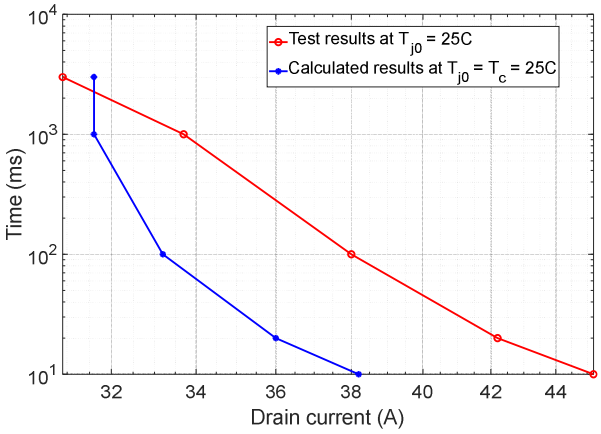
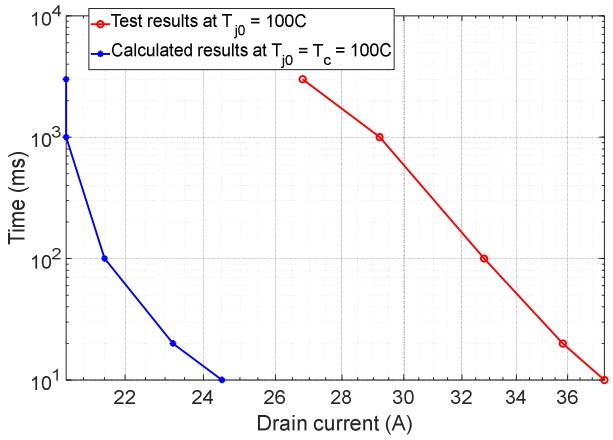


Fig. 11. Calculated dc overcurrent capability at different initial junction temperature, using $T_{j,max}$ = 150 °C.

The calculated results and the test results are compared, using initial junction temperatures of 25 °C and 100 °C. In most cases, the test results show higher overcurrent capability compared to the calculation results. The exception is 3 s with T_{j0} = 25 °C. This is because, in the test, very small amount of heat was transferred through the small copper block. As a result, the case temperature is not constant, and the case temperature increment can be more prominent at T_{j0} = 25 °C. However, in the calcualtion, the case temperagure is assumed constant, which equivalently to infinite heat transfer. The difference in thermal management can also affect the overcurrent capability of the device if time duration is longer than 1s [12].



(a)



(b)

Fig. 12. Calculated and test results (a) at T_{j0} = 25 °C, (b) at T_{j0} = 100 °C.

IV. Conclusion

In this paper, the dc overcurrent capability was experimentally determined. The test circuit, setup, and procedures were developed. Desat protection with relatively high drain-source voltage threshold ($V_{ds,th}$ = 10V) can allow the device to operate close to the limit, while protecting it from degradation. The maximum dc withstand current for GaN transistor under junction temperatures between 25 °C and 150 °C, and time durations between 10 ms and 3 s was tested. The maximum withstand energy, *it*-integral and i^2t-integral curves were derived. Compared with the electrothermal model using maximum junction temperature of 150 °C, the test results show much higher overcurrent capability. This indicates that the device can withstand more than 150 °C junction temperature for short durations. The results can be useful for the applications where overcurrent only occurs for limited number of times, such as dc SSCB. The long term reliability of the devices can still suffer if overcurrent and high temperature operation occur frequently [15].

Acknowledgment

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