IET Generation, Transmission & Distribution

*Research Article*

IET Journals
The Institution of Engineering and Technology

# Low cost, flexible, and distribution level universal grid analyser platform: designs and implementations

ISSN 1751-8687
Received on 7th January 2020
Revised 26th March 2020
Accepted on 6th April 2020
doi: 10.1049/iet-gtd.2020.0043
www.ietdl.org

*He Yin[1], Wenxuan Yao[2] ✉, Lingwei Zhan[2], Wenpeng Yu[1], Jiecheng Zhao[1], Yilu Liu[1,2]*

[1]*Min H. Kao, Department of Electrical Engineering and Computer Science, The University of Tennessee, Knoxville, TN 37996, USA*
[2]*Oak Ridge National Laboratory, Oak Ridge, TN 37830, USA*
✉ *E-mail: yaow1@ornl.gov*

**Abstract:** This study presents the designs and implementations of a distribution level open-universal grid analyser (Open-UGA) platform. The proposed Open-UGA platform consists of distribution-level phasor measurement units (PMUs), a standard signal generator, a router, and a server. Firstly, an overall introduction for the software, hardware, and server architectures of the Open-UGA platform is given. To give a detailed design, the software, hardware, server block diagrams, flowcharts, and printed circuit board photo of the Open-UGA platform are presented in detail. Then, four different types of distribution level PMU algorithms are introduced and implemented in the Open-UGA platform to verify the flexibility and reconfigurability. The flowcharts and functionalities of these four UGAs with different PMU algorithms are given as example implementations. Finally, a performance comparison is conducted with both quantitative and illustrative results.

## 1 Introduction

The synchronised phasor measurement technology has been developed for more than 30 years. As one of the key techniques of the wide-area measurement research area, synchrophasor measurement technologies have benefits on applications of power grid situational awareness, state estimation, and protection. To sense the power system, phasor measurement units (PMUs), which were originally designed for transmission level applications, have been utilised as synchrophasor measuring devices [1]. Interesting research topics for transmission-level PMUs have been widely discussed such as optimal PMU placement [2] and wide-area measurement system design [3]. However, transmission-level PMUs are suffering from the deployment location selections, high installation and manufacturing costs. In recent two decades, synchronised phasor measurement has been extended from transmission to distribution level. Distribution-level PMUs, such as frequency disturbance recorders (FDRs) [4], universal grid analysers (UGAs) [5], field-programmable gate array (FPGA)-based PMUs, and micro-PMUs ($\mu$-PMUs) [6] are developed and deployed.

Among distribution-level PMUs, FDRs are the first single-phase synchrophasor measurement devices of frequency monitoring network (FNET/Grideye) and utilise single phase at the distribution level to measure synchrophasors. FDRs were originally developed at Virgina Tech and now have been deployed with more than 300 units all over the world. However, FDRs have performance limitations such as low reporting rate, sampling inaccuracy, and lack of power quality parameter estimation. To overcome these drawbacks, UGAs are developed in the University of Tennessee, Knoxville, which are capable of sustaining a high reporting rate up to 120 Hz and calculating power quality parameters such as harmonics, signal-to-noise ratio (SNR), sags, and swells. Besides FDRs and UGAs, Pinte *et al*. [7] have introduced a FPGA-based PMU, which aims to have a high reporting rate. Meanwhile, $\mu$-PMUs are also designed with a high reporting rate and accurate phase angle [6].

The synchrophasor estimation algorithm is one of the most fundamental and critical parts of the distribution level PMUs. The general requirements for the synchrophasor estimation algorithm have been defined in IEEE C37.118.1-2011, 2014 [8], and IEEE/IEC International Standard – measuring relays and protection equipment – part 118-1 [9]. Among synchrophasor estimation algorithms, zero-crossing-based algorithm is a basic estimation algorithm that measures the time duration of the cycles [10]. Another widely used algorithm for synchrophasor calculation is the discrete Fourier transform (DFT)-based algorithm [11]. The DFT-based algorithm has a relatively low computational burden but the window size of the DFT and the off-nominal conditions have serious influences on the accuracy of the estimation [12]. DFT-based algorithms can be further enhanced to improve the measurement accuracy [13], widen the frequency range [14], and reduce the dynamic measurement error [15]. In addition to the DFT-based algorithms, other dynamic model-based algorithms can also be utilised in synchrophasor estimation [16, 17]. Meanwhile, the real-time point on wave (POW) measurement has been drawn increasing attention because (i) differential protections are based on POW data which needs at least a half or full cycle; (ii) power quality monitoring for inverters switching needs POW data since the frequency of power quality interference signal is up to several kHz levels and the harmonics are checked up to 50th order [18]; (iii) POW allows power quality detection such as voltage sag and swell; and (iv) POW in a smart home can be utilised to extract the working conditions of household appliances. Thus, it would be a great benefit to implement POW into distribution level PMUs.

However, different kinds of synchrophasor estimation and POW measurement algorithms have specific requirements on the hardware and software design of the distribution level PMUs. One distribution level PMU with a single algorithm may not satisfy the requirements of different PMU applications. This issue may become particularly serious when the requirements of the PMU applications are beyond the IEEE C37.118 standard, e.g. extreme fast estimation and high reporting rate for protection, accurate event predictions. Moreover, the existing commercial PMUs are not flexible and reconfigurable for new algorithm test and development. In addition to commercial PMUs, there are some Open-PMU projects such as Open-PMU LabVIEW project [19] and Open-PMU platform [20]. However, these platforms are still suffering from the high cost and the communication protocols are limited by the IEEE C37.118. Furthermore, the server of distribution level PMU should be redesigned to receive, parse, and store different kinds of synchronphasor data and other types of power system signals (e.g. the POW data) considering the noisy environment of the distribution power grid. To address the abovementioned issues, this paper proposes a low cost, flexible, and distribution level Open-UGA platform. The proposed Open-UGA platform is no longer limited by the IEEE C37.118 protocol

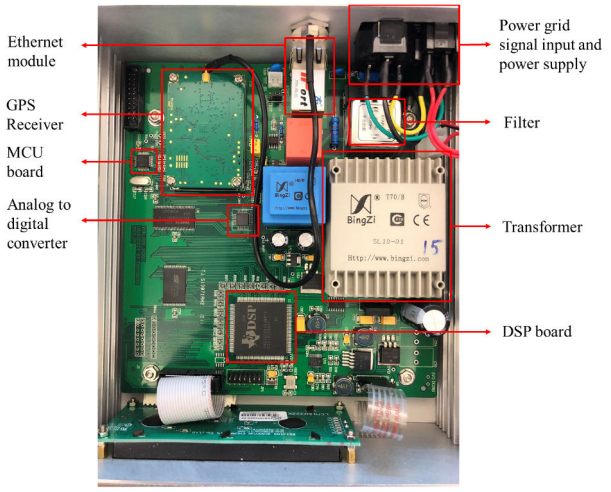


**Fig. 1** *PCB photo of open-UGA*

**Table 1** UGA specifications

| Module name | Type | Vendor |
|---|---|---|
| transformer | SL10-01 | BingZi |
| EMI filter | A1Ap-3A | ZhongBei |
| low pass | first order | NAN |
| filter | low pass filter | |
| ADC | AD7606 | analogue devices |
| GPS receiver | M12+TIMING | Ilotus |
| DSP board | TMS320C6713 | Texas Instruments |
| MCU board | STM32F103C8T6 | Stmicroelectroni |
| ethernet module | IPORT 3 | ZLG |

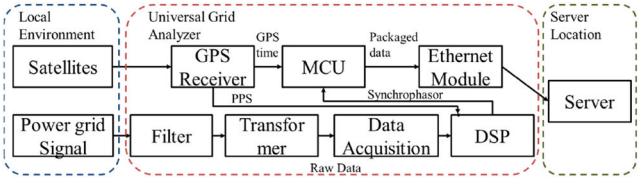


**Fig. 2** *Hardware architecture of Open-UGAs*

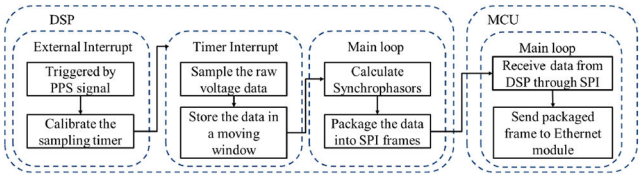


**Fig. 3** *Software architecture of UGAs*

on both PMU and server sides, which can satisfy the requirements of different kinds of algorithms, such as higher reporting rate (higher than 120 Hz) and different types of data parsers. To verify the capability of the proposed Open-UGA platform, four different kinds of algorithms are implemented. In addition, the steady-state and step response tests in the real world experiment system are designed to verify the performance of the proposed Open-UGA platform. The highlights of this study are summarised as follows:

- The distribution level Open-UGA platform is flexible and reconfigurable through which a variety of PMU algorithms can be implemented.
- The distribution level Open-UGA platform can achieve 6000 Hz reporting rate, 80 kHz sampling rate, and support different types of data streaming protocols, which is not limited by the IEEE C37.118 standard.
- Four real-world distribution level PMU algorithms are implemented to verify the performance of the Open-UGA platform.

## 2 Distribution level PMU platform

Unlike normal UGAs with a specific algorithm, the UGAs in the proposed platform are the Open-UGAs. In this Open-UGA, there is no default algorithm implemented. Thus, different kinds of distribution level PMU algorithms can be implemented, tested, and deployed in the Open-UGAs.

### *2.1 Hardware architecture*

As shown in Fig. 1, the photo of the printed circuit board (PCB) of the open-UGA gives an overview of the hardware architecture. The critical components are marked out with red squares. The hardware of the Open-UGA includes a global positioning system (GPS) receiver, a data acquisition, a digital signal processor (DSP) board, a microcontroller unit (MCU) board, and an Ethernet module. In addition, the Open-UGA specification including board and module types is summarised in Table 1. Note that A 16-bit ADC is used for synchronized sampling with sampling rate 200k Hz.

As shown in Fig. 2, in an Open-UGA, the GPS receiver is designed to receive the GPS signal from the antenna and generate the coordinated universal time and pulse per second (PPS) signal to the MCU and DSP. The power grid signal will be transformed and filtered before being sent to the data acquisition module. Note that with both the electromagnetic interference (EMI) and low pass filters, the aliasing issue in the phasor estimation process can be highly reduced. Then the data acquisition module can sample the raw data and send the digitally sampled signal to the DSP board. The DSP board is responsible for the implementation of the synchrophasor estimation, taking advantages of its ultra-high calculation ability. The synchrophasor data can be sent to the MCU board through serial peripheral interface (SPI) communication. Meanwhile, the MCU board is utilised to package the synchrophasor sent from the DSP board and send them to the Ethernet module. Finally, the Ethernet module can send the data package to servers through Ethernet simultaneously. In addition, to deploy an Open-UGA, an antenna is utilised for providing the GPS signal; a power cable is utilised for providing the power supply; an Ethernet cable is utilised for the data streaming to the servers.

### *2.2 Software architecture*

As shown in Fig. 3, the software architecture of the Open-UGA is given. First, the DSP uses its external interrupt pin to receive the PPS from the GPS receiver and calibrate the timer for sampling interval control. Note that this timer calibration is developed to reduce sampling-time error and improve the synchrophasor estimation accuracy. With help from the PPS interrupt, the synchrophasor sampling frequency error can be reduced by utilising a feedback controller. The detailed descriptions of the synchronised sampling strategy can be found in [21]. Then the timer interrupt of the DSP board will receive the sampling data from the data acquisition and store the data into a moving window. With synchronised sampling, in the main loop of the DSP board, the end-user can design estimation algorithms to estimate the synchrophasor at the designed moment. Meanwhile, the MCU will receive the synchrophasor estimation data in the main loop from the DSP board through a SPI communication protocol and then packages the data through the different protocol (e.g. IEEE C37.118.2 protocol). Note that to have a higher reporting rate, the IEEE C37.118.2 is revised with data stored in the analogue data part [5]. As shown in Fig. 4, in each redesigned IEEE C37.118.2 data frame, the first synchrophasor remains the same while the analogue data of the IEEE C37.118.2 is utilised for the second to the $N$ synchrophasors. With this design, multiple synchrophasors can be transmitted with one data frame. The benefits of this design are that: (i) multiple synchrophasors can share one set of the header, satellite, and power quality factor information through which the transmission burden can be reduced; (ii) the burden of the ethernet module can be highly reduced (extremely critical when dealing with the high reporting rate algorithms). Finally, the MCU will package the synchrophasor data and send the packaged frames to the Ethernet module through universal asynchronous receiver–transmitter communication protocol.

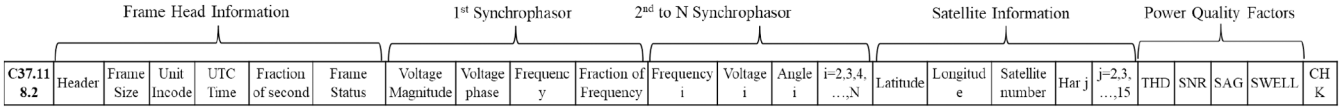


**Fig. 4** *The redesigned IEEE C37.118.2 protocol*

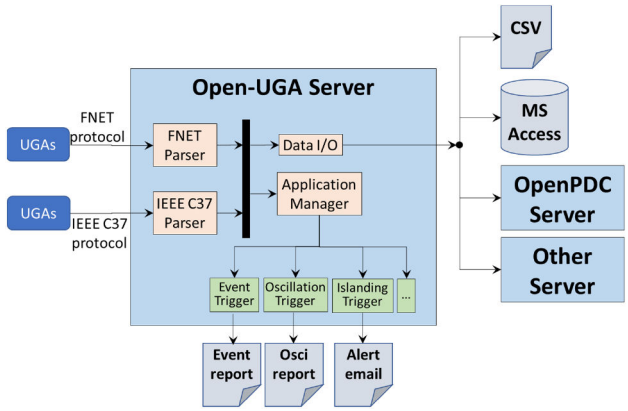


**Fig. 5** *Open-UGA server architecture*

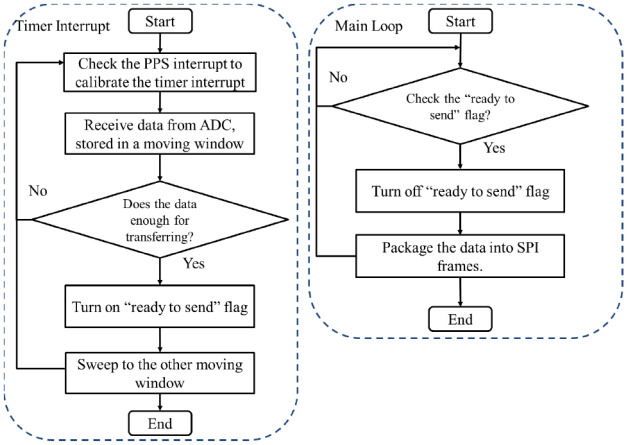


**Fig. 6** *Software architecture of POW-based UGAs*

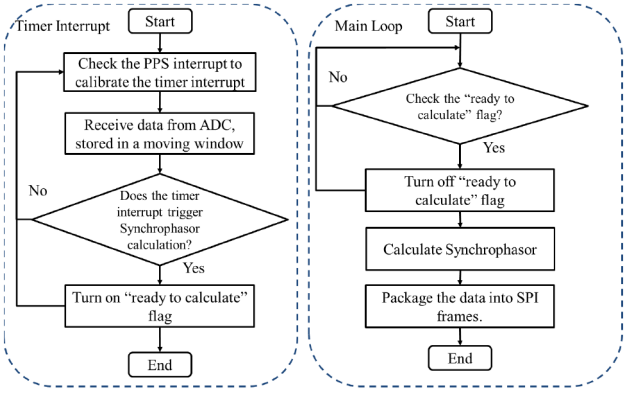


**Fig. 7** *Software architecture of ZCA-based UGAs*

### *2.3 Server architecture*

As shown in Fig. 5, the Open-UGA server can parse both the FNET and IEEE C37.118.1 protocol. Note that the FNET protocol was a synchrophasor communication protocol, which was created before the release of the C37.18 standard. After parser, the synchrophasor data or other types of data will be stored in both comma-separated values (CSV) and Microsoft access files, while they can also be transferred to other servers as well. In addition, the Open-UGA server has an application manager, which is utilised to detect events, oscillations, islandings etc. Two examples for the details for the application manager and its applications can be found in [22, 23]. In the Open-UGA platform, a router is utilised to connect the server and the Open-UGAs, which are not connected to Ethernet. In this case, only the CSV files are utilised for data storage and analysis. Note that the Open-UGA server is also specifically designed for the extreme long IEEE C37.118.2 frame parser. This study will not discuss the server design in detail while the detailed descriptions for the FNET server can be found in [24].

## 3 Example applications

The proposed Open-UGA platform is a generalised and flexible distribution level PMU test platform. In this section, four different applications have been implemented in the Open-UGAs to verify the flexibility and reconfigurability.

### *3.1 POW-based UGA*

With the benefits mentioned in the introduction section, it is worthy to design and develop a POW-based UGA with real-time POW data. In addition, a POW-based UGA can verify the capability of the high reporting rate of the Open-UGA. Thus, a POW-based UGA with a 6000 Hz sampling rate is designed and implemented in the Open-UGA.

From the software aspect, the POW-based UGA needs fast sampling and data transferring speed from the DSP to the MCU board. In this case, there may exist overrun issues. To solve this problem, the sampling programme is using timer interrupts while the SPI communication is realised in the main while loop. The sampling data is stored in two integer arrays, which will be utilised to store the sampling data alternatively. For example, when array A is utilised for recording the sampling data, array B will be utilised for SPI communication packaging. The DSP software architecture is summarised in Fig. 6.

### *3.2 Zero crossing algorithm (ZCA)-based UGA*

The ZCA is a classic and basic frequency estimation algorithm. verify that the Open-UGA is able to implement different kinds of synchrophasor estimation algorithms, an advanced zero-crossing-based frequency estimation algorithm [25] is implemented in UGAs, i.e. ZCA-based UGAs. Different from the conventional ZCA, a least square curve fitting method is utilised to improve the accuracy under noisy conditions. In addition, an ultra-high sampling rate (80 kHz) is applied to increase the estimation accuracy. With such a high sampling rate, the frequency reporting rate is still designed as 60 Hz since this algorithm needs one cycle data to estimate one frequency data.

With the same hardware architecture, the ZCA-based UGA has its specific software architecture. As shown in Fig. 7, the software architecture in the DSP board implements the ZCA into the main loop because the ultra-high sampling rate has taken up most of the memory of the DSP. Again, to avoid overrun, two alternative data arrays are utilised for temporal data storage and transfer, which is similar to the POW-based UGA. The different part of the ZCA implementation from the POW is that the ZCA has a much higher sampling rate and computational burden than the POW algorithm. On the other hand, the software in the MCU utilises the classic UGA architecture with a fixed reporting rate of 60 Hz.

The synchrophasor calculated in the ZCA-based UGA utilises the first-order polynomial function with respect to time to estimate the crossing location which can be described as

$$x_k = b_0 + b_1 k, \tag{1}$$

where $x_k$ is the voltage function.

With $n$ samples, $\boldsymbol{x} = [x_1, x_2, \ldots, x_n]$, (1) can be represented in the matrix form as

$$\boldsymbol{x} = \boldsymbol{bP}, \boldsymbol{P} = \begin{bmatrix} 1 & 1 \\ 1 & 2 \\ \vdots & \vdots \\ 1 & n \end{bmatrix}. \tag{2}$$

Since $P$ and $\boldsymbol{x}$ are known, $\boldsymbol{b}$ can be calculated as

$$\boldsymbol{b} = [\boldsymbol{P}^{\mathrm{T}}\boldsymbol{P}]^{-1}\boldsymbol{P}^{\mathrm{T}}\boldsymbol{x}\,. \tag{3}$$

Through determining $\boldsymbol{b}$, the zero-crossing location can be determined. In this case, the frequency can be calculated as

$$f = \frac{1}{T_1 + T_2}, \tag{4}$$

$$T_1 = T_{\mathrm{s}} \times (n_k - n_{k-1}), \tag{5}$$

$$T_2 = T_{\mathrm{s}} \times (n_{k-1} - n_{k-2}), \tag{6}$$

where $T_{\mathrm{s}}$ is the sampling period, $n_k$ is the sample count of last zero crossing, $n_{k-1}$ is the sample count of second to last zero crossing, and $n_{k-2}$ is the sample count of the third to last zero crossing.

### 3.3 DFT-based UGA

For the DFT-based UGA, a six-cycle recursive DFT algorithm is designed for single-phase synchrophasor estimation in the distribution system [26, 27]. The detailed algorithm of the DFT-based UGA is given in Fig. 8. A brief description of the calculate synchrophasor is given here. Assuming the sampling rate is $N$ sample per cycle, the first phasor can be calculated as

$$\overline{X} = \frac{1}{\sqrt{2}}(X_{\mathrm{c}} - \mathrm{j}X_s), \tag{7}$$

$$X_{\mathrm{c}} = \frac{2}{N}\sum_{k=1}^{N} x_k \cos\left(\frac{2\pi}{N}k\right), \tag{8}$$

$$X_{\mathrm{s}} = \frac{2}{N}\sum_{k=1}^{N} x_k \sin\left(\frac{2\pi}{N}k\right), \tag{9}$$

where $x_k$ stands for the $k$th sampling voltage in one moving window. Then, with recursive DFT described in [26], the new phasor can be calculated with every incoming voltage sample as

$$X_{\mathrm{c}}^{k+1} = X_{\mathrm{c}}^{k} + \frac{2}{N}(x_{k+1} - x_{k+1-N})\cos\left(\frac{2\pi}{N}k\right), \tag{10}$$

$$X_s^{k+1} = X_s^{k} + \frac{2}{N}(x_{k+1} - x_{k+1-N})\sin\left(\frac{2\pi}{N}k\right). \tag{11}$$

The $k$th phasor can be calculated

$$\phi_k = \tan^{-1}\frac{-X_{\mathrm{s}}^{k}}{X_{\mathrm{c}}^{k}}. \tag{12}$$

Given an assumption that the voltage phasor angle varies as a quadratic function

$$\phi_k = a_0 + a_1 k + a_2 k^2\,. \tag{13}$$

A computation window of $M$ phasor angle can be utilised to estimate the $a_0$, $a_1$, and $a_2$

$$\boldsymbol{\phi} = \boldsymbol{Ma} = \begin{bmatrix} 1 & 1 & 1 \\ 1 & 2 & 2^2 \\ \vdots & \vdots & \vdots \\ 1 & M & M^2 \end{bmatrix} \begin{bmatrix} a_0 \\ a_1 \\ a_2 \end{bmatrix}. \tag{14}$$

Matrix $\boldsymbol{a}$ can be calculated by the least error square solution as

$$\boldsymbol{a} = [\boldsymbol{M}^{\mathrm{T}}\boldsymbol{M}]^{-1}\boldsymbol{M}^{\mathrm{T}}\boldsymbol{\phi}, \tag{15}$$

where $[\boldsymbol{M}^{\mathrm{T}}\boldsymbol{M}]^{-1}\boldsymbol{M}^{\mathrm{T}}$ is constant matrix. To keep the curve fitting uniform, $\phi_1$ is set as zero. In this case, $\triangle f$ can be calculated as

$$\triangle f \simeq \frac{1}{2\pi} N f_0 (a_1 + 2a_2 N f_0 t), \tag{16}$$

where $f_0$ stands for the reference frequency, $t$ determines which instant inside the moving window the computed frequency corresponds to. Finally, the frequency $f$ can be calculated

$$f = f_0 + \triangle f\,. \tag{17}$$

Note that the unique characteristics for the DFT-based UGAs are the high reporting rate (i.e. 60 Hz), the resampling algorithm, and the power quality monitoring. The highest reporting rate for the DFT-based UGA is 120 Hz but this may sacrifice the power quality calculation. In this case, the 60 Hz reporting rate is chosen. Regarding the resampling, it is especially designed to improve the accuracy under off-nominal condition. In addition, the DFT-based UGA also calculates the power quality parameters including harmonics, SNRs, sags, and swells. These power quality parameters are calculated during the interval between two synchrophasor calculations. As a result, the reporting rate for the power quality parameters is 1 Hz [5].

### 3.4 High speed algorithm (HSA)-based UGA

In addition to the POW-, ZCA-, and DFT-based algorithms, a HSA with a 1440 Hz reporting rate is designed and implemented in the Open-UGAs, referred as HSA-based UGA [28, 29]. The HSA is designed based on a recursive DFT-based algorithm, which utilises the POW grid signals to estimate the continuous recursive phase angles and then estimate the continuous recursive frequencies. The advantages of this algorithm are the extremely low computational cost and ultra-high reporting rate. With such a high reporting rate, event detection, forecasting, and protection can be further studied with high-resolution frequency features.

Again, with the same hardware architecture, the software architecture of the HSA-based UGA is redesigned as shown in Fig. 9. From the DSP side, to implement the HSA, the HSA is implement within the timer interrupts. Owing to the small calculation burden of the HSA, there is no overrun issue happening in the DSP board and the synchrophasor calculation can be directly achieved within the timer interrupts. From the MCU side, due to the high reporting rate, the IEEE C37.118.2 standard is redesigned with 144 frequency estimations in one data frame. With all these changes, the synchrophasor data can be successfully received in the server.

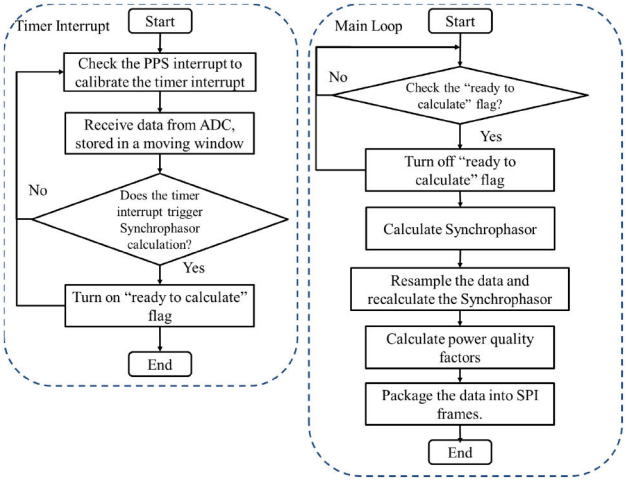


**Fig. 8** *Software architecture of DFT-based UGAs*

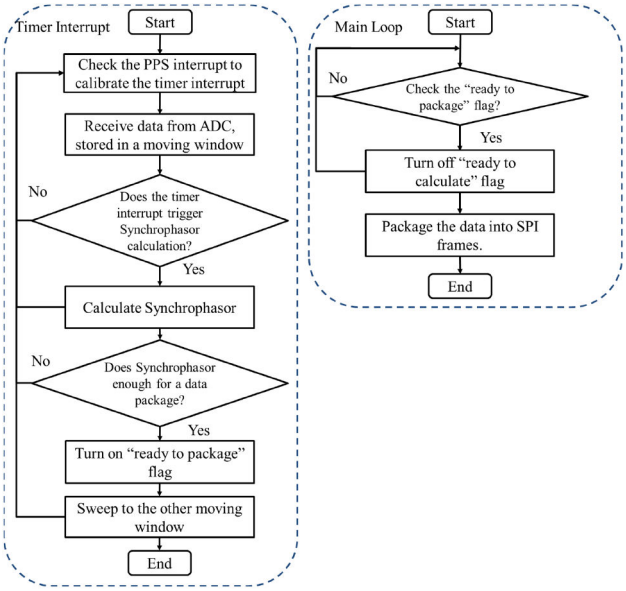


**Fig. 9** *Software architecture of HSA-based UGAs*

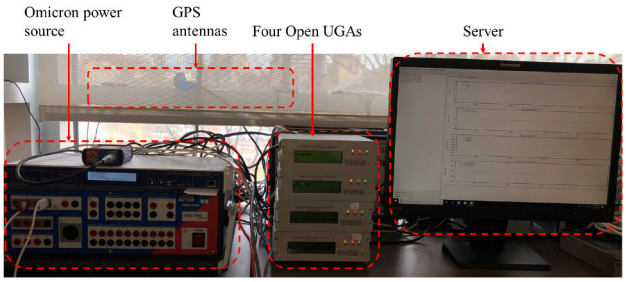


**Fig. 10** *Real world Open-UGA platform*

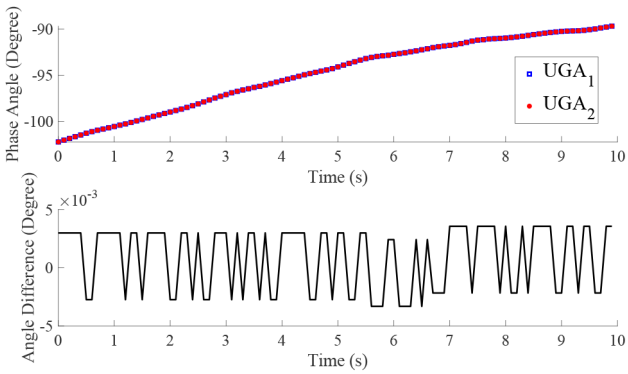


**Fig. 11** *Real world performance test with wall source at the same node*

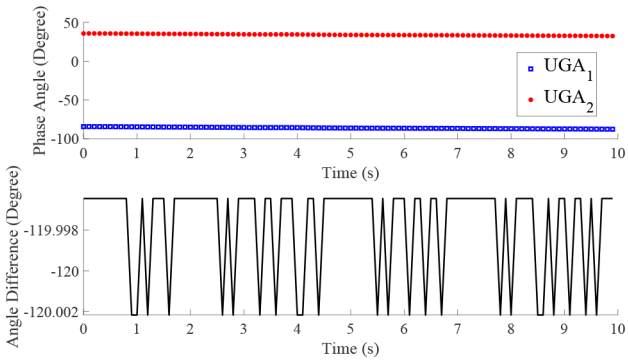


**Fig. 12** *Real world performance test with wall source at different node*

To give a better understanding of the HSA for calculating synchrophasor, the phase angle can be estimated with the same method discussed through (7)–(12). Assuming the number of $\phi_k$ utilised in estimating one frequency to be $(2L+1)$, a quadratic polynomial function is utilised to fit phase angles as

$$p(i) = c_0 + c_1 t(i) + c_2 t(i)^2, \tag{18}$$

$$i = 0, 1, \ldots, 2L, \tag{19}$$

where $t(i)$ is $(i-L)\Delta t$, $\Delta t$ is the time interval between two phase estimations, $c_0$, $c_1$, and $c_2$ are the coefficients, which can be estimated utilising least squares fitting technology. The frequency can be estimated as

$$f = \frac{1}{2\pi}\frac{\mathrm{d}p(i)}{\mathrm{d}t(i)} = \frac{a_1 + 2a_2(i-L)\Delta t}{2\pi}. \tag{20}$$

In this regard, the frequency estimation at $i = L$ can be written as

$$f = \frac{a_1}{2\pi}. \tag{21}$$

There are other details for the HSA such as the unwrapping algorithm discussed in [28, 29].

## 4 Experiment results

In this section, first, the real-time POW data generated from the Open-UGA will be shown with both steady-state and phase step responses from an ideal power source. Then, a comparison among three implements of the Open-UGAs is given under both steady-state and step responses. Since both the ZCA-based UGA and the HSA-based UGA are designed for frequency estimation, the performances of synchronised frequency measurement are evaluated.

### *4.1 Experiment test bench*

As shown in Fig. 10, the experiment test bench of the Open-UGA platform consists of a standard signal generator (includes an Omicron 256 plus and a SEK-2488 satellites synchronised network clock), four Open-UGAs, GPS antennas, a router, and a server. The Omicron power source can generate both ideal steady-state signals and step response signals, which are utilised as the signal inputs for the Open-UGAs. The desktop has installed the server software to receive and store the real-time data from the four Open-UGAs. The Open-UGAs are connected to the desktop through a router with Ethernet connection (i.e. a local area network). In addition, the GPS antennas provide the synchronisation signals to the Open-UGAs.

To emulate a real distribution network, an offline simulation can be set up under Matlab Simulink or power systems computer-aided design. Through the offline simulation, the amplitude and phases for a single node can be recorded and thus converted into voltage signal profiles. Utilising these profiles as inputs of the Omicron power source, the end-users can emulate the practical operating condition of one of the distribution network nodes. In this study, for verification purposes, only the steady-state and step response tests are given as examples.

To further justify the real-world performance of the Open-UGAs, two DFT-based UGAs are connected to the same real-world distribution network at the same node. As shown in Fig. 11, the phase angles and phase angle difference between two DFT-based UGAs show that the Open-UGAs have almost the same phase responses under the real distribution network while the phase difference is within ±0.0036°. Then, two DFT-based UGAs are connected to the real world distribution network with different phases (two phases with the same three-phase node in which the phase difference is 120°). As shown in Fig. 12, again, the two DFT-based UGAs have the same phase angle trend and the angle difference is within ±0.0038°. Since the angle difference standard deviations of the two tests are both within 0.0029°, corresponding to 0.134 $\mu$s time error, which verifies the accuracy of UGA for measurement of practical distribution power grid

**Table 2** Requirements for the four PMU algorithms

| Algorithm name | Sampling rate, Hz | Reporting rate, Hz | Algorithm complexity |
|---|---|---|---|
| POW | 6000 | 6000 | very low |
| ZCA | 80k | 60 | low |
| DFT | 5760 | 60 | high |
| HSA | 1440 | 1440 | extreme low |

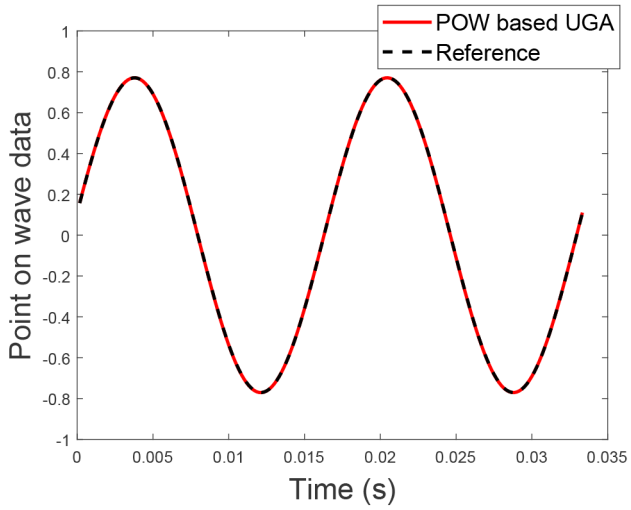


**Fig. 13** *POW data from the POW-based UGAs under steady-state test case*

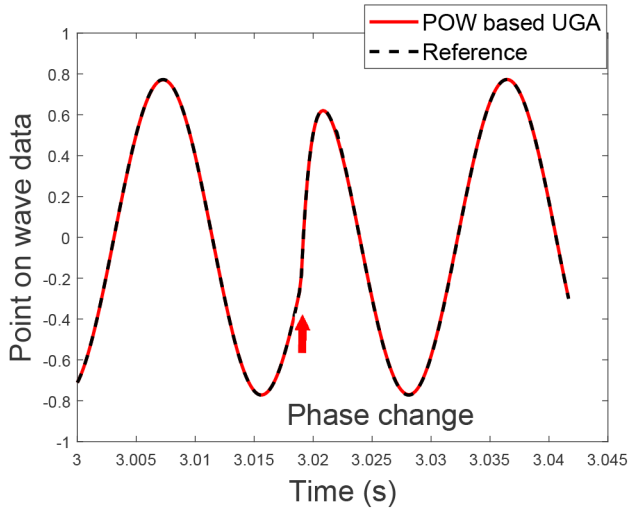


**Fig. 14** *POW data from the POW-based UGAs under phase step response test case*

As shown in Table 2, the sampling rate and reporting rate requirements for four PMU algorithms are summarised. It can be observed that each algorithm has totally different and specific requirements: (i) the POW algorithm has a very high requirement on the reporting rate; (ii) the ZCA has a high requirement on the sampling rate; (iii) the DFT algorithm has a high algorithm complexity, i.e. need large memory; (iv) the HSA has a high requirement on the reporting rate. Thus, to test all these algorithms, the open UGA platform has to be flexible with a high sampling rate and large memory. Based on the performance of the DSP board and ADC, it can be concluded that all four algorithms can be implemented in the Open-UGAs.

### *4.2 POW UGA test*

As shown in Figs. 13 and 14, the POW data for both the steady-state and phase step responses are compared with ideal reference signals. It can be observed that with a 6 kHz sampling rate, the

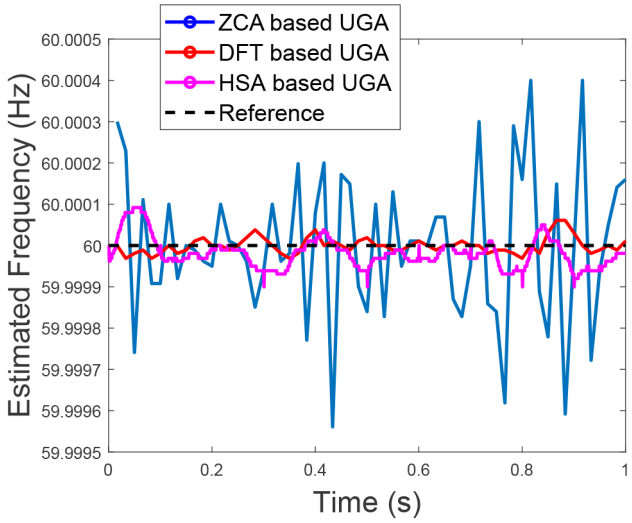


**Fig. 15** *Frequency response from the ZCA-, DFT-, and HSA-based UGAs under steady-state test case*

POW data can smoothly rebuild the real world 60 Hz signal. A comparison between the POW and the specification of the Omicron power source shows that the POW sampled by the POW-based UGA can match the total harmonics distortion (THD) given by the datasheet of the Omicron power source (the THD listed on the specification is 0.015% [30] while the THD detected by the POW-based UGA is 0.025%.).

In Fig. 14, a phase change occurs at 3 s from 0 to 90°. Since the steady-state on the POW is less significant than the phase step change, a phase step response is utilised for performance verification. Owing to the delay in the Omicron power source, the step change occurs at 3.018 s. Since the Omicron power source has a smooth change, there is no spike in the POW sampling while the waveform has an obvious phase change. Therefore, the performance of the POW-based UGA can be verified through these two tests. Note that the POW data has been normalised between $[-1\ 1]$. The raw data ranges from $[-32,767\ 32,768]$ with the 16-bit ADC.

### *4.3 Steady-state response test*

As shown in Fig. 15, 1 s frequency steady-state responses for ZCA-, DFT-, and HSA-based UGAs are given. It can be clearly observed that the frequency errors for all three UGAs are within 5 mHz, which is the frequency error requirement for the steady-state frequency error in IEEE C37.118.1. In addition, as shown in Fig. 16, it can be obviously shown that the HSA-based UGA has a much higher frequency resolution than other two UGAs with a zoomed-in view of the frequency measurement.

To have a quantitative comparison among three UGAs, the average frequency error (FE), average rate of change of RE (RFE), phase error (PE), total vector error (TVE), and magnitude error (ME), and the response time (utilised in the frequency step response tests) are utilised as criteria. As listed in Table 3, the FE for the ZCA-based UGA is the largest (i.e. $1.8091 \times 10^{-4}$ Hz), while the FEs for the DFT are close to the HSA-based UGAs (i.e. $2.1478 \times 10^{-5}$ Hz and $4.6034 \times 10^{-5}$ Hz). In addition, the results for the RFEs of all three UGAs are quite similar to the FEs, i.e. the RFE of the DFT-based UGA is close to that of the HSA-based UGA, while the RFE of the ZCA-based UGA is much larger than the other two UGAs. These results are reasonable because the DFT-based algorithms usually have a more steady frequency estimation results compared with ZCA-based ones. Note that both the FEs and RFEs for the DFT- and HSA-based UGAs satisfy the requirements listed in the IEEE C37.118.1, i.e. 5 mHz and 0.01 Hz/s [8], while the ZCA-based UGA can satisfy the requirement for the FE but it does not satisfy the requirement for the RFE. Since the POW- and ZCA-based UGAs did not have the phase and magnitude calculation algorithm deployed, only results for the DFT-based UGA is given. It can be observed that all three

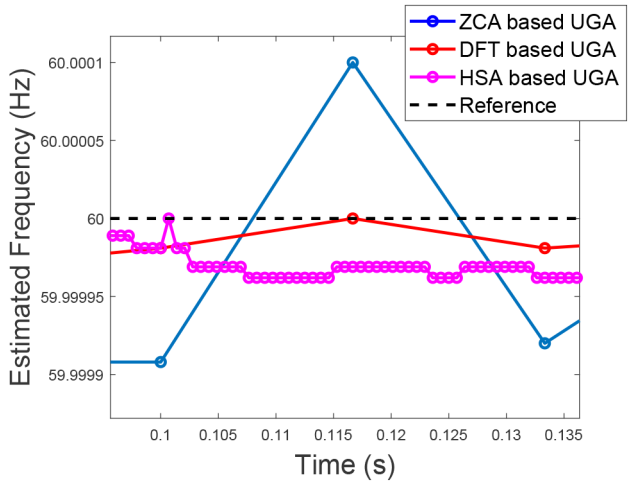


**Fig. 16** *Zoomed-in frequency response from the ZCA-, DFT-, and HSA-based UGAs under steady-state test case*

**Table 3** Comparison among ZCA-, DFT-, and HSA-based UGA

| Open-UGAs | FE, Hz | RFE, Hz/s | PE, deg | TVE, % | ME, V | Response time, s |
|---|---|---|---|---|---|---|
| POW-based UGA | $1.8091 \times 10^{-4}$ | 0.0188 | NAN | NAN | NAN | 0.0333 |
| DFT-based UGA | $2.1478 \times 10^{-5}$ | 0.0012 | 0.0029 | 0.0005 | 0.0042 | 0.1000 |
| HSA-based UGA | $4.6034 \times 10^{-5}$ | 0.0017 | NAN | NAN | NAN | 0.0931 |

parameters are far smaller than the requirements listed in the IEEE C37.118.1.

### *4.4 Frequency step response test*

As shown in Fig. 17, frequency step responses for ZCA-, DFT-, and HSA-based UGAs from 59 to 60 Hz and then to 61 Hz are given. It can be seen that all three UGAs can smoothly follow the frequency step response reference. To have a clear view of the step response, a zoomed-in view of the step change from 59 to 60 Hz at around 3 s is given. In addition, the frequency response times for three UGAs are also listed in Table 3. It can be observed that the ZCA has the shortest response time (0.0333 s). On the other hand, the response time for the HSA- and DFT-based UGAs are close to each other (0.0931 and 0.1000 s, respectively). Note that the response times for all three UGAs satisfy the response time requirement listed in the IEEE C37.118.1 (0.120 s) [8].

### *4.5 Compatibility discussion*

Since the compatibility of the synchrophasor estimation algorithms has been fully verified in Section 3 with four different algorithms, the compatibility of the proposed Open-UGA platform with existing distributional PMUs is discussed here. The DFT-based UGA and two other distributional PMUs, i.e. a $\mu$-PMU and a commercial PMU (Arbiter 1133A), are chosen in this compatibility test. In this test, the power signals for three PMUs are generated from the Omicron 256 plus while the data frames are received by the Open-UGA server. Since the data streaming protocols of all three PMUs are the same, i.e. IEEE C37.118.2 and their estimated synchrophasors are all GPS synchronised, the received data from these three PMUs are comparable.

As shown in Fig. 18, to verify the compatibility of the Open-UGA platform, a frequency steady-state test is given among three PMUs. It can be observed that the synchrophasors from three PMUs can be successfully received by the Open-UGA server

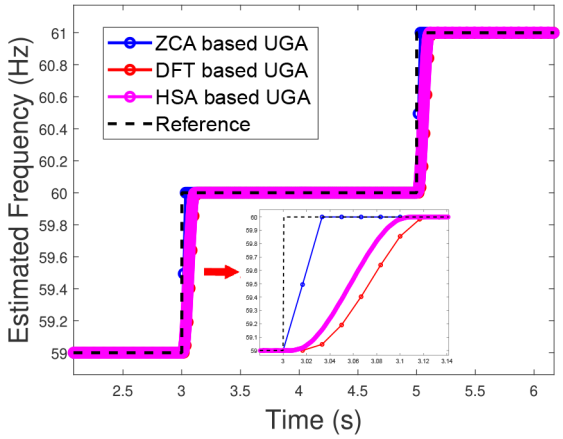


**Fig. 17** *Frequency response from the ZCA-, DFT-, and HSA-based UGAs under the step response test case*

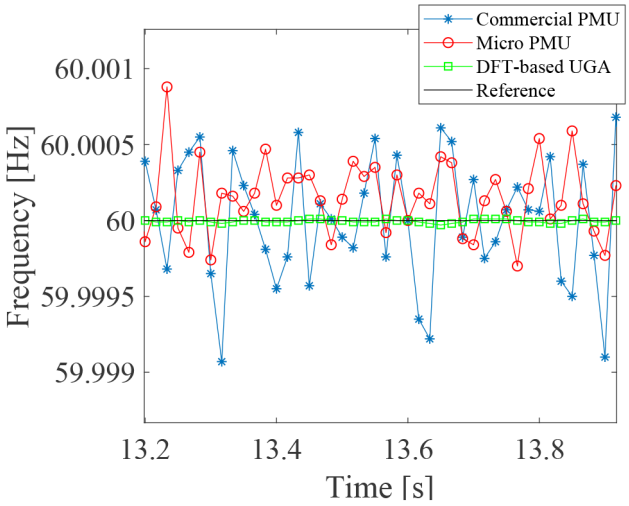


**Fig. 18** *Frequency response from the DFT-based UGA, μ-PMU, and commercial PMU under steady-state test case*

simultaneously. In addition, this result also shows that the DFT-based UGA has a lower frequency error compared with the other two PMUs while the frequency errors of all three PMUs are within the frequency error requirement listed in the IEEE C37.118.1, i.e. 5 mHz.

Since the first-order low-pass filter has a cut-off frequency as 600 Hz, there is a requirement for the algorithms to be implemented in the Open-UGA

$$\frac{f_s}{2} \geq 600, \tag{22}$$

where $f_s$ is the sampling rate of the implemented algorithm. If the implemented algorithm needs a low-sampling rate, it may need to design a digital filter in the algorithm to filter the aliased frequencies

### *4.6 Anti-aliasing filter discussion*

To deal with the aliasing issue on the sampling accuracy for the Open-UGAs with a low sampling rate, two anti-aliasing filters are implemented in the Open-UGAs, i.e. an EMI filter and a low pass filter. A real-world experiment has been done with two DFT-based UGAs. One of the UGAs is without the anti-aliasing filters. The test is a standard steady-state test with 60 Hz and 90°. As listed in Table 4, the frequency error of the Open-UGA is 3.11% less than that of the Open-UGA without anti-aliasing filters. In addition, the phase angle error of the Open-UGA is 1.11% less than that of the Open-UGA without anti-aliasing filters. With these results, it can be observed that the anti-aliasing filters on the Open-UGAs can cancel part of the aliasing effects.

**Table 4** Anti-aliasing test results

| | FE, Hz | PE, deg |
|---|---|---|
| Open-UGA | $1.5510 \times 10^{-5}$ | 0.0051 |
| Open-UGA without anti-aliasing filters | $1.5993 \times 10^{-5}$ | 0.0052 |

## 5 Conclusions

This study has discussed the designs and implementations of a low cost, flexible, and distribution level open UGA platform. First, the hardware, software, and server designs and architectures of the Open-UGAs are introduced with block diagrams, flowcharts, and a PCB photo. Then, to verify the flexibility of the Open-UGAs, four example implementations of the Open-UGAs are discussed with the algorithm requirements and software architectures. Finally, four Open-UGAs with different implemented algorithms are tested under the steady-state and the step response conditions. The experiment results are compared and discussed with both illustrative and quantitative analysis. From the analysis of the experiment result, it can be concluded that the Open-UGAs provide a flexible platform to implement and evaluate different distribution level synchrophasor estimation algorithms.

## 6 Acknowledgments

This study was partially authored by UT-Battelle, LLC under contract DE-AC05-00OR22725 with the US Department of Energy (DOE). The US government retains and the publisher, by accepting the article for publication, acknowledges that the US government retains a non-exclusive, paid-up, irrevocable, worldwide license to publish or reproduce the published form of this manuscript or allow others to do so, for US government purposes. DOE will provide public access to these results of federally sponsored research in accordance with the DOE Public Access Plan(http://energy.gov/downloads/doe-public-access-plan).This work also made use of Engineering Research Center shared facilities supported by the Engineering Research Center Program of the National Science Foundation (NSF) and the Department of Energy under NSF Award Number EEC-1041877 and the CURENT Industry Partnership Program.

## 7 References

[1] Phadke, A.G.: 'Synchronized phasor measurements in power systems', *IEEE Comput. Appl. Power*, 1993, **6**, (2), pp. 10–15

[2] Bashian, A., Assili, M., Anvari Moghaddam, A., *et al.*: 'Co-optimal PMU and communication system placement using hybrid wireless sensors', *Sustain. Energy Grids Netw.*, 2019, **19**, p. 100238

[3] Bashian, A., Assili, M., Anvari Moghaddam, A., *et al.*: 'Optimal design of a wide area measurement system using hybrid wireless sensors and phasor measurement units', *Electronics*, 2019, **8**, (10), p. 1085

[4] Liu, Y., Zhan, L., Zhang, Y., *et al.*: 'Wide-area-measurement system development at the distribution level: an FNET/GridEye example', *IEEE Trans. Power Deliv.*, 2015, **31**, (2), pp. 721–731

[5] Yin, H., Yu, W., Bhandari, A., *et al.*: 'Advanced universal grid analyzer development and implementation'. 2019 Int. Conf. on Smart Grid Synchronized Measurements and Analytics (SGSMA), College Station, Texas, USA., 2019, pp. 1–5

[6] Pinte, B., Quinlan, M., Reinhard, K.: 'Low voltage micro-phasor measurement unit ($\mu$PMU)'. 2015 IEEE Power and Energy Conf. at Illinois (PECI), Champaign, IL, USA., 2015, pp. 1–4

[7] Pinte, B., Quinlan, M., Yoon, A., *et al.*: 'A one-phase, distribution-level phasor measurement unit for post-event analysis'. 2014 Power and Energy Conf. at Illinois (PECI), Champaign, IL, USA., 2014, pp. 1–7

[8] 'IEEE Std C37. 118: 'IEEE standard for synchrophasor measurements for power systems'. IEEE Std C371181-2011 (Revision of IEEE Std C37118-2005), 2011, pp. 1–61

[9] 'IEC/IEEE 60255-118: 'IEEE/IEC international standard – measuring relays and protection equipment – part 118-1: Synchrophasor for power systems – measurements', IEC/IEEE 60255-118-1:2018, 2018, pp. 1–78

[10] Angioni, A., Lipari, G., Pau, M., *et al.*: 'A low cost PMU to monitor distribution grids'. 2017 IEEE Int. Workshop on Applied Measurements for Power Systems (AMPS), Liverpool, UK., 2017, pp. 1–6

[11] Zhao, J.: 'Performance improvement of wide-area-monitoring-system (WAMS) and applications development'. PhD Electrical Engineering and Computer Science, The University of Tennessee, Knoxville, Knoxville, TN, 2018

[12] Macii, D., Petri, D., Zorat, A.: 'Accuracy analysis and enhancement of DFT-based synchrophasor estimators in off-nominal conditions', *IEEE Trans. Instrum. Meas.*, 2012, **61**, (10), pp. 2653–2664

[13] Xia, T., Liu, Y.: 'Single-phase phase angle measurements in electric power systems', *IEEE Trans. Power Syst.*, 2009, **25**, (2), pp. 844–852

[14] Kamwa, I., Pradhan, A.K., Joos, G.: 'Adaptive phasor and frequency-tracking schemes for wide-area protection and control', *IEEE Trans. Power Deliv.*, 2010, **26**, (2), pp. 744–753

[15] Premerlani, W., Kasztenny, B., Adamiak, M.: 'Development and implementation of a synchrophasor estimator capable of measurements under dynamic conditions', *IEEE Trans. Power Deliv.*, 2007, **23**, (1), pp. 109–123

[16] Platas Garza, M.A., Platas Garza, J., de la Serna, O.J.A.: 'Dynamic phasor and frequency estimates through maximally flat differentiators', *IEEE Trans. Instrum. Meas.*, 2009, **59**, (7), pp. 1803–1811

[17] Zhan, L., Liu, Y.: 'Improved WLS-TF algorithm for dynamic synchronized angle and frequency estimation'. 2014 IEEE PES General Meeting Conf. & Exposition, National Harbor, MD, USA., 2014, pp. 1–5

[18] 'IEEE recommended practice and requirements for harmonic control in electric power systems', IEEE Std 519-2014 (Revision of IEEE Std 519-1992), 2014, pp. 1–29

[19] 'Open PMU labview project'. Available at http://www.ni.com/product-documentation/52975/en/

[20] Laverty, D.M., Best, R.J., Brogan, P., *et al.*: 'The OpenPMU platform for open-source phasor measurements', *IEEE Trans. Instrum. Meas.*, 2013, **62**, (4), pp. 701–709

[21] Yao, W., Zhan, L., Liu, Y., *et al.*: 'A novel method for phasor measurement unit sampling time error compensation', *IEEE Trans. Smart Grid*, 2016, **9**, (2), pp. 1063–1072

[22] Wang, W., Yin, H., Chen, C., *et al.*: 'Frequency disturbance event detection based on synchrophasors and deep learning', *IEEE Trans. Smart Grid*, 2020, p. 1

[23] Wang, W., Yao, W., Chen, C., *et al.*: 'Fast and accurate frequency response estimation for large power system disturbances using second derivative of frequency data', *IEEE Trans. Power Syst.*, 2020, **35**, pp. 2483–2486

[24] 'Public FNET website'. Available at http://fnetpublic.utk.edu/index.html

[25] Yao, W., Zhao, J., Liu, Y., *et al.*, , *et al.*: 'Synchrophasor measurement method for power systems'. Google Patents, 2018, US Patent App. 15/609,484

[26] Chen, J.: '*Accurate frequency estimation with phasor angles*' (Virginia Tech, USA., 1994)

[27] Zhan, L., Zhao, J., Culliss, J., *et al.*: 'Universal grid analyzer design and development'. 2015 Power & Energy Society General Meeting, Denver, CO, USA., 2015, pp. 1–5

[28] 'A new high-speed and high accuracy measurement method for power grid'. Available at https://www.ornl.gov/technology/201904450

[29] Zhan, L., Xiao, B., Li, F., *et al.*: 'A fault-tolerant grid frequency measurement algorithm during transients', *IET Energy Systems Integration*, 2020, doi: 10.1049/iet-esi.2019.0126

[30] 'The reference manual of CMC 256'. Available at https://www.omicronenergy.com/en/products/cmc-256plus/