

DC-Saturated Continuously Variable Series Reactors (CVSRs) for Power Flow Control in Power Transmission Systems

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Abstract – This paper proposes a novel continuously variable series reactor (CVSR) based on a dc current controller (DCC) to manage power flow in transmission systems. There are threefold major contributions. First, the three-dimensional electromagnetic interaction has been comprehensively analyzed to extend the understanding beyond the conventional 2D relationship. Second, a high-fidelity reluctance model of the CVSR with an improved DCC model is proposed and implemented. To overcome the fundamental concern for the system modeling, the DCC has been modeled as an ideal current source in parallel with an output impedance. The induced back-EMF can be precisely projected which provides critical design guidelines for the DCC. Third, inspired by the theoretical analysis and modeling, a reliable high power DCC converter is designed accordingly to interface with kV-level back-EMF and supply kA-level dc current for a 115 kV / 1500 A CVSR. Experiments are conducted in a practical transmission demonstration system. When the ac current in the transmission system varies from zero to 1500 A, experimental results show that the proposed CVSR can continuously regulate the reactance from 1.6 Ω to 5 Ω , validating the effectiveness of the proposed system design and modeling methodology.

Index Terms—Continuously variable series reactors (CVSRs); variable inductor (VI); power flow control.

I. INTRODUCTION

Over recent decades, actively routing the power flow in the transmission system has been considered as a promising candidate to more fully utilize the existing large scale transmission networks. Active power flow control includes increasing the power flow on underutilized lines and limiting the power flow on congested lines [1]. Previously, mechanically controlled capacitors and reactors [2] are connected in series in the power system as means of regulating power flow. In addition, tap changers, phase shifters [3], [4], and variable frequency transformers [5]-[7] are cost-effective methods to control the power flow in transmission systems.

As an alternative method, power electronics-based series compensation, such as flexible AC transmission system (FACTS), is also a good solution, and it can realize the continuous control of terminal voltages, impedances, and phase angles in the transmission system [8]-[20]. In the last two decades, power electronics-based FACTS devices have been installed and operated in several locations worldwide to increase the power system reliability, but the relatively high cost of installation and operation prevents this type of technology from being widely deployed in the grid. Based on published literature, FACTS devices typically cost more than U.S.\$ 100 per kVAR [10]. The Custom Power Active Transformer (CPAT) proposed in [21], [22], is an emerging concept to multiplex subtransmission or distribution transformers with incorporating power electronics converters. However, the unbalanced flux distribution in three limbs, due

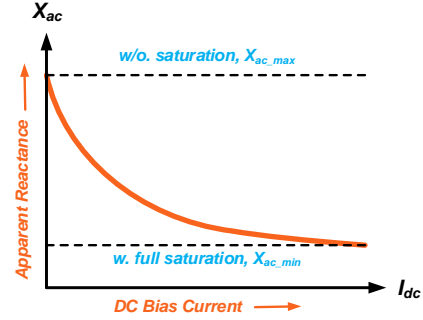


Fig. 1. Relationship between the apparent reactance and the DC bias current in the conventional low-power application of variable inductor (VI).

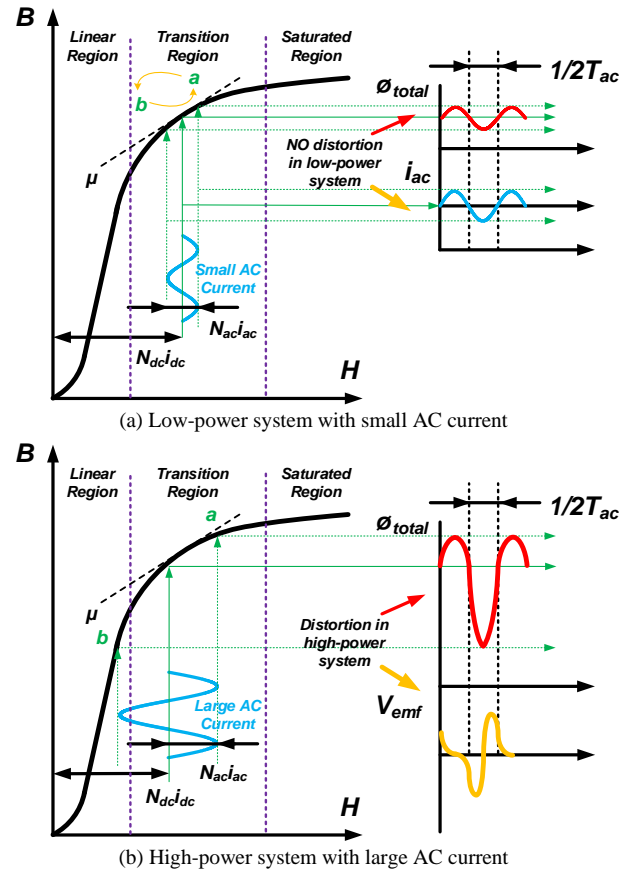


Fig. 2. Working range of B-H curve of the variable inductor (VI) for low- and high-power applications: high-power system back EMF has distortion.

to the asymmetrical winding arrangement, imposes additional cooling and mechanical design considerations on the top of conventional three phase transformer design. Consequently, the design and fabrication challenges have not been fully explored and verified through utility scale prototyping. In contrast, the continuously variable series reactor (CVSR) has been

implemented to vary the line reactance and control the power flow [23]-[25], as a cost-efficient series compensation technology. By directly exploiting the mature and sophisticated technologies of power transformer design, the cost of CVSR is estimated to be less than U.S.\$ 10 per kVAR based upon the established utility scale prototype. The ideal installation locations for CVSRs are located at subtransmissions or transmission network having AC constraints and a series of $N - 1$ contingencies. The optimal placement and scenario analysis can be found in [26], [27].

Basically, a CVSR is a magnetic-based device similar to a variable inductor (VI) [28]-[31], which has been proposed and employed in low-voltage applications, including the dimming of fluorescent lamps, LED drivers, and power factor correction circuits. The apparent reactance of the AC winding of the inductor can be controlled by tuning the DC bias current flowing through the DC winding, as shown in Fig. 1. When the DC bias current is zero, the AC reactance reaches the maximum value; while the DC bias current is large enough to saturate the magnetic core, the AC reactance drops dramatically. Fig. 2 shows the B-H curve of a VI, considering both the DC and AC currents. In Fig. 2(a), for a conventional VI in low-power applications, the magnitude of the AC current is relatively low and varies in a narrow region. The impact of AC current on the VI reactance is very limited and can be ignored. As a result, the apparent reactance is determined by the DC bias current as shown in Fig. 1. The induced back-EMF at DC winding is also not significant, which greatly relieve the DCC design difficulty.

However, for a high-power VI in Fig. 2(b), such as the CVSRs in the high-power utility application [32], [33], the operation principle is totally different. The AC current can be as high as thousands of amperes and continuously swings in a broad region. Due to the saturation of the magnetic core, the induced back-EMF voltage cannot be neglected, as displayed in Fig. 2(b). The impact of the AC current on both the reactance of the AC winding and the design of DCC have not been explored in previous research studies. The widely varying AC current offsets the reactance and makes the simplified model in Fig. 1 insufficient to predict the system's electromagnetic behavior. In previous literature [34], the authors utilized a gyrator-capacitor (G-C) approach to model this complicated magnetic-electric interaction. However, the DCC was only modeled as a constant current source which is not a valid assumption in most CVSR operation conditions. Therefore, this paper will address all these design and modeling concerns how to properly design and model the DCC considering all CVSR operation conditions, then the characteristic of a high-power CVSR and propose an effective method to regulate the reactance for high-power applications, so far lacking in the scientific literature.

Therefore, this paper will address these aforementioned fundamental issues and propose novel system design and modeling methodology in threefold, as an extension of reference [32], [33]. First, the three-dimensional electromagnetic interaction mechanism determined by both AC and DC windings of a CVSR has been comprehensively analyzed to extend the understanding beyond the conventional 2D relationship. Second, a high-fidelity equivalent

based model of the CVSR with an improved DCC model is proposed and implemented. To overcome the fundamental concern for the system modeling, the DCC has been modeled as an ideal current source in parallel with an output impedance. With the proposed system modeling methodology, the induced back-EMF can be precisely projected which provides critical design guideline for the DCC. Third, inspired by the theoretical analysis and modeling, a reliable high power DCC converter is designed accordingly to interface with kV-level back-EMF and supply kA-level dc current for a 115 kV / 1500 A CVSR. The experimental results validate the feasibility and effectiveness of the proposed system design and modeling methodology.

The content of this paper is organized as follows: The

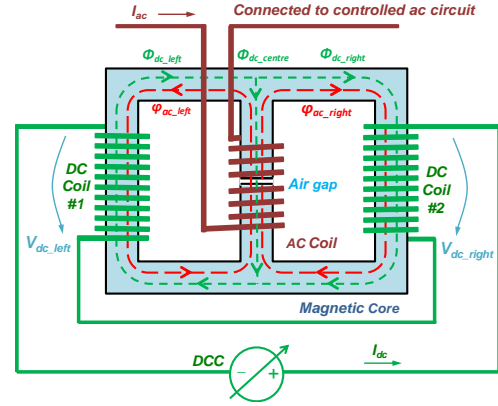
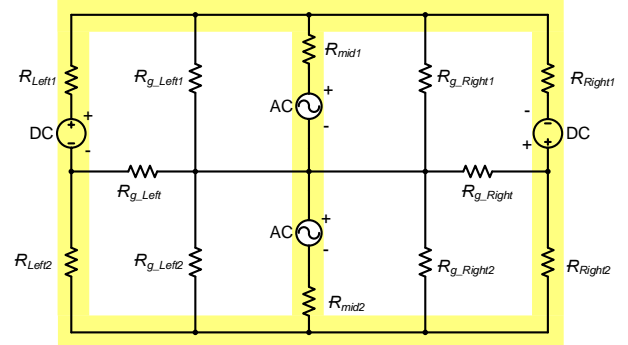
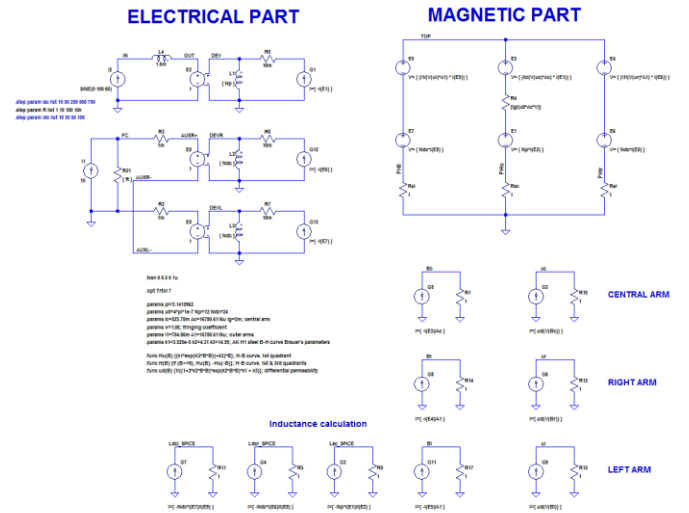


Fig. 3. Structure of a DCC-enabled CVSR to regulate the AC reactance.



(a) Equivalent reluctance-based model of the DCC-enabled CVSR.



(b) System modeling implementation in LTspice environment

Fig. 4. The proposed high-fidelity system modeling with CVSR and DCC.

comprehensive three-dimensional electromagnetic interaction mechanism and the proposed high-fidelity systematic modeling approach are illustrated in Section II. The DCC design procedure is then presented in detail in Section III. The influence of the proposed feedforward assisted double-loop controller on the interaction between DCC and the CVSR dc winding has been explicitly investigated in Section IV. Then, A full-power prototype with the developed feedforward assisted double-loop controller is implemented and tested at different

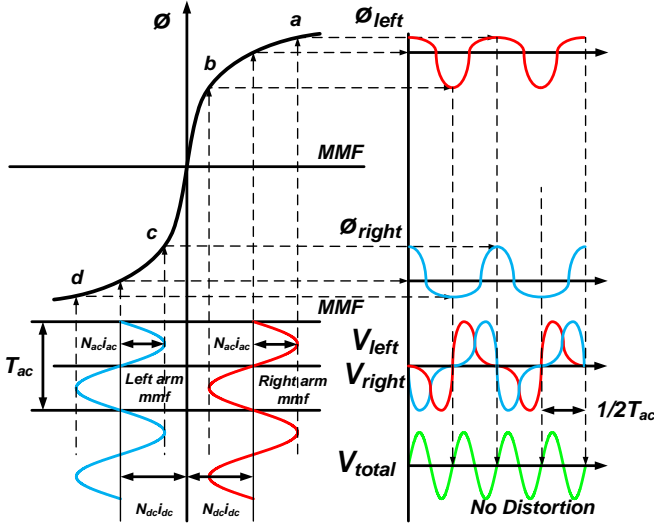


Fig. 5. Working principle of the B-H curve of the proposed DCC-enabled CVSR to eliminate the back EMF distortion.

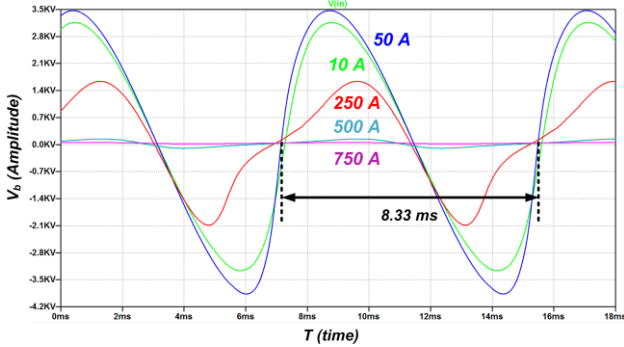


Fig. 6. The simulation results of induced back-EMF voltage under different DC bias currents when the AC current is set at 500 Arms.

conditions, which eventually demonstrates the continuous ac reactance regulation performance of CVSR-DCC system.

II. ELECTROMAGNETIC INTERFACE BETWEEN DCC AND CVSR

A. System Description

The structure of a DCC-enabled CVSR is shown in Fig. 3. For the three-leg magnetic core, the AC coil is wound on the middle leg, and two DC coils are placed symmetrically on the outer legs. The two dc coils are series-connected in opposite polarity to form the dc winding as the controlling element. The magnetomotive force (MMF) generated by the AC and DC windings has the same polarity in one leg and opposite polarity in the other leg.

The equivalent reluctance-based model of the CVSR is shown in Fig. 4 (a). The voltage sources represent the AC and

DC MMF, respectively. The reluctances of the magnetic core are split into six pieces: R_{left1} , R_{left2} , R_{right1} , R_{right2} , R_{mid1} , R_{mid2} . Also, the reluctances of air gaps are also shown in Fig. 4 (a). It should be noted that, since the magnetic core can be fully saturated by the DC bias current, the core reluctances could be comparable to the air gap reluctances. Thus, an air gap has also been created intentionally to introduce a much larger reluctance dominated by the air gap on the middle leg compared to that of outer legs. There are two main consequences:

- 1) The ac flux is much smaller than the dc flux and have less impact on the permeability variation in the outer legs;
- 2) Most of the dc bias flux only circulates in the outer legs of the core, especially when the core is not fully saturated.

Besides, the DCC has been modeled as an ideal current source in parallel with an output impedance to address the fundamental concern of the DCC modeling mentioned in the introduction. The model implementation of the whole system, including both the DCC and CVSR, in LTspice environment is given in Figure 4 (b). According to the proposed reluctance and DCC modeling methodology, the working principle of the B-H curve of the proposed CVSR is shown in Fig. 5. It is worth mentioning that the actual operation conditions could be much more complicated than the showcase in Fig. 5 because of the introduction of the DCC output impedance. How to accurately estimate the output impedance will be covered in Section IV. The instantaneous permeability on the outer legs is asymmetrical, so the magnitude of fluxes (ϕ_{ac_left} , ϕ_{ac_right}) and their changing rates ($\partial\phi_{ac_left}/dt$, $\partial\phi_{ac_right}/dt$) are different. The induced voltages (V_{dc_left} , V_{dc_right}) on two DC coils and the total voltage V_{total} are also presented. Comparing Fig. 2(b), it clearly shows that the proposed winding structure can significantly mitigate the distortions in the induced back EMF voltage.

Based on the proposed CVSR structure in Fig. 3, the circuit model in Fig. 4, and the system parameters and dimensions in section V, the magnitude of the induced back-EMF is simulated as shown in Fig. 6. In the simulation, the AC current is set at 500 Arms as an example. The DC bias current varies in a wide range to estimate its impact on the back-EMF voltage. The waveforms validate the analysis in Fig. 5 that the back EMF voltage distortions are reduced.

When the DC bias current is low (50 A), the EMF magnitude is relatively high, reaching 3.5 kV. The magnitude maintains on the order of kV when the DC current is within 250 A. When the DC current is higher than 500 A, the induced back-EMF is very low, meaning the magnetic core is saturated. In this way, the impedance of the AC winding is regulated by the DC bias current. Meanwhile, Fig. 6 also shows that the kV level back-EMF voltage should be considered in the design and implementation of the DCC circuit in the next section.

III. DCC CONVERTER TOPOLOGY DESIGN

According to the proposed CVSR topology in Fig. 3, DCC is a critical component to tune the DC bias current and the AC winding inductance. The DCC design includes two aspects: the hardware circuit topology and the software control algorithm. This section focuses on the circuit topology design and analysis, and the corresponding control algorithm will be presented in the next section.

A. System Topology and Configuration

The proposed CVSR system topology and configuration is

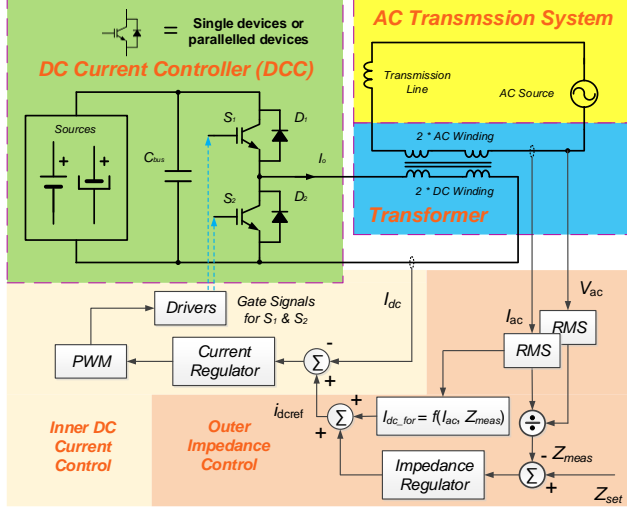


Fig. 7. Proposed topology and configuration of the proposed CVSR system.

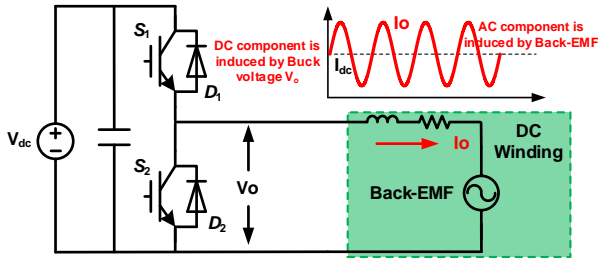


Fig. 8. Equivalent circuit of DCC to generate DC current.

Table I. Specifications and parameters of the proposed DCC

| | | | |
|--------------------------|---------------|--------------------------------|--------|
| DC link voltage V_{dc} | 280 V | Maximum output current I_O | 1000 A |
| DC winding resistance | 62 m Ω | Maximum output power P_{out} | 62 kW |
| DC winding inductance | 2.2 mH | Maximum efficiency f_{sw} | 98% |
| Switching frequency | 1200 Hz | Maximum temperature | 75 °C |
| Back-EMF frequency | 120 Hz | Maximum duty ratio | 0.221 |

shown in Fig. 7, including four subsystems: the DCC circuit, the DC and AC coupling transformer (CVSR), the AC transmission system, and the control system.

The basic function of DCC is to convert three-phase ac voltage to a regulated dc current. Several topologies are capable of being selected as a candidate for the DCC to meet the specifications shown in Table. I. One-stage three-phase ac-dc buck rectifier (e.g. thyristor phase-controlled rectifier) is first considered, due to its simplicity and reliable performance. However, this one-stage rectifier has two obvious drawbacks: not being able to provide bidirectional current to achieve required maximum reactance, and also high losses. Two-stage topologies equipped with various types of dc-dc converter are alternative solutions. At the source side, the DC voltage can be acquired from an AC voltage and a rectifier. A half-bridge-based synchronous buck converter is then selected to realize the DCC function. The synchronous buck converter output current includes two components.

1) The DC component of the output current is determined by the switching of the main switch S_1 , and the DC winding resistance.

2) The AC component of the output current is determined by the induced back-EMF from the AC winding as shown in Figs.

5 and 6, and the DC winding inductance.

During the normal working process, the switch S_1 and S_2 are driven by a pair of complimentary PWM signals to generate the DC voltage and current. When S_1 turns on, the source voltage is applied on the DC winding. When S_1 turns off, the DC current circulates through the free-wheeling diode D_2 or the switch S_2 .

There are three advantages to utilize the synchronous buck converter to realize the DCC function in this utility application.

1) Simplicity and low cost: the circuit only contains two main switches to adjust the DC output voltage and current.

2) High reliability: In the normal operation, the freewheeling diode D_2 and the switch S_2 can allow the ac component of the output current flowing in both directions and isolate the input source from the high back-EMF voltage. Under a fault condition, the switch S_2 can prevent the DC current from flowing into the DC link capacitor C_{bus} through the anti-parallel diode D_1 , and overcharge it to a damageable high voltage.

3) Low loss profile and natural convection cooling: the output dc current requirement of the DCC is so high that the total losses generated by the DCC have to be minimized. The utilization of the synchronous buck converter can significantly reduce the power device count and increase the total efficiency to ensure its low loss profile. This system benefit enables the employment of natural convection cooling system instead of forced air cooling, as it is preferred in utility application to drive down the maintenance requirement, improve device reliability and system resilience.

The equivalent circuit of the synchronous buck-based DCC is shown in Fig. 8. In a practical application, the back-EMF voltage is usually in the range of kV, as shown in Fig. 6. The input DC source voltage is in the range of 100s Volts, because the DC winding resistance is usually small. Through the PWM control of the converter, the output voltage V_o is much lower than the back-EMF. Therefore, the converter is not used to counteract the back-EMF. Instead, it is primarily used to generate a DC current and then protect the low-side DC voltage from being affected by the high-side back-EMF voltage.

B. DCC Circuit Design Example

In this section, according to the practical requirement, a 62 kW / 1000 A synchronous buck converter is designed as the DCC circuit for a 115 kV / 1500 A CVSR. The specifications and parameters of the DCC are shown in Table I.

In the transmission system, the CVSR requires a variable reactance in a wide range from 2 Ω and 5 Ω to regulate the power flow. Then, the DCC circuit should provide a DC bias current from 0 A to 1000 A. Based on the magnetic structure design in Fig. 3, the DC winding resistance is 62 m Ω , and the inductance is 2.2 mH. It can be estimated that the maximum output power of the proposed converter could reach 62 kW, which is challenging to achieve in practical implementation. The efficiency should be maintained at >98% to reduce the power loss and the temperature rise of the converter, especially when natural convection is mandatory for most utility applications. Since the back-EMF frequency is primarily at 120 Hz, the switching frequency of the converter is 1200 Hz in order to reduce the switching loss. The 1200 V / 2500 A IGBT module (CM2500DY-24S) is utilized in this design, which is very reliable and can be paralleled for high-power applications.

IV. DCC CONTROL ALGORITHM DESIGN

The DCC circuit hardware topology has been presented, and this section focuses on the modeling and control algorithm design for DCC circuit.

A. Modeling of the Proposed DCC Circuit

Based on the proposed DCC circuit topology in Fig. 8, the equivalent circuit model is shown in Fig. 9. It mainly includes two parts: the converter and the DC winding, which are explained as follows.

For the converter, its major function is to generate a DC current, so it can be modeled using the Norton equivalent circuit as shown in Fig. 9. The current source $G_c i_{dc\text{ref}}$ is used as the input, and the impedance Z_{dcc} is the equivalent impedance corresponding to the DCC dynamics, which will be presented in the controller design. It needs to be noted that the input current mainly contains a DC component, dominating the DC current i_{dc} flowing through the DC winding. The controller design is used to optimize the parameters G_c and Z_{dcc} .

For the DC winding, it is modeled as three components: resistance R , inductance L , and back-EMF. It should be noticed that R and L are nonlinear parameters related to the operating condition, and back-EMF is determined by both the AC-side and DC-side currents. For example, in the practical DC winding manufactured in this design, R is 50 mΩ at 20 °C, but it increases to 62 mΩ at the high-power condition when the temperature is 80 °C. Since the magnetic core is saturable, the inductance L also varies between 1.2mH and 2.2 mH at different power levels. In addition, the simulation results in Fig. 6 have shown that the back-EMF voltage changes from a small

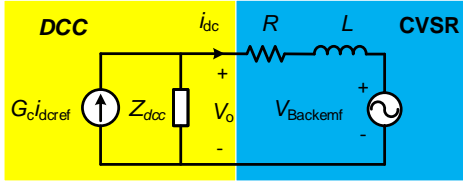


Fig. 9. Equivalent modeling of the proposed DCC circuit.

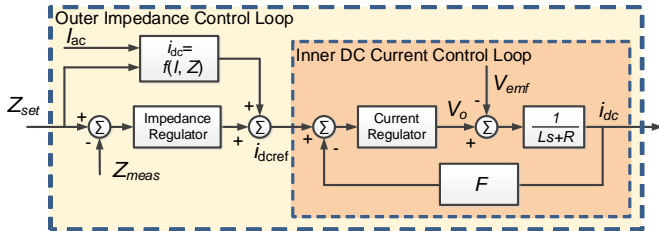


Fig. 10. Double-loop control structure for the proposed DCC circuit.

value to a few kV. Therefore, it shows that a controller design is necessitated to regulate the DC current of the DCC circuit.

B. Feedforward Assisted Double-Loop Control Structure

According to the proposed CVSR system structure in Fig. 7, a double-loop control structure is presented in Fig. 10, which includes the outer impedance control loop and the inner current control loop.

The outer impedance control loop is used to regulate the AC winding impedance and provide the reference current for the DC current. There is also a feedforward control unit to assist the impedance regulator and accelerate the control process. In the design process, the relationship between the AC current and the

impedance is tested in different conditions and saved in a look-up table in the controller. Then, the impedance controller only needs to deal with a relatively small error and the control sensitivity can be maintained.

The inner DC current control loop is used to directly regulate the DC winding current. In Fig. 10, the current regulator is the key component, and it is selected as a PI controller with the parameters K_p and K_i to simplify the design process. In this design, the parameter relationship is expressed in (1), where ω_c is the control bandwidth.

$$K = \frac{K_p}{L} = \frac{K_i}{R} = \frac{\omega_c}{V_{dc}} \quad (1)$$

According to Figs. 9 and 10, the equivalent impedance Z_{dcc} can be expressed as below.

$$Z_{dcc} = \frac{L \cdot s^2 + (R + V_{dc} \cdot K_p) \cdot s + V_{dc} \cdot K_i}{s} + (s \cdot L + R) \quad (2)$$

In the equivalent circuit model of Fig. 9, since the back-EMF voltage (a few kV) is much larger than the DC input voltage (280 V), the controller is not designed to follow the 120 Hz frequency. Therefore, the impedance Z_{dcc} only needs to respond to the DC current command, and its bandwidth is much lower than 120 Hz, which also contributes to reduce the switching frequency of the converter. For example, in this design, the PI controller is designed to achieve a frequency of 4.78 Hz. Then, according to the impedance analysis in Fig. 9, it shows that the input voltage is also coupled with 4.0% of the back-EMF, which is about 100 V / 120 Hz ripple in the worst case.

The advantage of this control structure is that a low-voltage synchronous buck converter is sufficient to regulate the DC current value to adjust the impedance in the power system. Also, the modeling and control analysis also indicates that the proposed method is robust to the L and R variation, and the real-time changing of circuit parameters can be compensated by the proposed controller. However, the disadvantage is that the control speed is at the same order of the power system dynamics, and it requires a few AC cycles to accomplish the control process.

V. PROTOTYPE DESIGN AND EXPERIMENTAL VALIDATION

A. Critical Components Selection

In the 62 kW converter design, the critical components include the semiconductor devices (IGBT transistors) and the DC link capacitor. Based on voltage and current ratings, two IGBTs are selected: CM1400DUC-24S and CM2500DY-24S. Moreover, the devices can be parallel connected to further reduce the power loss. Then, the power loss comparison of three IGBT configurations is shown in Fig. 11.

Fig. 11 compares the switching loss, the IGBT main body conduction loss, and the anti-parallel diode conduction loss. According to the parameters in Table I, the duty ratio of the converter is relatively low, meaning the anti-parallel diode conducts current during most of the time, so the diode loss dominates as shown in Fig. 11. Then, it is helpful to connect multiple devices in parallel to reduce the conduction loss. According to Fig. 11, by utilizing two CM2500DY-24S in parallel, the total power loss in the semiconductor devices is reduced by 15.3%.

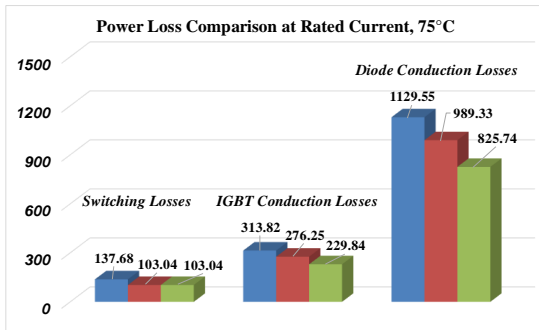


Fig. 11. Loss comparison between CM1400DUC-24S, CM2500DY-24S and paralleled CM2500DY-24S at the operating conditions listed in Table I.

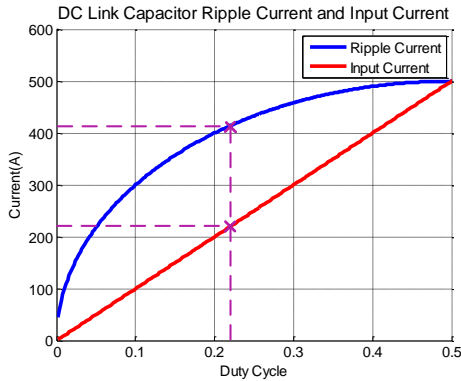


Fig. 12. The relationship between duty cycle and dc link capacitor ripple current and input current.

In addition, the thermal resistance is also an important parameter in evaluating the device performance. For example, the junction to case thermal resistance of CM2500DY-24S is $13^{\circ}\text{C}/\text{kW}$, but the value is $16^{\circ}\text{C}/\text{kW}$ for CM1400DUC-24S. Therefore, the dual-connected CM2500DY-24S is selected in the system implementation.

The DC link capacitor is used to deal with the ripple current flowing in the DC bus. For the proposed 62 kW converter, the relationship between the duty cycle and the DC link current ripple is shown in Fig. 12.

In the DCC circuit, the converter is used to generate a current. Since the desired output current is fixed, when the duty ratio increases, the input voltage decreases and the input current increases. In this case, the input current ripple also increases, which can induce a ripple voltage on the DC bus. In this high-power application, the ripple could cause under- or over-voltage protection in the system.

In order to reduce the current ripple, the DC link capacitance should be increased. There is a tradeoff between the ripple voltage and the DC link capacitance, which can reduce the ripple without affecting the system power density. In this design, the duty ratio is selected to be 0.221, and the ripple current is ~ 420 A. Multiple $970\ \mu\text{F}/1000\ \text{V}$ film capacitors are connected in parallel to handle the ripple current.

B. 115 kV / 1500 A CVSR Prototype Implementation

According to the design and simulation, an experimental prototype of 115 kV / 1500 A single-phase CVSR was implemented as shown in Fig. 13. In addition, the specifications and parameters of the designed 115 kV / 1500 A CVSR prototype is give in Table. II from electrical, mechanical, and magnetic perspectives. The ac winding is directly connected to

the transmission system. The dc winding is connected to the DCC circuit as illustrated in Fig. 14. The DCC contains a 62 kW synchronous buck converter, and it can supply a DC current up to 1000 A for the dc winding excitation.

Table II. Specifications and parameters of the designed 115 kV / 1500 A CVSR prototype

| Electrical Parameters | | | |
|--------------------------|---------------------|--------------------------|---------------------|
| Rated ac winding voltage | 115 kV | Rated dc winding voltage | 480 V |
| DC winding rated current | 1500 A | DC winding rated current | 1000 A |
| Magnetic Core Parameters | | | |
| Core shape | 3-leg | Core material | AK H1 steel |
| Middle leg net area | 394 in ² | Yoke net area | 192 in ² |
| External leg net area | 192 in ² | Window height | 65.3 in |
| Window width | 17.8 in | Air gap | 5.3 in total |
| Mechanical Parameters | | | |
| Length | 106 in | Width | 96 in |
| Height | 147 in | | |

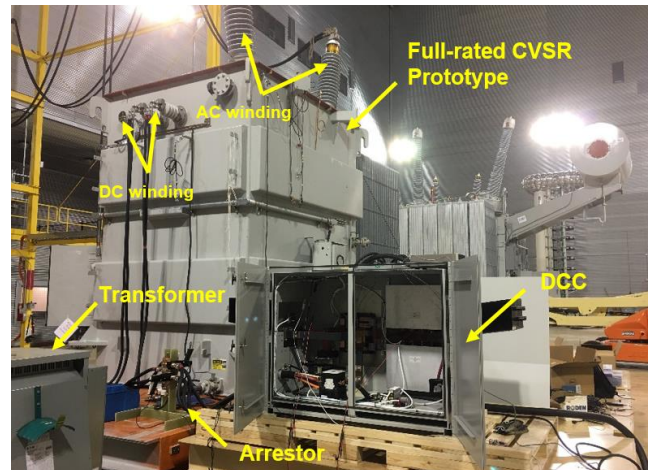


Fig. 13. Prototype of 115kV/1500A CVSR with the DCC in field-testing.

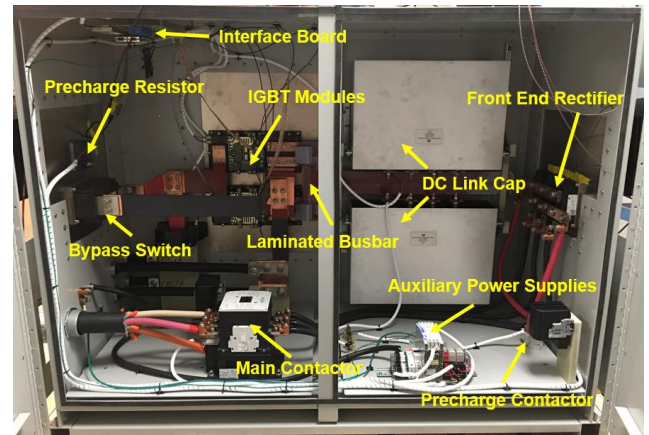
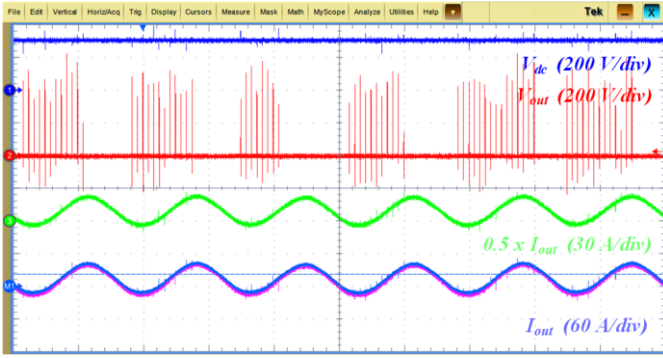


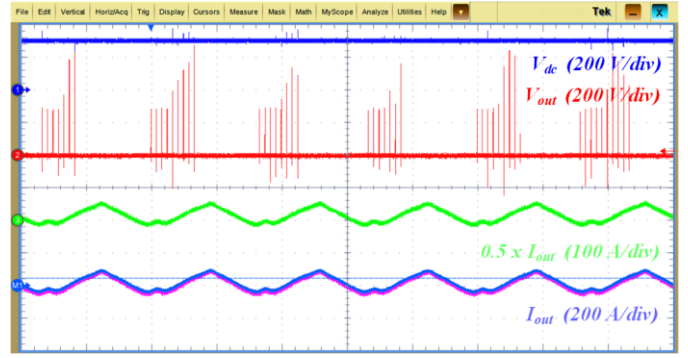
Fig. 14. Prototype DCC circuit based on a 62 kW converter, which can provide 0 – 1000 A DC current for the proposed CVSR.

C. Experimental Results of DCC Output Waveforms

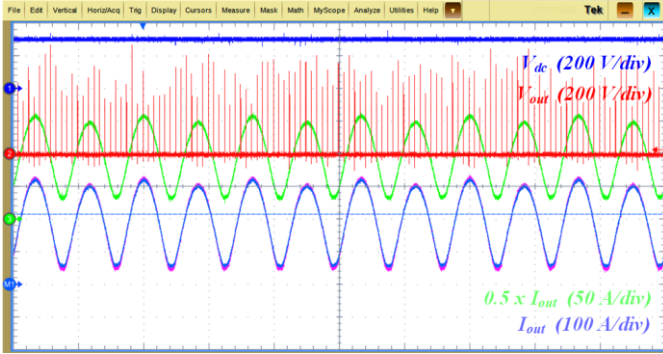
In the experiments, the converter is controlled by the PWM signal to adjust the DCC output current. In this way, the equivalent ac reactance of the CVSR is tuned. When the AC current in the transmission system is controlled at 500 A, the DC current reference is set to be 20 A, 200 A, and 1000 A, respectively. The experimental waveforms of the DCC output



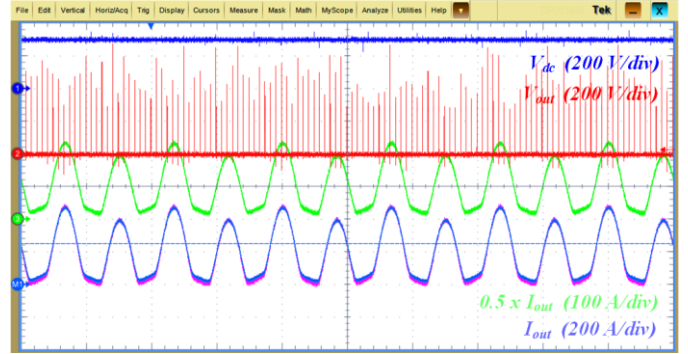
(a) DC current reference set at 20A



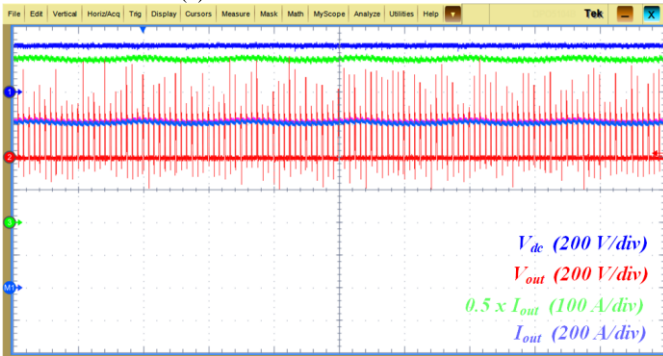
(a) DC current reference set at 200A



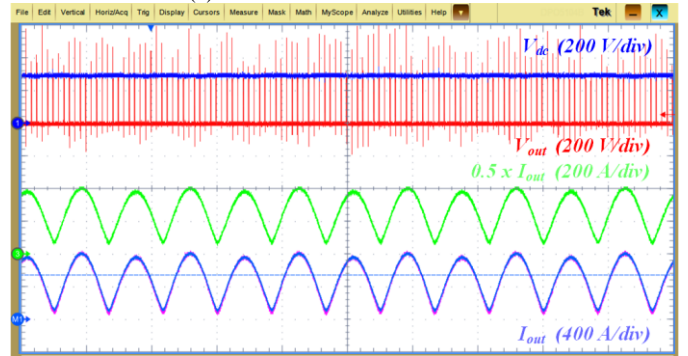
(b) DC current reference set at 1000A



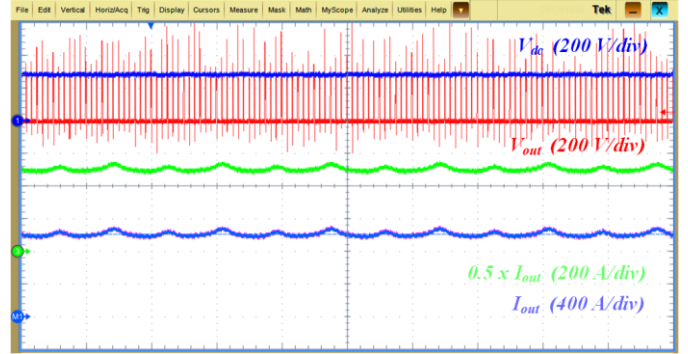
(b) DC current reference set at 200A



(c) DC current reference set at 1000A



(c) DC current reference set at 500A



(d) DC current reference set at 1000A

Fig. 15. Experimental waveforms of the DCC circuit when the ac current in the transmission system is set at 500 A with various dc current references.

voltage and current are shown in Fig. 15. It is worth mentioning that the utilized current probe is Tektronix TCP404XL whose current rating is only 750 A, smaller than the rated dc current. Thus, two cables are parallel connected at the DCC output terminal to share the dc current. Two current probes are clamped around these two cables respectively to measure half of the dc winding current, labeled as $0.5I_{out}$. The mathematical function in the oscilloscope is utilized to acquire the total dc winding current, displaying as I_{out} (the orange curve) in Fig. 15 and Fig. 16. Another two measurements are the dc-link voltage (V_{dc}) and DCC output voltage (V_{out}). In all the experimntal waveform, the time scale of the oscilloscope is consistently set at 10 ms per division.

In Fig. 15(a), the average dc current is measured as 23.72 A. Since the resistance of the dc winding is very small, the duty ratio of the converter is so small that it works in the burst mode. It shows that the dc output voltage is only effective for a short time period and the dc output current contains multiple pulses. In addition, the CVSR is still operating at linear region, no 120 Hz ac current component can be observed.

Fig. 15(b) shows the boundary case between the burst and

Fig. 16. Experimental waveforms of the DCC circuit when the ac current in the transmission system is set at 1500 A with various dc current references.

normal modes of operation of the converter, whose duty ratio is still very small. The average dc current is 213.2 A. The magnetic core is not saturated, although it is driven collectively by both the dc and ac currents to a status to maximize the back-EMF voltage. This back-EMF voltage is applied on the dc winding inductor as explained in Section III, resulting in a large ac current ripple (261 A) on the output current.

In Fig. 15(c), the average dc current is measured as 1009.1 A. Since the dc bias current is extremely large, the magnetic core

is fully saturated, and the back-EMF voltage from the ac winding to the dc winding is dramatically reduced. The induced output current ripple can be barely seen from the waveform.

Then, the ac current in the transmission system is increased to 1500 A. The dc current is also regulated from 0 A to 1000 A. The experimental waveforms associated with four dc current steps (20 A, 200 A, 500 A and 1000 A) are given in Fig. 16. Compared to Fig. 15, the current ripple is increased, primarily because the back-EMF voltage is boosted due to the 1500 A ac current.

Similar to Fig. 15(a), since the dc output current is very small, the converter works in the burst mode again. However, a

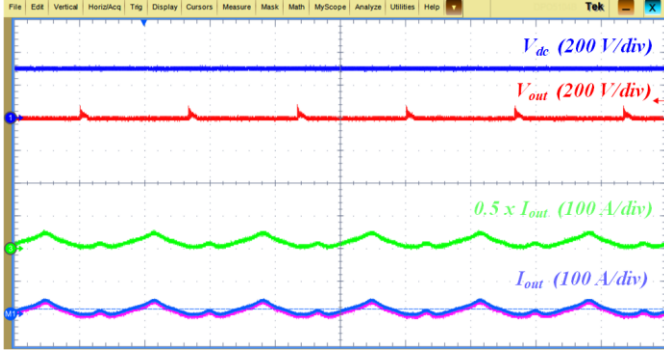


Fig. 17. Experimental waveform of the DCC circuit w/o. achieving zero DC current when the bottom IGBT S_2 turns off and AC current is set at 500 A.

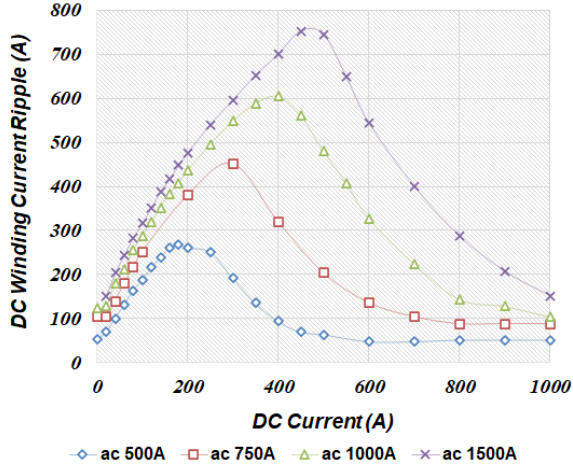


Fig. 18. Experimental results of the proposed DCC output current ripple at different AC and DC current conditions.

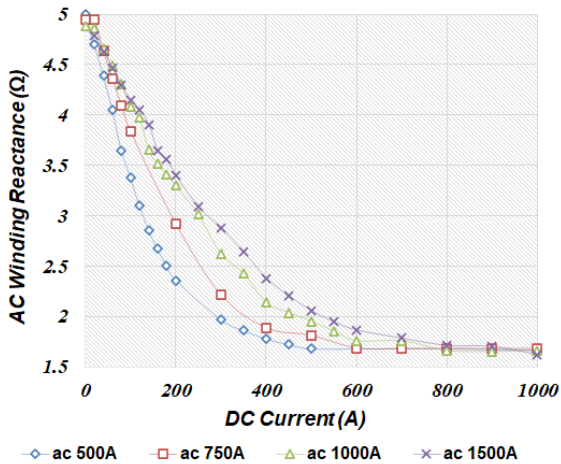


Fig. 19. Experimental results of the proposed CVSR ac winding reactance at different ac and dc current conditions.

significant difference is illustrated in Fig. 16 (a). By recalling Fig. 2(b), with only 20 A dc bias current but much greater ac current of 1500 A, the CVSR is operating between linear region and transition region, making the 120 Hz ac current component emerge. Then, the induced current ripple presents totally diverse waveform pattern.

Fig. 16(b) and (c) show two distinct high back-EMF scenarios, when the dc current is 200 A and 500 A respectively. Because of a much larger ac induced MMF, the corresponding current ripples are much more significant (436 A and 480 A). By zooming in the dc link voltage, only 30 V voltage ripple is observed in both cases, which verifies the effectiveness of the control algorithm proposed in Section IV. Fig. 16(d) also illustrates the influence of ac winding current, since a 120 Hz component can be clearly spotted even when the average dc current is 1007.5 A.

If the bottom IGBT S_2 does not turn on as proposed in Section III, it is impossible to control the converter to zero average current and achieve the desired maximum reactance. The corresponding experimental waveform is shown in Fig. 17. Without providing a bidirectional current path required by the back-emf induced current ripple, even the DC current reference is set to 0 A. The observed average current is still as high as 37.8 A, driving the ac reactance down to 4.5 Ω .

D. Experimental Results of Impedance Tuning by DCC

Based upon Figs. 15 - 17, further experiments are conducted at different ac and dc current conditions. The ac current varies from zero to 1500 A, while the dc current changes from zero to 1000 A, the measured output current ripple of the synchronous buck-based DCC is illustrated in Fig. 18. Then, two interesting phenomena can be summarized.

1) For a certain ac winding current, there exists a dc current value to maximize the dc current ripple. It is because dc current provides a flux bias to change the operation range of the magnetic core. When the magnetic core is not fully saturated within a cycle, there is a dc bias current that can maximize the back-EMF. However, when the dc bias current is high enough to fully saturate the core, the back-EMF is dramatically reduced.

2) For a certain dc current, the increase of the ac current value also means an increase of the dc current ripple. It is because the ac current can generate flux in two directions, which enlarges the operation range of the magnetic core and prevents the magnetic core from being fully saturated. When the core is not fully saturated, an increased ac current can increase the back-EMF. When the core is saturated by the dc current, the ac current can de-saturate the core from an opposite direction, and the back-EMF can also be observed.

The experimental results show that the proposed DCC circuit can adjust the dc current coupled with an ac ripple. The dc and ac windings work collectively through the magnetic structure of CVSR. Therefore, the ac winding reactance is measured at different ac and dc current conditions as shown in Fig. 19. The data in Fig. 19 is saved as a look-up table to realize the feedforward control in Fig. 10, which can improve the controller accuracy and dynamic performance.

Fig. 19 shows that the proposed DCC circuit can continually regulate the ac winding reactance through tuning the dc current. When the dc current is relatively low, the magnetic core is not

saturated and the reactance is relatively high. Once the dc current increases to the range of a few 100s of Ampere, the magnetic core is being saturated, and the reactance is reduced. However, a higher ac winding current usually exhibits a larger apparent reactance value. This experimental phenomena agree with the analysis disclosed in Section II. The experiments validate that the reactance can be tuned between 1.6Ω and 5Ω at various ac current profile (0 to 1500 A), which accounts for 68% reactance control range and satisfies the power flow control requirement in the transmission system.

E. Experimental Results of AC Current Harmonics

The proposed DCC as the control element for the CVSR is basically a power electronics converter who contains power-electronic components switching at high frequency (1.2 kHz). Another potential harmonics source is coming from the complicated electromagnetic interaction determined by both AC and DC windings of a CVSR. The primary concern to power engineers is the harmonic components introduced by these two factors to the power grid. During the field tests, among other data points that have already reported in the manuscript, the harmonic content and the total harmonic distortion (THD) of the phase current flowing through the ac winding of the CVSR have been monitored through dedicated Hall-effect current transducers. Due to the limited go-through hole size of the utilized Hall-effect current transducers, two cables are used to share the ac winding current. Thus, one CT only measures half of the ac winding current. Over the full operation range (DC: 0 A to 1000 A, AC: 0 A to 1500 A), the DCC and CVSR introduces negligible harmonic to the grid based upon intensive current measurements at different operating conditions. The maximum THD captured by the data acquisition system during the overall field test is less than 0.008 (0.8%), given that the background THD in the test facility is about 0.025. The worst case occurs when the ac current in the transmission system is around 1500 A and the dc current reference is set at 500 A. At this moment, the dc winding current has a significant ripple of 120 Hz, as shown in Fig. 16 (c). The corresponding experimental waveform is illustrated in Fig. 20. It is observed that the ac winding current does not exhibit any switching frequency component imposed by the DCC or 120

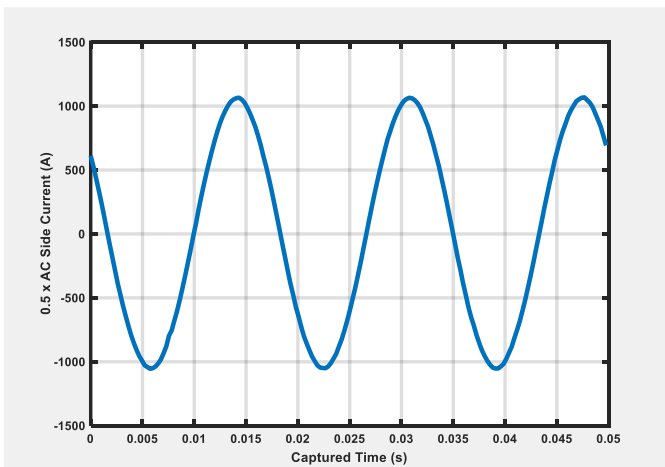


Fig. 20. Experimental results of the ac winding current when the ac current in the transmission system is set at 1500 A and the dc current reference set at 500 A.

Hz component caused by the complicated electromagnetic interaction as explained before.

VI. CONCLUSION

This paper intensively investigates the complicated electromagnetic interactions between the CVSR and the DCC. Considering the significant differences between the CVSR in utility applications and conventional VIs in low power application, the interaction mechanism has been further improved to extend the understanding beyond the conventional 2D relationship. An high-fidelity equivalent reluctance-based model of the CVSR with an improved DCC model has been proposed and developed to predict the CVSR's characteristics and provide technical insights for the DCC design. Based upon the theoretical analysis and modeling, a full-rated (62 kW) DCC converter with the proposed feedforward assisted double-loop controller is implemented and tested at various operating conditions. When the DC current varies from zero to 1000 A and the AC current varies from zero to 1500 A, the CVSR with the designed DCC can continuously regulate the AC reactance from 1.6Ω to 5Ω as desired. The experimental results validate the feasibility and effectiveness of the proposed system design and modeling methodology.

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