Experimental Evaluation of Capacitors for Power Buffering in Single-Phase Power Converters

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***Abstract*—Single-phase inverters and rectifiers require the use of an energy buffer to absorb twice-line-frequency power ripple. Historically, this challenge has been addressed by the use of large electrolytic capacitors. Lifetime constraints and the need for improved system performance have motivated designers to seek other capacitor technologies, such as ceramic and film, which are frequently used in conjunction with active filtering converters to reduce the capacitance required. Active filtering converters cycle the capacitor voltage over a wide voltage range while maintaining a constant dc bus voltage. This large-swing operation demands different capacitor qualities than most other filtering applications, and the data sheet parameters available for commercial capacitors may be ineffective or require special care for calculating characteristics, such as efficiency and energy storage capability. This work presents an experimental setup for evaluating capacitor performance under a large voltage swing along with detailed experimental results. Energy storage data for a number of capacitors in the 50–630 V range from several manufacturers are included. The approach and findings of this paper can serve as an aid to power electronics designers for the selection and evaluation of capacitors in energy buffering applications.**

***Index Terms*—DC-AC power converters, AC-DC power converters, inverters, power conditioning, photovoltaic systems, switched capacitor circuits, power capacitors.**

I. Introduction

CONVERSION between dc and ac electric power using inverters or power factor correction rectifiers, requires energy buffering to balance the instantaneous power difference between the two systems. Fig. 1 depicts the power imbalance between dc and ac energy transfer and the difference in energy which must be buffered over a full ac cycle. This challenge is often referred to as power pulsation decoupling or twice-line-frequency energy buffering in the literature and is present in all single-phase dc/ac and ac/dc converters [1], [2].

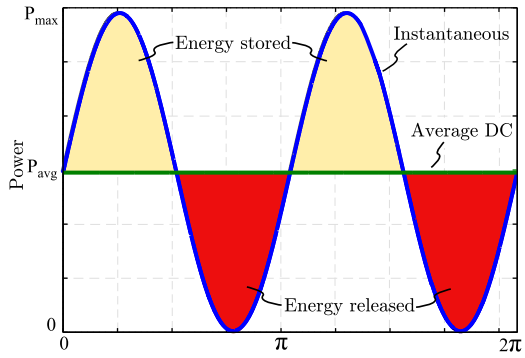

Fig. 1. Comparison of instantaneous power presented by single-phase ac at twice the line frequency and the average dc power over one power line cycle.

The simplest capacitive energy buffering strategy is the placement of a large capacitor across the dc bus. The energy which must be stored in the dc bus capacitor (W_{buffer}) each line cycle is determined by the converter average power (P_{ave}) and the ac frequency (f_{line}), and can be expressed as

$$W_{\text{buffer}} = \frac{P_{\text{ave}}}{2\pi f_{\text{line}}}. \tag{1}$$

This energy will be stored in a capacitance (C) by rippling the voltage between some maximum ($V_{\max}$) and minimum ($V_{\min}$) value during each line cycle. For an ideal capacitor, the energy stored over this voltage range can be calculated as

$$W_{\text{buffer}} = \frac{1}{2}CV_{C\max}^2 - \frac{1}{2}CV_{C\min}^2. \tag{2}$$

Assuming a constant value of capacitance, and defining V_{avg} as the arithmetic average of $V_{\max}$ and $V_{\min}$, this result can be equivalently stated as

$$W_{\text{buffer}} = C * V_{\text{avg}} * \Delta V. \tag{3}$$

Many practical applications impose very strict ripple requirement on the dc bus voltage, so the voltage ripple, ΔV is typically limited [3]. To meet this ripple requirement and the accompanying energy storage requirement, a large capacitance is typically

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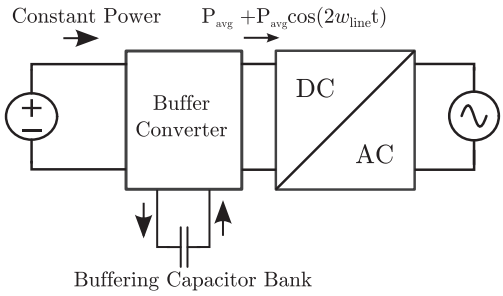

Fig. 2. Energy buffering circuit of single phase inverter.

required on the dc bus. Certain applications, such as power supplies for telecommunication and computing typically impose hold-up time requirements, where sufficient energy storage must be maintained to continue uninterrupted power delivery in the event of a short-term (e.g., one or a few line cycles) voltage disturbance. The energy storage requirements for such applications is typically significantly higher than for twice-line-frequency buffering.

Historically, designers have used electrolytic capacitors for energy buffering because of their relatively high energy storage density and relatively low cost. Unfortunately, electrolytic capacitors pose concerns in long-life applications because of the use of a wet electrolyte which evaporates with age. Electrolytic capacitors are also lossy during charging and discharging compared to other technologies [4]. When long system life is important, designers have the option to use capacitors with dry dielectric that will not evaporate such as film or ceramic capacitors. Film capacitors exhibit lower energy density than electrolytics, which results in a tradeoff between density and the lifespan of the completed system.

In contrast to electrolytic and film capacitors, multilayer ceramic capacitors (MLCCs) have a dry dielectric and moderate energy density. A significant drawback of MLCCs is that they have historically been comparatively costly and they are limited in size due to the fragile nature of ceramics. Thus, although ceramic capacitors exhibit high energy storage density per unit of volume, the accumulation of sufficient capacitance for passive energy buffering in a single package has been challenging due to cost and mechanical constraints. Additionally, the capacitance of MLCCs suitable for energy buffering also changes with dc bias voltage, aging, temperature, large signal amplitude, and frequency [5], [6].

The effective energy density of capacitors can also be improved dramatically by decoupling the energy storage and voltage regulation requirements of buffering as is done in [1]–[3], [7]–[15]. These systems interface the buffering capacitance to the dc bus through a power converter, thereby allowing the capacitor voltage to vary over a wider range while maintaining a constant dc bus voltage. A basic schematic of an energy buffering architecture is shown in Fig. 2. Such power buffering techniques enable the use of thin film and MLCCs because smaller capacitance values are needed as compared to a passive buffer comprised of a capacitor connected directly to the dc bus. Moreover, as will be shown, MLCCs offer comparable or higher energy density than film or electrolytic capacitors when used in active energy buffering applications.

A great deal of research has been done to characterize the performance of capacitors under small signal operation [16]–[18]. A key contribution of this work is the analysis and experimental verification of the performance of commercially available capacitors operating with large voltage swings. Although the focus of this work is twice-line-frequency energy buffering, many other applications use capacitors in large voltage swing operation to store and transfer energy. The design of switched-capacitor converters [19]–[23] (especially soft-charging converters [24], [25]), requires a knowledge of the practical energy storage capability of MLCCs operating with wide voltage swing at high frequencies. In this paper, we use experimental and analytical approaches to study the actual energy storage capability of various capacitors in detail, and have included test data from a range of capacitor technologies. This paper is an extension of our previous conference publication [26], with expanded experimental results and guidelines for the implementation of energy buffers using MLCCs.

The remainder of this paper is organized as follows. Section II discusses the proper method of evaluating the energy stored in a ceramic capacitor and how manufacturer provided data sheets can be used to obtain a good estimate of energy storage. Section III discusses the experimental setup that has been used to test the energy storage and power loss of a wide variety of capacitors. Section IV provides analysis of the measured data, highlighting energy density results across capacitor technologies. Section V includes an example of how the information in this paper can be used in the design of an active power buffer. Section VI concludes the paper.

II. Large Voltage Swing Characteristics

A. Fundamentals of Ceramic Multilayer Capacitors

There are three classes of ceramic dielectrics defined per IEC/EN 60384-1. The three main classes of ceramic capacitors are tailored for a range of operating temperatures and designated by a three character code, which indicates the minimum operating temperature, maximum operating temperature, and the deviation in capacitance over the temperature range, respectively.

Capacitors with the temperature class designations of NP0, CG, and C0G employ Class I dielectrics. Class I ceramics are paraelectrics, which have dielectric constants that are stable with temperature, dc bias, and capacitor age. Class I capacitors also have low loss and therefore, a high quality factor. These characteristics make Class I devices well suited for resonant and precision circuits. The main drawback of Class I ceramics, in energy buffering applications, is that they have a low relative permittivity (ϵ_r) of 15–100, and therefore have low energy storage density [5], [27], [28].

Barium titanate-based ($BaTiO_3$) Class II ceramic dielectrics are ferroelectric, with relative permittivities in the range of $\epsilon_r =$ 2000–4000, and are the focus of this work. One drawback of Class II ceramics is that their permittivity, and hence the capacitance of the device they are used in, decreases significantly with applied electric field [18]. This decrease in permittivity under electric field saturation is analogous to the decrease in relative magnetic permeability exhibited by magnetic materials under high magnetic fields.

Fig. 3 shows the manufacturer's specified capacitance for a Class II device designed for 450 V operation. It can be seen that the capacitance can decrease by as much as 78% at the rated voltage compared to the value at a bias voltage of zero. Some

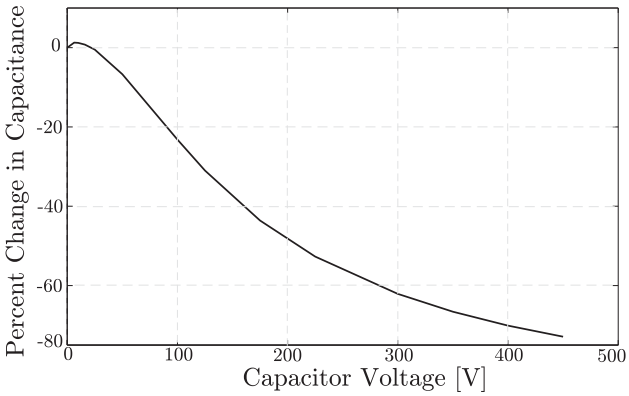

Fig. 3. Plot of capacitance change versus bias voltage for TDK CKG57NX7R2J474M500JH capacitor [29].

example Class II temperature designations include X8R, X7R, X5R, and X6S. In practice, it is found that energy storage in MLCCs increases approximately linearly with voltage, instead of quadratically as one would expect if the dielectric permittivity were independent of voltage [27].

Class III ceramic dielectrics have an even higher relative permittivity than Class II, with values of up to 50 000. However, along with this high initial permittivity, Class III devices also exhibit higher variation in capacitance values with temperature, voltage, and age than Class II devices [18]. Hence, although Class III capacitors typically have exceptional initial capacitance density, they are not ideal for energy storage.

B. Calculation of Energy Storage Density

In order to account for the voltage dependence of a ceramic capacitor as the capacitor is charged from $V_{\min}$ to $V_{\max}$, the energy stored in the capacitor (W_{stored}) can be defined as

$$W_{\text{stored}} = \int_{q_{\min}}^{q_{\max}} v \, dq \tag{4}$$

where q is the charge in the capacitor. Using the substitution

$$dq = C(v) \, dv \tag{5}$$

(4) can be rewritten as

$$W_{\text{stored}} = \int_{V_{\min}}^{V_{\max}} C(v) v \, dv. \tag{6}$$

It is important to note that C is now a function of voltage, and $V_{\min}$ and $V_{\max}$ are the limits of the voltage ripple imposed on the capacitor. It can be seen that, if C is independent of v, then the integration of (6) will yield (2).

Equation (6) is idealized in that it does not take into account the energy lost due to capacitor non-idealities during charging or discharging. The dominant capacitor losses are usually combined into an equivalent series resistance (ESR), therefore the energy required to charge the capacitor may be approximated in terms of losses and W_{stored} as

$$W_{\text{charge}} = W_{\text{stored}} + i_{\text{RMS}}^2 \, R_{\text{ESR}} \, T_{\text{cycle}} \tag{7}$$

where i_{RMS}, R_{ESR}, and T_{cycle} are the RMS capacitor current, the ESR, and the buffering period, respectively. Equation (7)

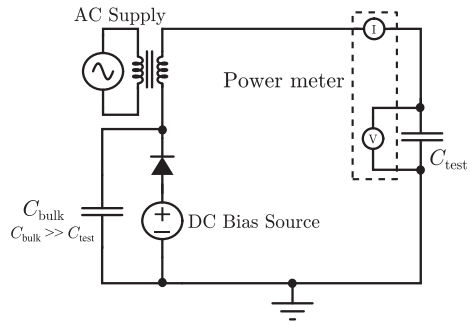

Fig. 4. Capacitor test schematic.

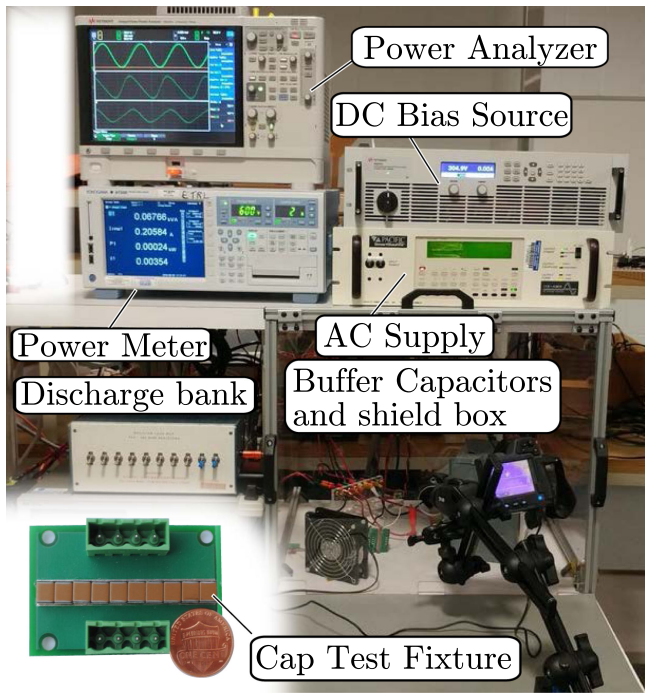

Fig. 5. Experimental test setup and capacitor test fixture with 10 MLCCs.

can be alternatively stated as

$$W_{\text{charge}} = W_{\text{stored}} + W_{\text{loss}} \tag{8}$$

where W_{loss} is the loss incurred over the complete charge and discharge cycle. The ESR in (7) represents device physical series resistance and parallel leakage as well as the hysteretic losses, which result from a realignment of the electrostatic domains within the dielectric. The hysteretic losses are of special interest because they are dependent on frequency and potentially the voltage bias at which the capacitor is operated [6].

C. Characterization of Capacitor Performance

Round-trip efficiency is an important parameter in the evaluation of any energy storage system. The capacitor full-cycle energy storage efficiency is defined as the ratio of the energy extracted from the capacitor during discharge to the energy supplied to charge the capacitor, or equivalently

$$\eta = \frac{W_{\text{charge}} - W_{\text{loss}}}{W_{\text{charge}}} \times 100\%. \tag{9}$$

TABLE I
EQUIPMENT USED IN CAPACITOR EXPERIMENTAL TEST CIRCUIT

Label	Instrument
DC Bias Source	Keysight N8937A
Power Meter	Yokogawa WT3000E
Power Analyzer	Keysight PA2201A
AC Supply	Pacific Smart Source 112-AMX
Isolation Transformer	Schneider Electric Cat. No: 151F

As discussed in the Introduction, energy density is also of primary importance in energy buffers and defined to be

$$C_{\text{Density}} = \frac{W_{\text{charge}} - W_{\text{loss}}}{\text{Capacitor volume}}. \tag{10}$$

Another capacitor characteristic used in some applications is the quality factor, or Q factor of the capacitor. This characteristic normalizes the energy stored in the capacitor (or any resonant system) by the amount of energy lost per cycle [30]. The Q factor can be defined as

$$Q = \frac{2\pi \times (W_{\text{charge}} - W_{\text{loss}})}{W_{\text{loss}}}. \tag{11}$$

III. EXPERIMENTAL MEASUREMENT OF ENERGY STORAGE

As the preceding discussion has shown, it is important to accurately calculate the energy storage of capacitors and MLCCs in particular. We have, therefore, performed detailed experimental characterization of a number of capacitors of different voltage ratings, dielectrics, and packages under large signal voltge swing. This testing strategy also enables an accurate assessment of losses in energy buffering applications with large signal, conditions so that hysteretic and other second-order losses are properly represented [6]. In order to equitably select a group of test devices, the basic specifications for thousands of ceramic, electrolytic, metalized polyester, and metalized polypropylene capacitors were mined from supplier data. The energy storage density for each device was calculated based on the volume, capacitance at zero bias, and rated voltage of the devices using (2). It should be pointed out that this is a simplification required to narrow the scope of the project as one of the main points of this work is that (2) does not accurately capture energy storage. It is possible that the characteristics of different dielectrics may yield different energy storage densities at operating voltage. To address this issue, the highest density devices of each dielectric technology and voltage ratings of 50, 100, 250, 450, and 630 volts were selected. In some instances, the highest density capacitors were devices with individual capacitances, which were too small for practical energy buffering applications. In these cases, a device with slightly lower energy density but a capacitance of 1 μF or greater was typically chosen.

A schematic for the experimental test circuit is shown in Fig. 4. This test configuration was capable of varying both the ac voltage ripple amplitude and dc voltage bias of the capacitors. To increase measurement accuracy and average tolerances between capacitors, the capacitors were typically tested in sets of six or more. A photo of the test equipment and capacitor test holder is shown in Fig. 5. A list of the hardware used is presented in Table I.

During the testing of the film and ceramic capacitors, the voltage was cycled from 0 to the rated voltage with an average value of one-half the rated voltage. Thus, the dc bias was 50% of the rated voltage and the ac peak amplitude was 50% of the rated voltage. This replicates the waveform imposed when the capacitor is used in an active twice-line-frequency unipolar buffer application. In the case of the electrolytic capacitors, however, this full voltage range ripple far exceeded the current rating of the devices. The electrolytic capacitors were instead rippled between the rated voltage and the lowest voltage possible such that the manufacturer-defined RMS current rating was not exceeded. The integration function of the Yokogawa WT3000E meter was used to measure the energy flowing into and out of the capacitor. This work was specifically focused on determining the performance of the capacitors in twice-line-frequency applications, therefore the capacitors were cycled at 120 Hz. During testing, an integration of energy flowing into and out of the each device was performed over 5 separate 30-s intervals. The standard error for each set of five measurements is included with the full data in Table III of Appendix A. This approach thus computed the average energy stored over 3600 cycles, and nullified any phase-induced measurement errors. With the integral of power given by the meter in watt-hours, and the integral of current given in amp-hours, a unit conversion then yields energy transferred into and out of the capacitor over a complete cycle.

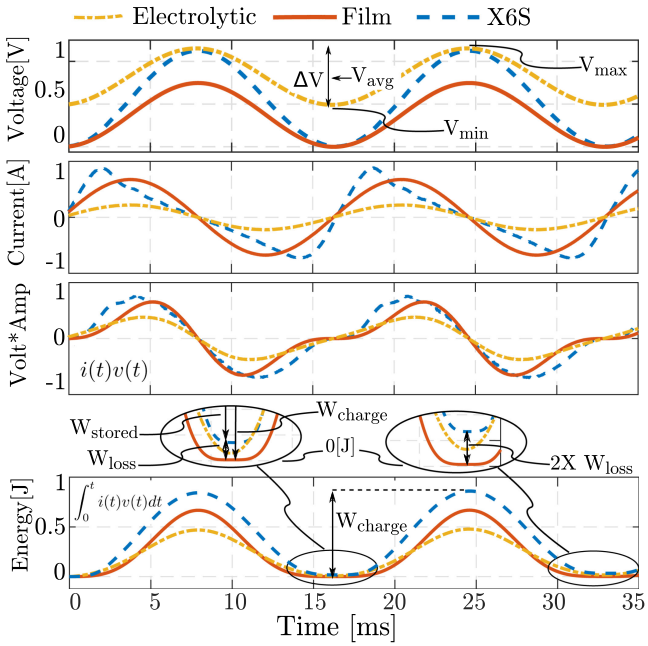

Fig. 6. Experimental test waveforms for electrolytic, X6S ceramic and metallized polyester capacitors.

IV. CAPACITOR PERFORMANCE EVALUATION

A. Behavior of Capacitor Energy Storage Under Large Voltage Swings

Fig. 6 compares the experimental charge and discharge waveforms for an X6S Type II ceramic capacitor, a bias-independent film capacitor, and an electrolytic capacitor. All three capacitors have sinusoidal ac voltage applied, however, it can be seen that the bias-dependent capacitance of the X6S capacitor leads to a linearly increasing/decreasing current while the current drawn by the other two capacitors is sinusoidal. The quantities refer-

TABLE II
MEASURED AND CALCULATED ENERGY STORED PER CYCLE FOR TYPE II CERAMIC CAPACITORS

Approach	X6S 2.2 uF	X7R 0.47 uF	X5R 0.22 uF	X7T 2.2 uF	Avg. Error
Measured (mJ)	66.9	21.4	11.4	84.3	
Calculated using $C(0V)$ (mJ)	203.9	46.1	23.5	194.4	+80.58%
Calculated using $C(450V)$ (mJ)	36.1	7.6	3.9	52.6	-74.84%
Calculated using $C(v)$ (mJ)	58.9	20.6	10.6	81.3	-6.84%

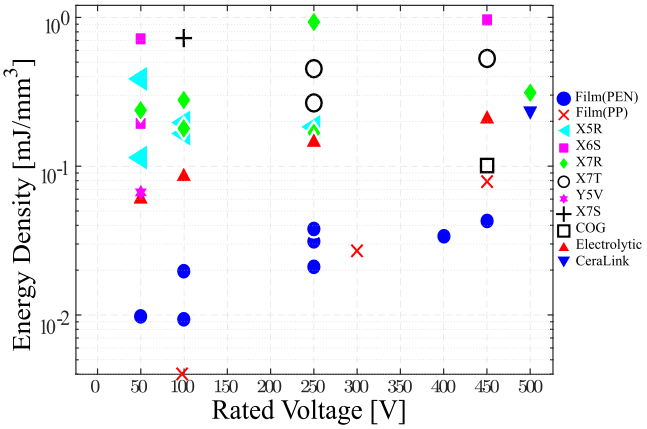

Fig. 7. Measured capacitor energy density with film capacitors ranking among the lowest energy density and ceramics ranking among the highest.

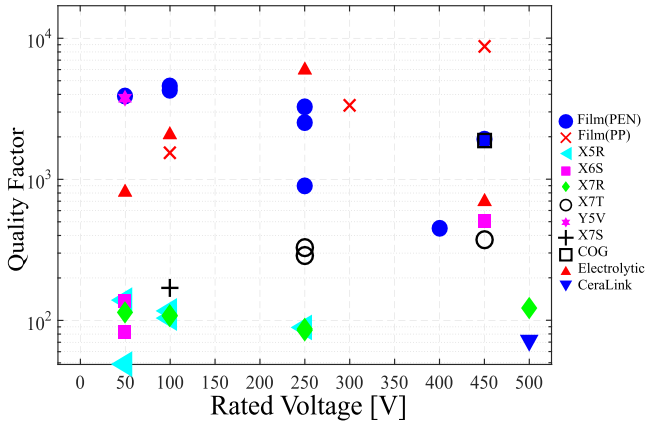

Fig. 8. Measured capacitor quality factor showing that film capacitors rank among the highest in quality factor.

enced in (2)–(8) are labeled as well. Of particular interest is the offset between the minimum energy after the first and second cycle and the numerical zero value. This measurement of W_{loss} shows the difference between the energy extracted from the capacitor and the energy which would theoretically be available if the capacitor was 100% efficient.

For a first high-level design iteration, it is helpful to estimate energy storage based on manufacturer specified capacitance. Table II shows three different estimations of capacitor energy storage at rated voltage based on data sheet specifications. For each device, the manufacturer-provided capacitance versus voltage data is scaled by the ratio of the measured to nominal capacitance of the test devices at zero bias voltage. This reduces the impact of tolerance and aging on the results of Table II.

The first data row of Table II is the experimentally *measured* energy stored by the capacitor minus losses. This value is then compared to the energy storage *calculated* based on the nominal capacitance value and the manufacturer supplied capacitance at full voltage using (2), in rows 2 and 3, respectively. The fourth row of Table II shows the energy storage calculated using a midpoint Riemann sum over $C(v)$ from the manufacturer data sheet. This approach applies (6) to accurately calculate the stored energy for a changing capacitance value while taking the losses of (7) into account. The last column on the right shows the error between a given method and the measured energy storage of the capacitor. This value is averaged over all capacitors.

It is evident that the use of a constant nominal capacitance over the full voltage range leads to very inaccurate energy storage estimation when device capacitance is bias dependent as it is in ceramic capacitors. However, by performing piece-wise integration using the manufacturer-provided capacitance data, the energy stored in the capacitor between two voltage levels can be estimated with relatively small (i.e., $< \pm$ 10%) error. This accuracy is contingent on the accuracy of the manufacturer-supplied capacitance derating with bias. It is worth noting that the energy storage capabilities of all ceramic capacitors are underestimated numerically. It is suspected that this is due to ESR losses being overestimated. Future work will seek to better identify these sources of error.

B. Full Comparison of Devices

It is also insightful to see how trends in energy density develop over a broader range of capacitor technologies. Shown in Fig. 7 is a plot of measured capacitor energy density versus rated voltage, for metal film, ceramic, and electrolytic capacitors, as indicated in the legend.

It is observed that MLCCs generally achieve the highest energy density under this test scenario. It should be re-emphasized that the electrolytic capacitors tested here were current ripple limited, meaning that although they can fundamentally store more energy than what is shown here, not all of that energy can be effectively *transferred* at twice-line-frequency without causing excessive loss (and heating). While the metal film capacitors (metalized polyester and metalized polypropylene) evaluated in this study have relatively low energy density, their low-loss is readily apparent in Fig. 8, which shows the capacitor Q factors versus voltage ratings. It should be noted that the Q factor here is as defined in (11), and is derived from measured energy loss and storage capability.

Cost is another important consideration in system design. Fig. 9 explores the relationship between the capacitor normalized energy storage cost and the device energy density over the range of capacitors tested. With X-axis of energy density inverted from the normal direction of increase, high-performance components are plotted toward the lower left of the figure. It is of special interest to see that cost of MLCCs is currently an order

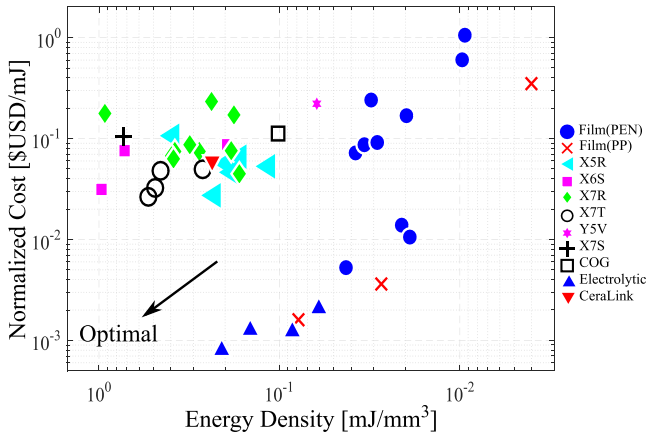

Fig. 9. Normalized cost of energy storage versus energy storage density. 10 k quantity assumed. Under full amplitude voltage ripple, ceramic capacitors have up to an order of magnitude higher energy density than electrolytics. This is at the expense of over an order of magnitude higher cost [31], [32].

of magnitude higher than high density electrolytic capacitors. However, under the constraints of full range voltage ripple, they are able to store an order of magnitude more energy on a per-cycle basis. Additionally, MLCCs generally come in smaller form factors and in lower capacitance values than metal film and electrolytic capacitors, therefore requiring a large number of individual capacitors to be paralleled. While this may lead to reliability and manufacturing challenges, it also enables flat and customizable form factor, which may be important in some applications.

Fig. 10 displays Q factor versus energy density for all capacitors evaluated in this study. For the twice-line-frequency buffering applications considered here, the MLCCs again stand out for their high energy density, and acceptable Q factor. It should be noted that at higher frequencies the tradeoff between Q factor and energy density may be different, leading to other preferred capacitor technologies.

V. Energy Buffering Converter Design

The preceding sections of this manuscript have evaluated the large-signal performance of a range of capacitor technologies and have shown that MLCCs have some of the highest energy density among the non-electrolytic devices. As discussed, this trait comes with the complication that the capacitance of these devices changes with dc bias voltage. In order to utilize the results presented in Section IV in the design of a high power density active energy buffer, it is important that the design of the power converter in which the capacitors will be used be tailored to the capacitor characteristics. It will be shown that the power density of the system can also be improved by rippling the voltage of the buffer capacitors at a voltage lower than the capacitor's maximum specified voltage. In this design discussion, the focus will be on minimizing overall system volume, however this strategy can be incorporated into a more comprehensive optimization with specific cost and efficiency goals.

A. Impact of Voltage Ripple Range on Capacitor Energy Storage Density

In order to understand the implications of bias dependent capacitance on the energy buffering system, it is helpful to first compare the energy storage density of a bias-independent capacitor and an MLCC bias-dependent ceramic capacitor. As is highlighted by (3), it is typically advantageous to operate energy buffering capacitors such that the ripple and dc average voltage are optimized with respect to the constraints imposed by the peak voltage limits of the system. Assuming unipolar voltage ripple, the ripple is constrained to

$$\frac{\Delta V}{2} < V_{pk} - V_{\text{avg}}. \tag{12}$$

To maximize density, V_{pk} should be the highest voltage within the system limits. For a system using bias-independent capacitors, the highest energy density for a given V_{avg} is calculated as

$$W_{\text{buffer}} = 2CV_{\text{avg}} * (V_{pk} - V_{\text{avg}}) \tag{13}$$

which implies that the maximum energy can be stored by operating with $V_{\text{avg}} = \frac{V_{pk}}{2}$.[1]

Fig. 11 plots energy storage density, as a function of capacitor average voltage and ripple for a capacitor with a voltage independent dielectric. This "ideal capacitor" is assumed to have a value of 2.2 μF, and a 2220 SMT package. It can be seen that the highest energy density tends to be located at high ripple voltage and the highest average voltage which can be accommodated by the system. However, the optimal operating voltage range for systems based on real (bias-dependent) MLCCs is not as clear due to bias-dependent capacitance.

Fig. 12 plots the corresponding energy density for the bias-dependent X6S ceramic capacitor enumerated as 26 in Fig. 10 and Appendix A. The X6S ceramic is used for reference because it has the highest energy density of the evaluated MLCCs. Although the trend in Fig. 12 is similar to that in Fig. 11, it will be noted that the contours of equal energy density are more vertically aligned as opposed to the diagonally aligned equidensity lines in Fig. 11. This shows that the energy density of ceramic capacitors is reduced at high bias voltage. The absolute difference in energy density between the two plots is not the focus of this comparison. Instead, the purpose is to compare the relative values of ripple voltage and average voltage that yield the maximum energy density in both cases.

In addition to identifying the average voltage and ripple at which the capacitor energy storage density is the highest, it is important to consider the capacitor operating voltage range, which will minimize the volume of the entire buffer system. For the active buffer in Fig. 13, the inductance requirements, current rating, and system losses will change over the range of average voltages and voltage ripple magnitudes shown in Figs. 11 and 12. These factors will each have an impact on the overall system density.

At least 50 different topologies have been proposed for energy buffering applications [1], [33]. These designs each represent tradeoffs between complexity, size, and performance, with different benefits and drawbacks. The full ripple port topology shown in Fig. 13 is a relatively simple and robust architecture, which allows a large degree of flexibility in the capacitor dc bias and ripple voltage and has been utilized in a number of works [8], [9]. Because of its simplicity and broad design space,

[1]The authors especially thank a journal reviewer for sharing their thoughts in articulating this concept.

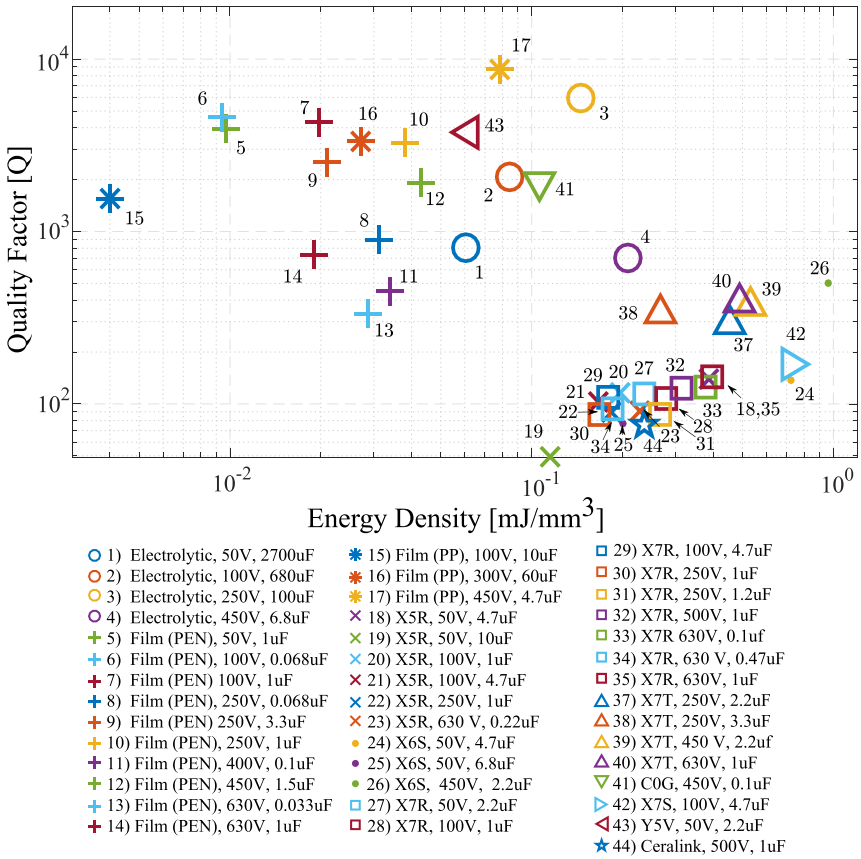

Fig. 10. Capacitor Q versus energy storage density.

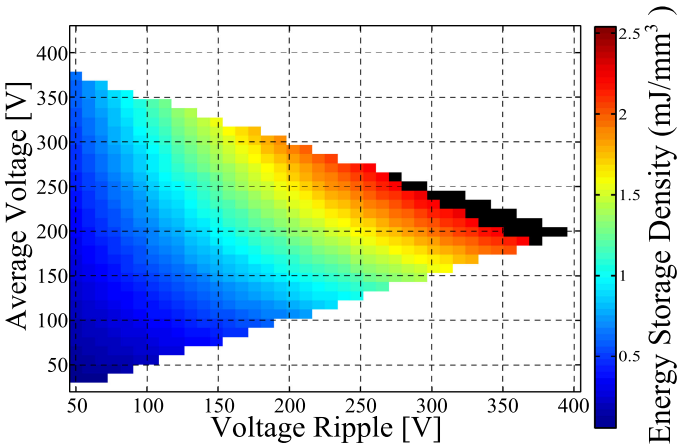

Fig. 11. Energy buffering density for a bias-independent 2.2 μF capacitor with the same dimensions as #26. Black region indicates top 10% of energy density. It can be observed that, under the constraint of the capacitor and switch voltage ratings, the maximum energy density is obtained by maximizing the voltage ripple and maintaining as high of an average voltage as possible.

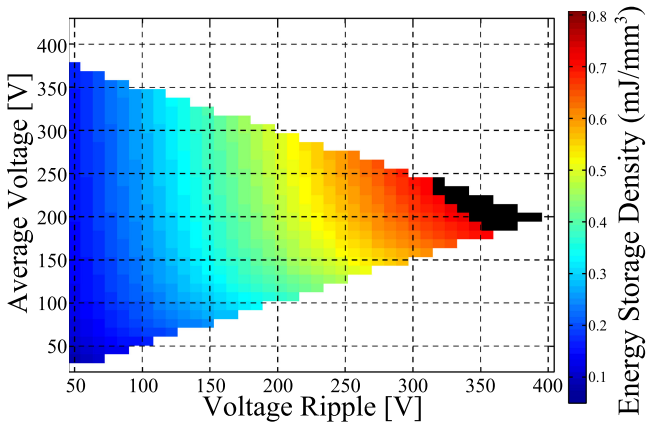

Fig. 12. Energy buffering density for the 2.2 μF, 450 V, X6S capacitor #26. Black region indicates top 10% of energy density. In the bias-dependent buffer configuration note that the maximum energy density still occurs at high voltage ripple, however, the average voltage is shifted slightly down. This difference is small, however, exploring the implications of this shift is the focus of this section.

the full ripple port converter will be used in this work to illustrate the design of an energy buffering converter using ceramic capacitors.

The following design sequence outlines a general approach to minimizing the overall converter volume.

1) Determine maximum twice-line-frequency energy storage required for the application as specified by (1).
2) Model the voltage dependence of the capacitor technology to be used.
3) Develop a model for converter losses and volume as a function of the average voltage and ripple of the buffering capacitors.
4) Iterate over the feasible range of average voltage and ripple voltage to determine system power density for each operating condition.

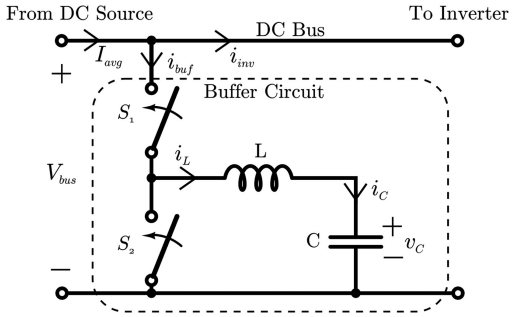

Fig. 13. Bidirectional buffer converter schematic.

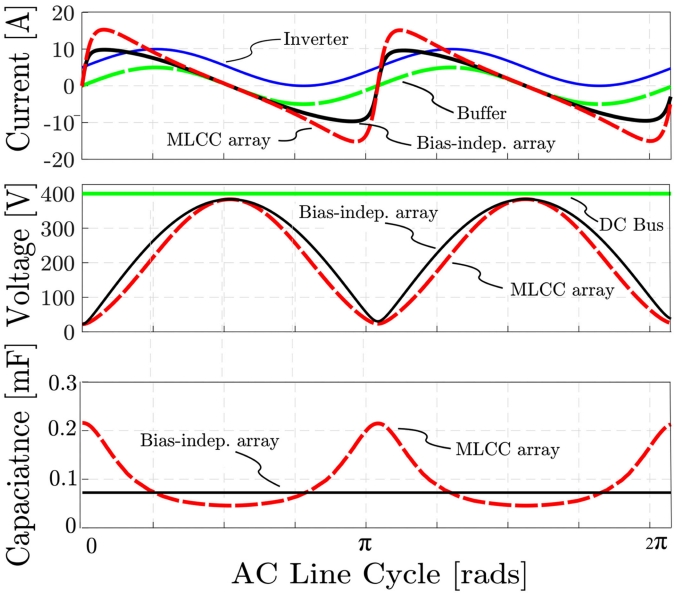

Fig. 14. Operating waveforms for capacitor array, buffer, and inverter. The peak currents of the MLCC array are significantly higher than the peak currents for an ideal capacitor array due to the large change in capacitance of the MLCC array over the line cycle.

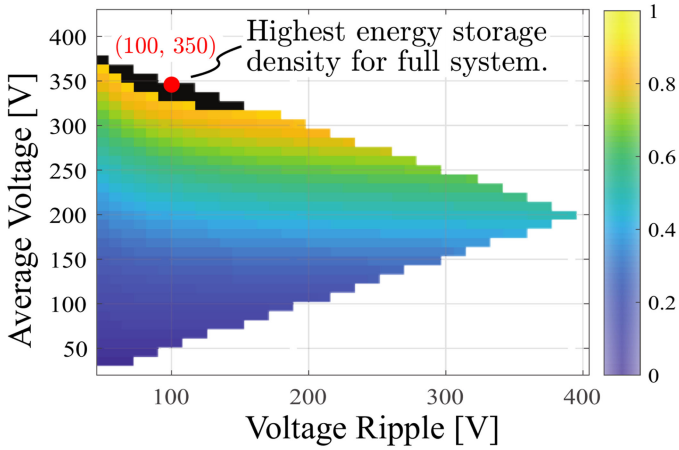

Fig. 15. Normalized relative energy density over ripple and average voltage for a full system including *bias-independent* capacitors, inductor, and heatsink. Black region indicates top 10% of density. It can be seen that the maximum energy density occurs at high average voltage.

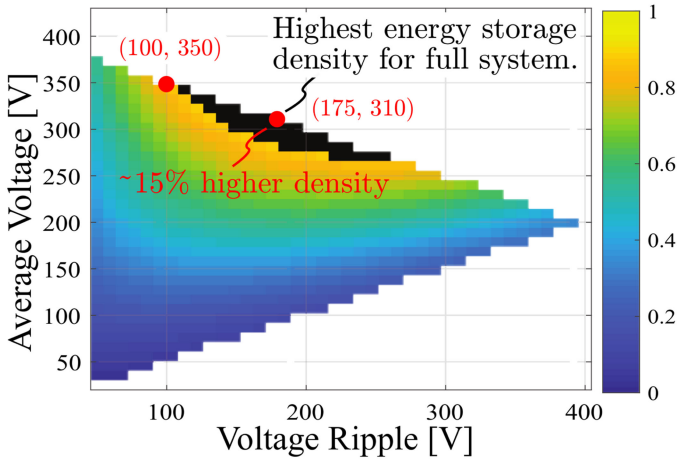

Fig. 16. Normalized relative energy density over ripple and average voltage accounting for *X6S MLCCs*, inductor, and heatsink. Black region indicates top 10% of density. It can be see that the maximum energy density occurs at a lower average voltage of 310 V as opposed to the system using bias-independent capacitors, which achieve optimal energy density at an optimal energy density of 350 V. Under the assumptions of this analysis, the system energy density can be increased $\approx 15\%$ through operating at 310 V average as opposed to 350 V average.

This procedure is discussed in more detail in Appendix B, and a summary of key results follows.

B. Impact of Voltage Ripple Range on Energy Storage Density of the Full Buffer Converter

It is first significant to note the difference between the operating waveforms of a buffer converter built using MLCCs and capacitors with voltage-independent dielectrics. Fig. 14 shows calculated values of the inverter current, buffer current, and capacitor current for one full cycle for both an ideal capacitor array and the MLCC capacitor array. In this example, both arrays are sized to ripple between equal voltage limits and store equal energy as required by (1) for a complete line cycle. Although the ripple limits of both capacitor banks are equal, the amount of energy stored at each differential voltage is not equal. This is because at high voltage, the MLCC array has a lower capacitance than the ideal capacitor and at low voltage the capacitance of the X6S capacitor is over 2 $\times$ larger than the capacitance of the ideal capacitor.

The impact of this characteristic is clearly seen by comparing the three plots in Fig. 14. Considering the lower plot, it is seen that the capacitance of the MLCC array at the minimum capacitor voltage is over twice that of the ideal array. Thus, the dynamically changing capacitance of the X6S, MLCC capacitor array results in higher peak currents in the buffering capacitor and converter than occur for the bias-independent capacitor array. These higher peak currents translate into higher conduction and switching losses, which must be taken into account in the overall optimization of the energy buffering system.

Combining the density impact of the MLCCs, the inductors, and the system cooling, it is possible to identify the buffering energy density which can be obtained for each value of buffering capacitor average voltage and voltage ripple. Details can be found in Appendix B. Fig. 15 shows the plot of normalized system buffering energy densities that can be achieved using the previously specified bias-independent capacitors and a unipolar, hard switched, and ripple-port converter to implement a twice-line-frequency buffer. Similarly, Fig. 16 shows the rela-

tive energy density obtained for an active buffer developed using the X6S capacitors numbered 26 in Fig. 10.

It can be seen that the highest system-level energy density can be obtained by operating the bias-independent capacitors at 350 V average with a 100 V peak ripple, while the optimal average for the X6S capacitors is a 310 V average and a 180 V ripple voltage. Looking at the color gradient, it is evident that operating the X6S-based system at the same optimal ripple range as the bias-independent system would result in an $\approx 15\%$ reduction in the power density of the system. This shows that there is a benefit to be obtained through taking the characteristics of the bias-dependent capacitors into account in the design of energy buffering systems. Additionally, it can be seen that this benefit extends beyond the initial sizing of the capacitor bank. This general process can be repeated for any given ceramic capacitor in order to obtain the optimal operating range for overall system power density.

VI. Conclusion

This paper has explored the selection of ceramic capacitors for energy buffering applications. Suitable methods for computing the energy stored in ceramic capacitors are discussed and demonstrated through experimental measurements. Additionally, the energy density and quality factor of ceramic capacitors is compared to polyester and polypropylene film capacitors as well as electrolytics. Finally, the results discussed in the initial sections of the paper are applied in the design process of a line frequency buffer. It is found that the optimal voltage ripple range is changed by the derating of Class II ceramic capacitors. It is the hope of the authors that the operational data, demonstrated test method, and system design suggestions, will be useful tools for designers to select, size and design with the appropriate ceramic capacitors for line energy buffering and other applications.

Appendix A
Experimental Capacitor Performance Data

TABLE III
Measured 120 Hz Capacitor Performance Data Plotted in Fig. 10

#	Description	Manufacturer PN	Efficiency		Q		Density mJ/mm^3		Cost ($USD)@10,000
			Mean	SE	Mean	SE	Mean	SE	
1	Electrolytic, 50 V, 2700 uF	EPCOS(TDK) - B41858C6278M	99.20%	0.14%	809	153	6.03E-2	9.39E-4	1.34
2	Electrolytic, 100 V, 680 uF	EPCOS(TDK) - B41858C9687M	99.45%	0.37%	2074	1550	8.49E-2	2.14E-4	1.10
3	Electrolytic, 250 V, 100 uF	EPCOS (TDK) - B43888F2107M	99.30%	0.34%	5968	10280	1.45E-1	8.92E-4	1.23
4	Electrolytic, 450 V, 6.8 uF	EPCOS (TDK) - B43890A5685M	98.92%	0.40%	698	329	2.08E-1	3.82E-4	0.29
5	Film (PEN), 50 V, 1 uF	Kemet - LDECD4100KA0N00	99.51%	0.35%	3921	3793	9.74E-3	1.96E-5	0.77
6	Film (PEN), 100 V, 0.068 uF	Panasonic - ECW-U1683KC9	99.49%	0.52%	4582	4281	9.40E-3	2.55E-5	0.37
7	Film (PEN) 100 V, 1 uF	Kemet - LDEEE4100KA0N00	99.69%	0.16%	4306	5010	1.97E-2	3.92E-6	0.79
8	Film (PEN), 250 V, 0.068 uF	Kemet - LDEID2680JA5N00	99.03%	0.35%	898	690	3.11E-2	2.12E-3	0.51
9	Film (PEN) 250 V, 3.3 uF	Nichicon - QAK2E335KTP	99.62%	0.29%	2528	1249	2.10E-2	4.90E-5	1.46
10	Film (PEN), 250 V, 1 uF	Panasonic - ECW-U2105KCZ	99.56%	0.35%	3277	2675	3.80E-2	7.06E-5	2.21
11	Film (PEN), 400 V, 0.1 uF	Kemet - LDEME3100JA5N00	98.45%	0.43%	448	173	3.39E-2	7.45E-5	0.71
12	Film (PEN), 450 V, 1.5 uF	Panasonic - ECQ-E2W155KH	99.64%	0.11%	1934	666	4.29E-2	2.55E-5	0.81
13	Film (PEN), 630 V, 0.033 uF	Panasonic - ECW-UC2J333JV	98.05%	0.40%	331	69	2.88E-2	2.18E-4	0.60
14	Film (PEN), 630 V, 1 uF	Nichicon - QAK2J105KTP	99.13%	0.13%	732	128	1.89E-2	2.55E-5	2.12
15	Film (PP), 100 V, 10 uF	Cornell Dubilier - 935C1W10K-F	99.54%	0.14%	1545	668	3.99E-3	9.80E-6	17.47
16	Film (PP), 300 V, 60 uF	EPCOS (TDK) - B32678G3606K	99.67%	0.22%	3332	1482	2.71E-2	5.88E-5	9.84
17	Film (PP), 450 V, 4.7 uF	Panasonic - ECW-FD2W475J	99.85%	0.15%	6753	4364	1.10E-1	2.16E-4	0.55
18	X5R, 50 V, 4.7 uF	TDK - C2012X5R1H475K125AB	95.65%	0.45%	140	15	3.88E-1	1.90E-2	0.15
19	X5R, 50 V, 10 uF	Kemet - C1210C106K5PACTU	88.57%	0.23%	49	1	1.15E-1	2.80E-4	0.32
20	X5R, 100 V, 1 uF	TDK - C3216X5R2A105K160AA	94.84%	0.35%	116	9	1.96E-1	1.11E-3	0.10
21	X5R, 100 V, 4.7 uF	TDK - C3216Y5V1H225Z/1.15	94.25%	0.35%	103	7	1.66E-1	1.63E-3	0.75
22	X5R, 250 V, 1 uF	TDK - C5750X5R2E105K230KA	93.44%	0.21%	90	3	1.83E-1	5.92E-4	0.56
23	X5R, 630 V, 0.22 uF	TDK - C5750X5R2J224M230KA	93.54%	0.46%	91	7	2.29E-1	7.55E-4	0.41
24	X6S, 50 V, 4.7 uF	TDK - C2012X6S1H475K125AC	95.58%	0.39%	137	13	7.21E-1	1.64E-3	0.20
25	X6S, 50 V, 6.8 uF	TDK - C3225X6S1H685M250AC	92.98%	0.40%	83	5	1.95E-1	1.11E-3	0.47
26	X6S, 450 V, 2.2 uF	TDK - C5750X6S2W225M250KA	98.73%	0.21%	503	98	9.65E-1	8.58E-4	1.13
27	X7R, 50 V, 2.2 uF	TDK - C2012X7R1H225K125AC	94.78%	0.34%	115	8	2.37E-1	8.11E-4	0.20
28	X7R, 100 V, 1 uF	TDK - C3216X7R2A105K160AA	94.44%	0.36%	107	8	2.79E-1	3.78E-3	0.14
29	X7R, 100 V, 4.7 uF	TDK - CKG45NX7R2A475M500JJ	94.52%	0.45%	109	9	1.79E-1	8.53E-4	2.09
30	X7R, 250 V, 1 uF	TDK - C5750X7R2E105K230KA	93.27%	0.30%	87	4	1.67E-1	3.16E-4	0.53
31	X7R, 250 V, 1.2 UF	Kemet - C2225C125KARACTU	93.09%	0.32%	85	4	2.56E-1	3.00E-3	0.96
32	X7R, 500 V, 1 uF	Knowles - 2220Y5000105KXTWS2	95.12%	0.14%	123	4	3.14E-1	6.92E-4	3.51
33	X7R 630 V, 0.1 uF	AVX - 2220CC105KAZ2A	95.16%	0.46%	125	13	3.78E-1	1.69E-3	2.10
34	X7R, 630 V, 0.47 uF	TDK - CKG57NX7R2J474M500JH	93.72%	0.11%	94	2	1.85E-1	5.76E-4	2.18
35	X7R, 630 V, 1 uF	Knowles - 2220Y6300105KXTWS2	95.75%	0.34%	143	12	3.96E-1	1.25E-3	3.43
36	X7R, 1000 V, 0.47 uF	Knowles - 2220Y1K00474KXTWS2	95.14%	0.39%	124	11	3.86E-1	9.74E-4	3.12
37	X7T, 250 V, 2.2 uF	TDK - CGA9P3X7T2E225M250KE	97.80%	0.37%	288	54	4.55E-1	1.35E-3	1.52
38	X7T, 250 V, 3.3 uF	TDK - CKG57NX7T2E335M500JH	98.11%	0.16%	329	31	2.67E-1	5.64E-4	2.18
39	X7T, 450 V, 2.2 uF	TDK - CKG57NX7T2W225M500JH	98.21%	0.46%	372	102	5.32E-1	1.36E-3	2.18
40	X7T, 630 V, 1 uF	TDK - CKG57NX7T2J105M500JJ	98.38%	0.20%	388	54	4.87E-1	1.26E-3	2.61
41	C0G, 450 V, 0.1 uF	TDK - C5750C0G2W104K280KA	99.47%	0.34%	1885	1272	1.01E-1	2.69E-4	1.00
42	X7S, 100 V, 4.7 uF	TDK - 12061Z475KAT2A	96.39%	0.39%	170	21	7.25E-1	6.06E-2	0.74
43	Y5V, 50 V, 2.2 uF	TDK - C3216Y5V1H225Z/1.15	99.55%	0.30%	3755	4551	6.23E-2	9.60E-5	0.08
44	Ceralink, 500 V, 1 uF	TDK - B58031I5105M002	92.32%	0.39%	76	4	2.37E-1	7.84E-4	5.58

APPENDIX B
DETAILS OF CONVERTER VOLUME ESTIMATION

This appendix discusses the calculations and assumptions made to compare the volume, and by extension, the effective energy storage density of a twice-line-frequency buffering converter utilizing an MLCC capacitor array and one using a bias-independent array as defined in Section V. The purpose of this appendix is to inform readers of the assumptions made to determine the impact of MLCC capacitors on buffer converter power density.

A. Calculation of Required Inductance and Current Stress

In order to simplify the optimization and comparison of buffering converter designs, it is helpful to have a defined relationship between converter input and output voltage so that input and output current flow and power can be defined. This constraint can be guaranteed by designing with a large enough inductance that the converter operates in continuous conduction mode (CCM) with non-zero current flow through the inductor at all times. Under this condition, the relationship between the bus voltage ($V_{\rm bus}$) and the capacitor voltage (v_C) for the converter of Fig. 13 is

$$d_{S1}(v_C) = \frac{v_C(t)}{V_{\rm bus}} \tag{14}$$

where d_{S1} is the instantaneous duty ratio of switch S_1. This relationship holds throughout the line cycle as the capacitor is charged and discharged from the constant voltage dc bus. At any point in the line cycle, the required duty ratio of the converter is simply the ratio of instantaneous capacitor voltage to bus voltage.

Although the limits of the converter duty ratio are known based on the bus voltage and intended capacitor voltage ripple range, it is helpful to calculate the instantaneous converter duty ratio over the line cycle so that instantaneous capacitor and inductor current can be calculated. With the dc bus voltage fixed, it is only necessary to determine the instantaneous capacitor voltage over the line cycle and the duty ratio follows directly from (14). Because capacitor voltage is determined by the charge stored on the capacitor, one method of determining instantaneous capacitor voltage is to integrate the capacitor current, which must be enforced to meet buffering requirements.

Referencing Figs. 1 and 13, it can be observed that the current feeding the inverter ($i_{\rm inv}$) takes the form

$$i_{\rm inv}(t) = I_{\rm avg} + I_{\rm avg}\ \cos(2\omega t). \tag{15}$$

Equation (15) is the sum of the current supplied by both the buffer and the dc source. Assuming constant current and voltage from the dc supply, the buffer must supply a current ($i_{\rm buf}$) of

$$i_{\rm buf}(t) = -I_{\rm avg}\ \cos(2\omega t). \tag{16}$$

However, the instantaneous buffer current is not equal to the instantaneous capacitor current, but instead to the buffer current scaled by the converter duty ratio

$$i_C = i_L = \frac{i_{\rm buf}}{d_{S1}}. \tag{17}$$

As seen from (17), the instantaneous duty ratio is required to determine the capacitor current, however the instantaneous capacitor voltage, and duty ratio is unknown without the capacitor current. Thus, it is not possible to calculate the capacitor current directly from the buffer current alone and an iterative approach must be used to combine (15) through (17) to define the relationship between capacitor voltage and current.

The change in charge stored on the capacitor (Δq) is simply the integral of capacitor current (i_C) over time

$$\Delta q = \int_0^{\Delta T} i_C\, dt. \tag{18}$$

The incremental change in voltage (Δv_C) is the change in charge divided by the buffer capacitance (C)

$$\Delta v_C = \frac{\Delta q}{C(v_C)} \tag{19}$$

where the effective capacitance of $C(V_C)$ is a function of instantaneous capacitor voltage ($v_C(t)$). By extension, the capacitor voltage can be calculated at any point in the line cycle as

$$v_C(t) = \int_0^t \frac{i_C(\tau)}{C(v_C)} d\tau + v_C(0). \tag{20}$$

Equation (20) can then be rewritten in terms of converter current through substitution of (17), which yields the capacitor voltage over time as a function of $i_{\rm buf}$ and d_{S1}

$$v_C(t) = \int_0^t \frac{i_{\rm buf}(\tau)}{C(v_C)\ d_{S1}(v_C)} d\tau + v_C(0). \tag{21}$$

Finally, (21) can be rewritten by substituting (14) to obtain

$$v_C(t) = \int_0^t \frac{i_{\rm buf}(\tau)\ V_{\rm bus}}{C(v_C)\ v_C(\tau)} d\tau + v_C(0). \tag{22}$$

Evaluating (22) in a piece-wise fashion will allow the computation of the capacitor voltage over a full line cycle, and hence the instantaneous converter duty ratio will be known. With the duty ratio and buffer current waveform defined, (17) then allows for the capacitor current and inductor current to be calculated.

B. Inductor Volume

As mentioned, the previous relationships assume that the converter inductance is large enough to operate in CCM. For a given duty ratio d_{S1}, the minimum inductance required for CCM can be calculated as

$$L_{\rm CCM} = \frac{V_{\rm bus}(1-d_{S1})d_{S1}}{\Delta I_L f_{sw}} \tag{23}$$

where $V_{\rm bus}$ is the bus voltage, ΔI the peak-to-peak current ripple, and f_{sw} the converter switching frequency. It can be seen in (23), that $L_{\rm CCM}$ has a maximum value at a duty ratio of 50%. Thus, in order to determine the minimum inductor size for each average buffer capacitor voltage and ripple voltage shown over the axes in Figs. 11 and 12, it is necessary to determine the duty ratio closest to 50% that will be used during converter operation. Based on this duty ratio, the minimum inductance required to maintain continuous conduction can be determined.

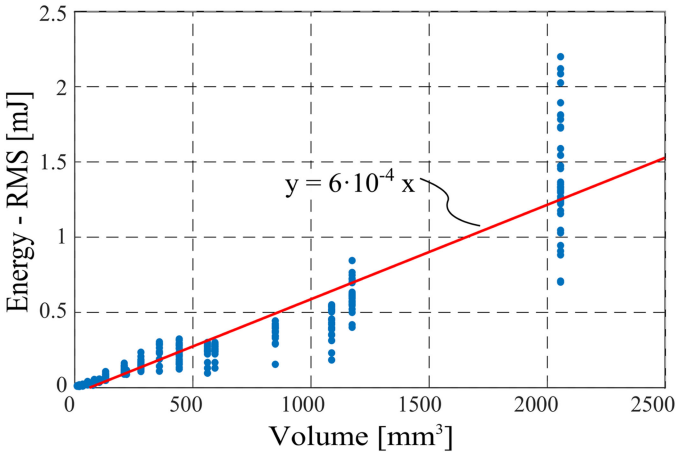

Fig. 17. RMS energy storage as a function of inductor volume for the IHLP inductor series by Vishay [35].

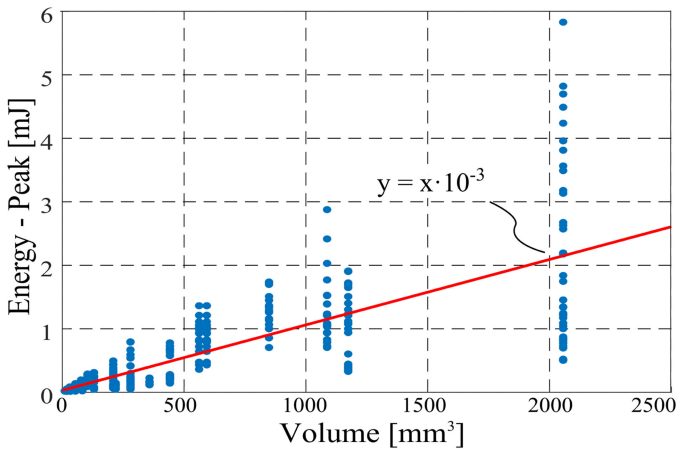

Fig. 18. Peak energy storage as a function of inductor volume for the IHLP inductor series by Vishay [35].

In order to perform a minimization of the overall system volume, it is necessary to develop a model of inductor volume as a function of inductance and current rating. In practice, these two specifications are often combined into the energy storage (W_L) rating of the inductor as

$$W_L = \frac{1}{2} L I_L^2 \tag{24}$$

for use in preliminary design analysis [34]. When considering component volume, it is important to take into account both the thermal and magnetic saturation limit of the inductor. The inductor thermal limit will set the RMS inductor current rating, and the saturation limit will set the peak inductor current limit.

In a practical implementation, the inductor volume will be determined by component availability and will not be a continuous function, but will instead be a discretized function depending on available core sizes. As an example to illustrate the discrete nature of inductor volumes and ratings as well as overall trends, Fig. 17 plots the energy storage of the high current, low profile (IHLP) product family of inductors from Vishay as a function of inductor volume. The linear fit of RMS energy stored (W_{RMS}) as a function of volume (V_L) is found to be

$$W_{\mathrm{RMS}}\ [\mathrm{mJ}] = 6 \cdot 10^{-4} \left[\frac{\mathrm{mJ}}{\mathrm{mm}^3}\right] * V_L\ \left[\mathrm{mm}^3\right]. \tag{25}$$

While a linear fit is a rough estimation of energy storage, it provides an approximate estimate of the volume requirements of existing technology. In addition to following the RMS current ratings which set the thermal limits of the inductor, the peak current rating of the inductor must also be accounted for in order to avoid saturation. Fig. 18 plots the inductor peak energy as a function of volume. The linear fit of peak energy storage as a function of volume is found to be

$$W_{pk}\ [\mathrm{mJ}] = 1 \cdot 10^{-3} \left[\frac{\mathrm{mJ}}{\mathrm{mm}^3}\right] * V_L\ \left[\mathrm{mm}^3\right]. \tag{26}$$

It is evident that the peak energy storage for a given volume is higher than the RMS energy density. What is not immediately evident is the ratio of RMS to peak current that the inductor will encounter for each design of voltage bias and ripple. Thus, in order to evaluate the energy density of a design, the volume needed to meet the RMS and peak requirements are both calculated separately and the maximum volume is chosen for each operating condition.

C. Heatsink Volume

An important final step in developing a volumetric model of the converter is to consider the volume of the cooling hardware required to dissipate converter losses. Low converter efficiency not only results in higher energy loss, but in larger required volume for cooling the converter. In this analysis, dissipation of inductor losses were accounted for by heeding the RMS ratings of the inductors, as this rating generally does not assume any type of heatsinking on the inductor. The other major source of losses occurs in the conduction and switching of the converter power switches. In this example, the switch losses for a half-bridge built of GS66508P devices from GaN Systems switching at 120 kHz were calculated and averaged over a full line cycle using a standard loss model for conduction and switching losses [36], [37].

The heatsink volume needed to dissipate the energy lost in the switches will change depending on the cooling approach (i.e., whether natural convection, forced air, or liquid cooling are used). Air cooling provides a simple baseline on which to make comparisons between designs. A thermal admittance of $0.02 - 0.03$ W/(cm^{3}K) for highly optimized air cooled systems, and $0.005 - 0.01$ W/(cm^{3}K) for more standard extruded systems was identified in [34]. In this example, a thermal admittance of 0.01 W/(cm^{3}K) was assumed as well as an ambient temperature of 30 °C and a maximum device temperature of 100 °C, or 70 °C above ambient. Under these constraints, 1428 mm^3 of heatsink volume are required per watt of loss to provide adequate cooling.

D. Design Summary

In order to develop a rough comparison of the overall volume required to build a buffer using both MLCC and bias-independent capacitors, the volume contributions outlined in Appendix B, sections A to C were totaled together for each range of capacitor average voltage and ripple voltage analyzed.

The overall power rating of the converter was then divided by the volume to determine the effective system power density. The resulting density plots are shown in Figs. 16 and 15. It should be emphasized that the purpose of this appendix is not to perform detailed loss or size calculations of power converters, but rather to inform readers of the assumptions made to determine the impact of MLCC capacitors on buffer converter power density. This calculation is not deemed to be a primary contribution of this paper.

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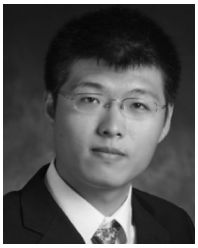

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