In-Package Common-Mode Filter for GaN Power Module with Improved Radiated EMI Performance

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***Abstract*—This paper discusses the impact of parasitic inductances on the electromagnetic interference (EMI) performance at radiated frequency and provides a new concept for high-frequency wide bandgap (WBG) power module package design with integrated π-type common mode filter (π-CMF). The connection parasitic-inductances of a π-type CMF model are analyzed, and the parasitic inductances from the CMF to the CM noise source and to the heatsink are minimized to improve the CMF's EMI performance in the radiated frequency range. Therefore, placing the π-CMF closer to the power module (i.e. in-package CMF) provides a larger noise attenuation compared to placing it outside the module (i.e. external CMF). To verify the theoretical analysis, a half-bridge GaN power module with an in-package π-CMF is designed, and experiments are conducted by comparing the attenuated noise spectrums of a 70-V/1.75-A hard-switching buck converter built by the designed module with an external CMF and the power-module integrated CMF. According to the experiment results, up to 10 dBμV more attenuation is achieved by the in-package CMF than the external CMF, validating the analytical conclusion.**

Keywords—in-package common mode filter, GaN power module package, radiated frequency, EMI

I. INTRODUCTION

As wide bandgap (WBG) devices are broadly used in power electronics applications, the system can switch at higher switching frequency and speed, which yields benefits such as reduced system size and power loss. On the other hand, the higher dv/dt during commutations will induce more noise spectrum, generating electromagnetic interference (EMI) issues [1-2]. While the noise at switching frequency and its harmonics can be suppressed by noise balancing and cancellation [3], for high-frequency noise in radiated EMI band, the cancellation model becomes inaccurate due to parasitic inductance effects. Therefore, in practice, the noise can only be effectively suppressed by filtering and shielding. Due to the greatly increased high-frequency noise spectrums, WBG system needs substantial design efforts in solving radiated EMI [4-5].

From the power module package design aspect, both reducing the noise propagation paths and adding extra filters have been explored. It is found in [4] that reducing the area of the bottom side of direct bond copper (DBC) and only keeping the effective area needed for the thermal performance, the parasitic capacitance is reduced so the EMI noise can be decreased. Integrating common-mode (CM) capacitors into a silicon carbide power module has shown improved performance for CM current reduction at the conduction frequency [5]. However, the feasibility of integrating a common mode filter (CMF) (composed of CM chokes and capacitors) has not been explored. The EMI analysis of the in-package CMF requires detailed characterization and modeling of parasitic inductances in the power electronics system, as they significantly impact the EMI at high frequency [6]-[8]. The electrical connection is one of the sources that cause parasitics and undermine the filter performance, so there have been many different equivalent circuit models built to explore the parasitics effect on the CMF performance [9]-[11].

In this paper, through the parasitic inductances analysis, common mode equivalent circuit building, line impedance stabilization networks (LISNs) voltage insertion gain calculation, and verification experiments, it is discovered that the parasitic inductances of the CMF to the CM noise source and to the heatsink significantly impact the filter's EMI performance, thus inspiring the concept of placing the CMF inside the WBG power module package to minimize the CMF-to-power-module and the CMF-to-heatsink parasitic inductances and ultimately realize a better EMI performance. In Section II, the parasitics analysis comparing an external and an in-package π-type CMF (π-CMF) and the derived LISNs voltage insertion gain equations are given. Section III introduces the designed half-bridge GaN power module package and the integrated π-CMF. Simulation

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results with corresponding parasitics values are also shown. The experimental results of the attenuated noise spectrums generated by a 70-V/1.75-A 80-kHz buck converter built by the designed half-bridge power module with an external CMF and with the in-package CMF are compared in Section IV, verifying the benefit that having a localized CMF close to the power module inside the package greatly improves the radiated EMI noise suppression.

II. Common Mode Equivalent Circuit and Theoretical Analysis

A. Parasitics Analysis

In a power conversion system, there are different parasitics that may affect the CMF's performance. Hence, addressing the main parasitics is helpful for the CM equivalent model building, theoretical analysis, and CMF performance prediction. The parasitic capacitances between the power module and the heatsink, and the parasitic inductances caused by the electrical connections are two kinds of parasitics that play important roles as the EMI propagation paths. Fig. 1(a) and (b) illustrate that in a half-bridge power module, there are three parasitic capacitances, C_P, C_N and C_{sw}, caused by the metal-ceramic-metal sandwich structure of the direct bond copper (DBC) between the heatsink and the three nodes of the power module, P, N and the switching node, respectively [4, 12-13].

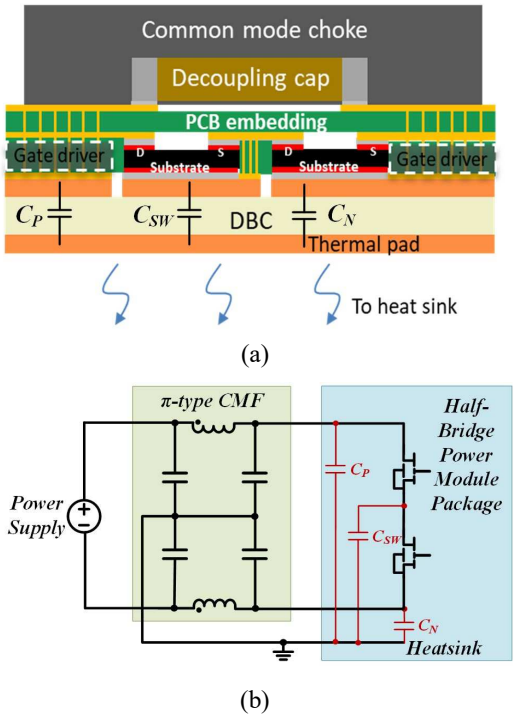


Fig. 1. (a) DBC caused parasitic capacitances in the designed half-bridge GaN power module package, (b) power module parasitic capacitances in the circuit.

For the power conversion system with π-type CMF, there are several main parasitic inductances due to the connection wires, the parasitic inductance between the LISNs and the CMF $L_{CMF\text{-}LISN}$, the parasitic inductance between the CMF and the power module (the CM noise source) $L_{CMF\text{-}PM}$, the CMF-to-heatsink parasitic inductance $L_{CMF\text{-}hs}$, and the heatsink-to-ground parasitic inductance $L_{hs\text{-}g}$, assuming that the CMF is grounded through the power module's heatsink. The corresponding CM equivalent circuit is shown in Fig. 2. C_{PN} is the sum of the paralleled C_P and C_N.

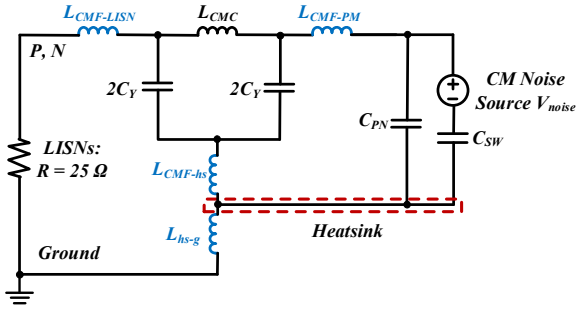


Fig. 2. CM equivalent circuit of a power conversion system with a half-bridge power module and π-CMF.

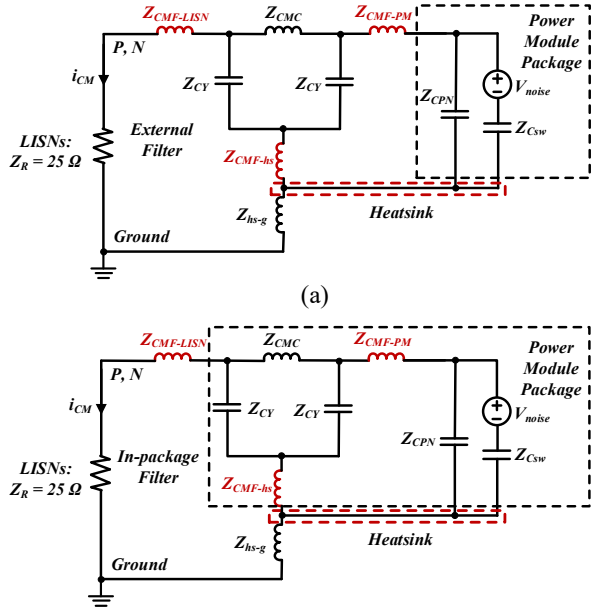


Fig. 3. (a) defined CM equivalent circuit structure for the system with an external π-type CMF, (b) defined CM equivalent circuit structure for the system with an in-package π-CMF.

Practically, the locations of the power supply, LISNs, power module and the heatsink for a certain system are assumed to be fixed. Thus, the heatsink-to-ground parasitic inductance and the total parasitic inductance between the LISNs and the power module, which is the sum of $L_{CMF\text{-}LISN}$ and $L_{CMF\text{-}PM}$, are constant, although some values of these parasitic inductances are determined by the connection and location of the CMF. Hence, this brings the concepts of external CMF and in-package CMF into consideration, placing the CMF away from the power module as the external filter or placing the CMF inside the power module package as the in-package filter. Compared to the in-package filter in Fig. 3(b), the external filter has a longer connection distance between the CMF and the power module, also the heatsink, so the values of $L_{CMF\text{-}PM}$ and $L_{CMF\text{-}hs}$ are larger.

$$Gain = \frac{Z_R \times i_{CM}}{V_{noise}} = \frac{Z_{CPN} Z_R}{(Z_{Csw}+Z_{CPN})\left(Z_{CMF-PM}+Z_{CMF-LISN}+Z_R+Z_{hs-g}+\frac{Z_{CMF-PM}\times(Z_{CMF-LISN}+Z_R+Z_{hs-g})}{Z_{CMF-hs}}\right)+Z_{Csw}Z_{CPN}(1+\frac{Z_{CMF-LISN}+Z_R+Z_{hs-g}}{Z_{CMF-hs}})} \quad (1)$$

However, $L_{CMF\text{-}LISN}$ is smaller assuming the total distance between the LISNs and the power module is fixed. When the filter is placed inside the power module package, the CMF-to-power-module and the CMF-to-heatsink wire connection lengths are minimized, resulting in smaller parasitic inductances $L_{CMF\text{-}PM}$ and $L_{CMF\text{-}hs}$ but a larger $L_{CMF\text{-}LISN}$.

B. LISNs Voltage Insertion Gain Derivation

According to Fig. 3, the voltage insertion gain of the LISNs can be calculated. Under very high frequencies (e.g., 30 MHz – 100 MHz), Z_{CMC}, the impedance of CM choke (usually around hundreds of nH to several μH) are much larger than Z_{CY}, the impedance of Y-capacitor (Ycap) (usually around several nF). Thus, $Z_{CY} = 0$ is assumed. The LISNs' voltage insertion gain, which is the noise received by the LISNs' equivalent impedance Z_R compared to the CM noise source V_{noise} generated from the power module, can be derived and simplified as (1), where i_{CM} is the CM current flowing through Z_R and all other parameters are the corresponding impedances of parasitics.

To further illustrate (1), the total sum of Z_R, $Z_{hs\text{-}g}$, $Z_{CMF\text{-}PM}$ and $Z_{CMF\text{-}LISN}$ can be written as Z_{SUM} since Z_R, $Z_{hs\text{-}g}$ and the sum of $Z_{CMF\text{-}PM}$ and $Z_{CMF\text{-}LISN}$ are all constants. The ratio of Z_{CSW} and Z_{CPN} is α and the ratio of $Z_{CMF\text{-}PM}$ and $Z_{CMF\text{-}hs}$ is η. Hence, (1) can be written as (2).

$$Gain = \frac{Z_R}{(\alpha+1)(Z_{SUM}+\eta(Z_{SUM}-Z_{CMF-PM}))+\alpha Z_{CPN}(1+\frac{Z_{SUM}-Z_{CMF-PM}}{Z_{CMF-hs}})} \quad (2)$$

For a GaN-based half-bridge power module, the normal value for the parasitic capacitance is usually around several pF due to the small dimension of the package. In this case, (2) can be further simplified as (3). In (3), there are only two variables, $Z_{CMF\text{-}PM}$ and $Z_{CMF\text{-}hs}$, suggesting that the gain reduces with the reduction of $Z_{CMF\text{-}PM}$ and $Z_{CMF\text{-}hs}$, which means that smaller $L_{CMF\text{-}PM}$ and $L_{CMF\text{-}hs}$ lead to a larger noise suppression along the propagation path so the LISNs receive lower noises. Therefore, better EMI performance can be realized by putting the CMF closer to the power module, which justifies the benefit of integrating the CMF in package with the power module.

$$Gain = \frac{Z_R}{\alpha Z_{CPN}(1+\frac{Z_{SUM}-Z_{CMF-PM}}{Z_{CMF-hs}})} \quad (3)$$

III. Designed Power Module and Integrated CMF

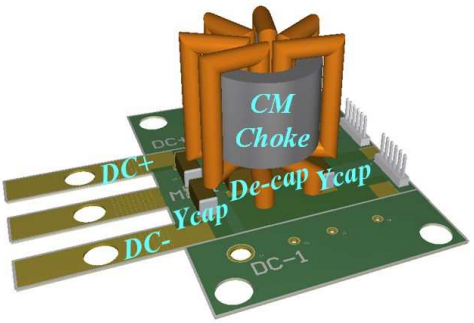
In this section, the power module and the in-package π-CMF are introduced in detail. The values of the parasitics used in the simulation are extracted through ANSYS Q3D or calculated based on the designed power module. According to the simulation results, the better EMI performance of in-package CMF is shown.

A. Designed Power Module with In-Package CMF

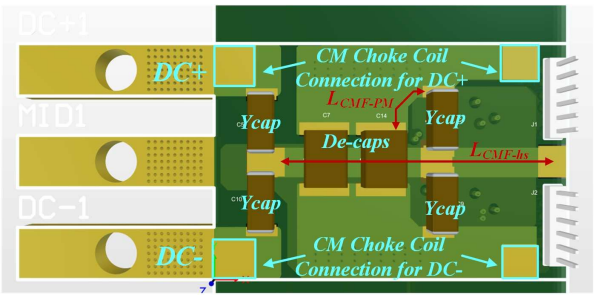
Fig. 1(a) presents the vertical cut view of the designed power module package, adopting low-cost printed circuit board (PCB) and DBC structure for double-sided cooling, embedding small GaN bare dies from GaN Systems for a vertical power loop with decoupling capacitor (de-cap), gate drivers and CMF integrated in the package to achieve a high-power-density and low-parasitics design. The dimension of the power module package is only 2.7 cm in length and 1.8 cm in width, so the power-module parasitic capacitances are small enough to use (3) to predict the CMF's performance.

The 3D view of the designed half-bridge power module package is shown in Fig. 4(a). Four Ycaps of the in-package π-CMF and the de-caps are soldered on the top side of the PCB while the GaN dies and integrated gate drivers are soldered on the bottom side of the PCB so they can be attached to the DBC for heat dissipation. The de-caps placing on the top side of the PCB are only for forming a vertical power loop with the GaN dies on the bottom side to minimize the power-loop parasitic inductance. The CM choke sits on top of the Ycaps and the de-caps. The parasitic inductances $L_{CMF\text{-}PM}$ and $L_{CMF\text{-}hs}$ of the in-package CMF shown in Fig. 4(b) are extracted by ANSYS Q3D, and other parasitic inductances for the in-package CMF, also the parasitic inductances for the external CMF and circuit without any filter are assumed for the simulation as listed in Table I. Parasitic capacitances caused by DBC are calculated by (4), where $\varepsilon_o\varepsilon_r$ is the dielectric constant of the DBC ceramic, A is the area of each DBC upper-side copper pad, d is the thickness of the DBC ceramic.

$$C = \frac{\varepsilon_o \varepsilon_r A}{d} \quad (4)$$



(a)



(b)

Fig. 4. (a) 3D view of the designed power module package, (b) parasitic inductances of in-package CMF extracted from the power module PCB.

TABLE I. PARASITICS VALUES

Parasitics Values	CMF Type		
	No CMF	*External CMF*	*Internal CMF*
$L_{CMF\text{-}PM}$ (nH)	The sum = 197 nH	116	1
$L_{CMF\text{-}LISN}$ (nH)		81	196
$L_{CMF\text{-}hs}$ (nH)	N/A	180	9
$L_{hs\text{-}g}$ (nH)	140	140	140
C_{SW} (pF)	14.01	14.01	14.01
C_{PN} (pF)	25.87	25.87	25.87
L_{CMC} (μH)	N/A	2	2
C_Y (nF)	N/A	1	1

B. Simulation Verification

In Fig. 5, the results of the simulation using the parasitics values listed in Table I show the EMI noises of the common-mode voltage measured from the equivalent impedance of the LISNs of a 70-V 80-kHz buck converter with no CMF, with an external π-CMF, and with an in-package π-CMF. More attenuation is achieved by the in-package CMF. The EMI noise increase of the converter with the external filter above 60 MHz is caused by the resonance of the CMF-connection parasitic inductances and the power-module parasitic capacitances.

The attenuation difference between the EMI spikes of the circuit with an external CMF and with an in-package CMF matches the LISNs' voltage insertion gain difference of the two CMFs calculated by (1) in Fig. 6, also confirming the correctness of the equation.

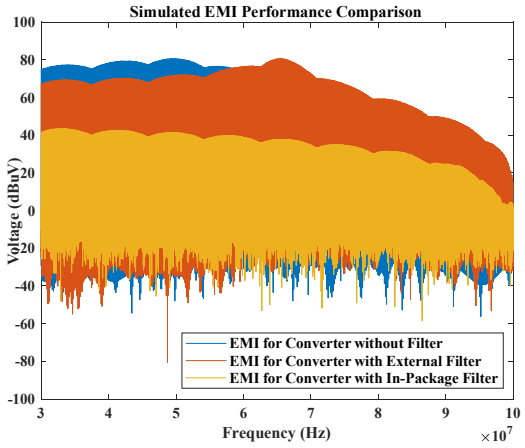


Fig. 5. EMI simulation comparion of the converter with no filter, with an external filter and with an in-package CMF under 70 V 80 kHz.

IV. EXPERIMENTAL VERIFICATION WITH THE DESIGNED POWER MODULE

The prototypes of the in-package π-CMF integrated with the designed half-bridge GaN power module and the external π-CMF are shown in this section. The experimental EMI spectrums of a 70-V/1.75-A 80-kHz hard-switching buck converter with the duty cycle of 0.5 built by the designed power

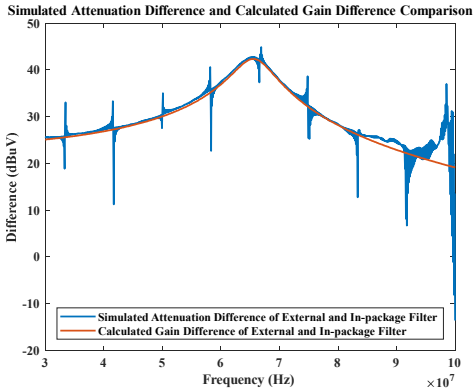
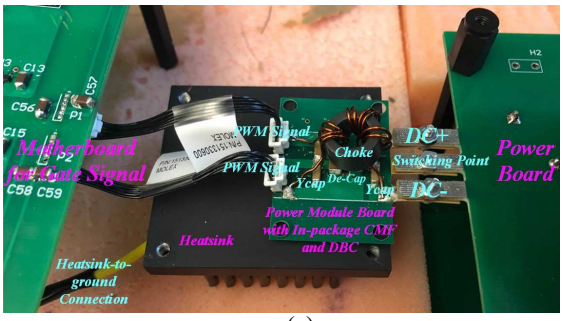


Fig. 6. Simulated attenuation difference and calcualted gain difference comparison.

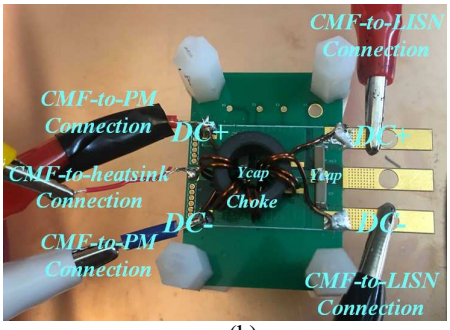
module without CMF, with the external CMF and with the in-package filter confirm the proposed conclusion.

A. Prototype of the External and In-package π-CMF

The prototypes of the designed power module with integrated CMF and the external CMF are shown in Fig. 7(a) and (b). For the in-package π-type CMF, the choke and the Ycaps are soldered directly on the power module board. DC voltage first goes through a power board including the energy storage capacitors connected after the LISNs then to the power module board. The same choke and Ycaps are soldered on an empty PCB to be used as the external CMF, which is connected between the LISNs and the power board, so the distance between the CMF and the power module is increased. The parasitic inductances of the connection wires are measured by impedance analyzer before the EMI test as Table I shows.



(a)



(b)

Fig. 7. (a) prototype of the designed power module with the in-package CMF, (b) prototype of the external CMF soldered on an empty power module PCB.

The specifications of the choke and the Ycaps are listed in Table II. The self-resonant frequency of the choke is 145 MHz, higher than the concerned frequency range of 30 to 100 MHz.

TABLE II. CHOKE AND YCAP SPECIFICATIONS

Specifications	Choke	Specifications	Ycap
Core Part Number	5961001101 Toroid Core, Ferrite 61 Material	Part Number	GA342DR7G F102KW02L
Core Dimension	Outer Diameter (mm): 12.70	Capacitance	1 nF
	Inner Diameter (mm): 7.90		
	Height (mm): 6.35		
Electrical Properties	A_e (cm^2): 0.15	Voltage Rating	250 Vac
	l_e (cm): 3.12		
	V_e (cm^3): 0.47		
Turns per side	4	Package	1808
Inductance per side	2 μH		
Resonant Frequency	145 MHz		

B. *Experimental EMI Results*

Fig. 8 is the EMI experiment setup. The experimental EMI results of the 70-V/1.75-A 80-kHz buck converter based on the designed power module without any filter, with the external CMF, and with the in-package CMF are shown in Fig. 9. From the EMI results, it can be concluded that both the external π-CMF and the in-package π-CMF have generally realized the EMI noise attenuation over the frequency range of 30 to 100 MHz. Moreover, up to around 10 dBμV more attenuation can be achieved by the in-package π-CMF with the same choke and Ycaps as the external π-CMF, validating the benefit of the in-package CMF for this GaN-based half-bridge power module.

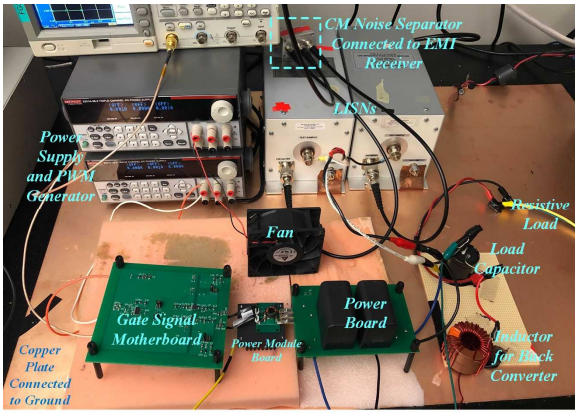


Fig. 8. EMI test setup for the 70-V 80-kHz buck converter.

CONCLUSION

This paper proposed a design concept of the GaN-based half-bridge power module package that shows integrating a π-type CMF into the half-bridge power module package achieves higher EMI attenuation at radiated frequencies than by placing the CMF externally. Through the analysis of the impact of different connection parasitic inductances on the noise reduction performance of common-mode filters, the CM equivalent circuit of a half-bridge power module was built and the equation of the voltage insertion gain on the LISNs was derived and analyzed. The theoretical analysis shows that by minimizing the parasitic inductances of the CMF to the power module and to the heatsink, the performance of the CMF is improved and more attenuation can be achieved at the high frequency range, which justifies the advantage of using an in-package π-type CMF.

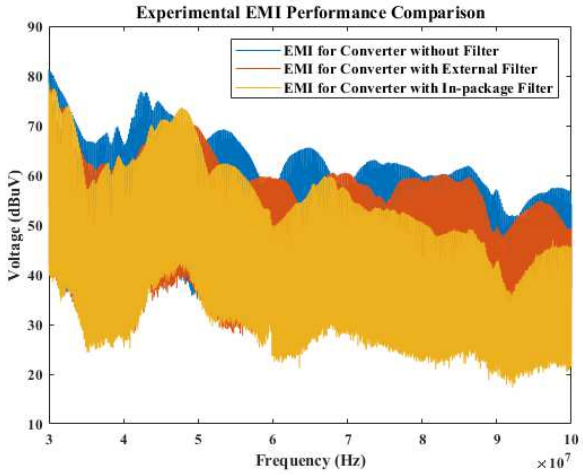


Fig. 9. Comparison of EMI results tested by converter without filter, with the external CMF and with the in-package CMF.

A half-bridge GaN power module package was designed for validation. The proposed conclusion was verified by the comparison of the EMI results of a 70-V/1.75A 80-kHz hard-switching buck converter built by the designed power module without a filter, with an external π-CMF, and with an in-package π-CMF. Up to around 10 dBμV more attenuation achieved by the in-package CMF than the external CMF indicates that the in-package π-type CMF shows a better EMI attenuation than the external filter under the frequency range of 30 to 100 MHz, and validates the proposed power module package design concept.

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