# Dynamic Performance Comparison and Prediction based on Distribution-level Phasor Measurement Units

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*Abstract*—This paper introduces a new distribution level Phasor Measurement Unit (PMU) which adopts advanced hardware components and structure. The hardware parameters from the new PMU and the existing PMU are used to build a simulation model to predict the PMU performance. Therefore, a real-world testbench is built and four distribution level PMUs are tested under the steady-state and dynamic tests. The quantitative experiment result confirms the prediction model which could guide future PMU design, and also verifies the accuracy of the new PMU on the synchrophasor and frequency measurements in multiple scenarios.

*Index Terms*—Phasor measurement units, error prediction, dynamic performance

## I. INTRODUCTION

The technology of phasor measurement units (PMUs) has rapidly grown in recent years, and the PMUs are being integrated into the power system for multiple purposes [1]. The monitoring [2], protection [3] and control [4] of the transmission grid have been benefited from the implementation of PMUs operating in real-time. However, a majority of PMUs installed at transmission level requires high cost for installation and production and the deploy position is limited in the substations [5]. In contrast, distribution level PMUs are designed for distributional power grid with low installation and production cost features [6]. Distribution level PMUs can be easily deployed in any place with 120V or 220V residential power supply, as an extension of the grid wide-area monitoring system (WAMS).

There are multiple distribution level PMUs in practical applications such as the commercial distribution level PMU [7], the microPMU [8] and the field programmable gate array (FPGA) based PMU [9]. Besides them, a family of distribution level PMUs have been developed by the frequency monitoring network (FNET) and are used to construct a FNET/Grid-eye monitoring system [10]. In the FNET monitoring system, more than 200 PMUs distributed worldwide are transmitting synchrophasor data to the FNET servers hosted at the University of Tennessee, Knoxville (UTK) via Internet. This PMU family includes the frequency disturbance recorder (FDR) [11], and

an improved version of FDR, the universal grid analyzer (UGA) [12]. With the synchronization from global positioning system (GPS), the FDR and UGA have a precise timestamp to measure the frequency and synchrophasor from one-phase signal [13]. Moreover, the UGA has higher synchrophasor accuracy and the ability to estimate the power quality factors in real-time, such as harmonics, Sags, Swells, signal to noise ratios (SNRs) and voltage flickers [14].

In this paper, a new distribution level PMU named the Ultra-high resolution Synchrophasor Recorder (USR) has been developed with advanced hardware and structure. The hardware update of the USR can reduce the timing error and quantization error in the data sampling, and the new structure expands the functionality in communication. As the next generation of the UGA, those updates could increase the measurement accuracy, but the degree of improvement about the performance should be predictable. Therefore, a PMU performance prediction based on hardware parameters is simulated and applied to the UGA and USR. To verify the performance estimation, a real world testbench has been built and four different distribution level PMUs are tested simultaneously. The test scenarios contain both steady-state and dynamic conditions defined by the PMU standard IEEE C37.118.1 [15]. The experiment result matches the performance prediction of the UGA and USR, and also verifies the high accuracy of the USR on the synchrophasor and frequency measurements in all scenarios.

This paper is organized as follows. The hardware comparison between PMUs is introduced in Section II. The compliance verification and testbench design are presented in Section III. Section IV demonstrates the error prediction about performance. Experimental results are shown and discussed in Section V. Section VI summarizes the key points in this paper.

## II. HARDWARE COMPARISON

The hardware of the USR consists of two parts, the computation-control core and the support modules. The major difference between the USR and UGA is the redesign of the computation-control core, which modifies the hardware

structure. In the previous design of the UGA, the measurement computation and data transmission are processed in two separate chips, a digital signal processor (DSP) and an advanced RISC machine (ARM). The data flow from the DSP to ARM is strictly defined, which limits the available data for reporting. Instead of the DSP-ARM design, the USR adopts an ARM-based system-on-a-chip (SoC) as its main control unit and migrates the computation function to this SoC. Due to the high performance of the SoC, the raw voltage samples can be instantly analyzed in the SoC and used for the computation of synchrophasor measurements and power quality factors. The SoC also handles the data package following the IEEE C37.118.2 Data transfer standard [16] and the Ethernet communication with the phasor data concentrators (PDC), and allows the USR to support data reporting in user-defined mode. Since all measurements and raw samples are already in the memory of the SoC, the SoC can directly select the required value and reorganize the data frame according to the received command from PDC. As a result, the user can enable or disable the reporting of the point on wave (POW) data or any other available power quality factors by sending different pre-defined commands.

The support modules of the USR consist of a GPS receiver for synchronization, an Anti-aliasing filter, an Analog to Digital converter (ADC) for data acquisition, a high frequency oscillator for sampling control, and an Ethernet module for data transmission. Those components are all updated to new hardware with better performance.

Table I shows the important hardware updates from the UGA to the USR in detail. The memory size of the SoC is 4 times that of the DSP, which allows a larger computation window in FFT and supports more power quality factors. For instance, the voltage flicker estimation function in the UGA consumes too much storage space and prohibits more factors working together, but it is not a problem in the USR.

The updates of other modules also improve the measurement accuracy, especially the update from 16-bits ADC to 24-bits ADC. The numeral range of sampled raw voltage expands 256 times, which gives a fine resolution to the raw data. Attributed to this 24-bits ADC, the maximum quantization error in the USR for a $\pm120$V input signal is reduced to $14.2\mu$V from 3.7mV in the UGA.

The decrease of GPS timing error and the increase of oscillator frequency both reduce the timing uncertainty in the data acquisition. In the UGA and USR, the sampling in

ADC is controlled by the sampling pulses. Given a target sampling rate $f_s$ at 5760Hz, each sampling pulse must wait multiple oscillator periods to be generated, and the ideal waiting number $N_I$ is normally a fraction.

$$N_I = \frac{f_{osc}}{f_s} \tag{1}$$

where $f_{osc}$ is the oscillator frequency. If $N$ is selected as $\lceil N_I \rceil$ or $\lfloor N_I \rfloor$, the timing error of the $n$th sample can be write as:

$$T_{error}^{(1)}(n) = \frac{|N_I - N|}{f_{osc}} \times (n - 1) \tag{2}$$

Therefore, a method adjusting the period selection between $\lceil N_I \rceil$ and $\lfloor N_I \rfloor$ was proposed [12], which could eliminate the accumulated timing error. The timing error due to the $f_{osc}$ becomes:

$$T_{error}^{(1)} = \frac{1}{2f_{osc}} \tag{3}$$

Meanwhile, the sampling of this second begins when the pulse per second (PPS) from the GPS is received and then stops when the next PPS arrives. The time interval between two PPSs is defined as "1 second". The ideal sample period should be $\frac{1second}{f_s}$. If the GPS timing error is introduced, the "1 second" would increase the amount of GPS timing error and the timing error due to GPS is:

$$T_{error}^{(2)} = \frac{GPS_{error}}{f_s} \tag{4}$$

Considering (3) and (4), the total timing error of data sampling can be represented as:

$$T_{error} = T_{error}^{(1)} + T_{error}^{(2)} \tag{5}$$

In the UGA, the maximum $T_{error}$ is 10.1ns which leads to $2.2 \times 10^{-4}$ degree angle error. By adopting the advanced hardware, the USR reduces these errors to one-third, 3.5ns timing error and $7.5 \times 10^{-5}$ degree angle error.

## III. COMPLIANCE VERIFICATION AND TEST SCENARIOS

The compliance verification of a PMU has been defined by the IEEE C37.118.1 standard [15] and several important evaluation metrics are proposed. A synchrophasor is represented as:

$$\vec{x} = Xe^{j(2\pi ft + \phi)} \tag{6}$$

where $X$ is the amplitude, $f$ is the frequency and $\phi$ is the phase angle. The metrics for frequency evaluation include the frequency error (FE), the rate of change of frequency (ROCOF) and the ROCOF error (RFE).

$$FE = |f - f_{gt}| \tag{7}$$

$$ROCOF = \frac{df(t)}{dt} \tag{8}$$

$$RFE = |ROCOF - ROCOF_{gt}| \tag{9}$$

The subscript $gt$ represents the ground truth value of a signal in specific test scenario. The amplitude and phase differences

TABLE I
HARDWARE UPDATION FOR THE UGA AND USR

| Module Name | UGA | USR |
|---|---|---|
| GPS timing error | 20 ns | 15 ns |
| ADC resolution | 16 bits | 24 bits |
| Oscillator frequency | 50 MHz | 144 MHz |
| CPU Memory size | 16 MB | 64 MB |

Fig. 1. Testbench and diagram illustration



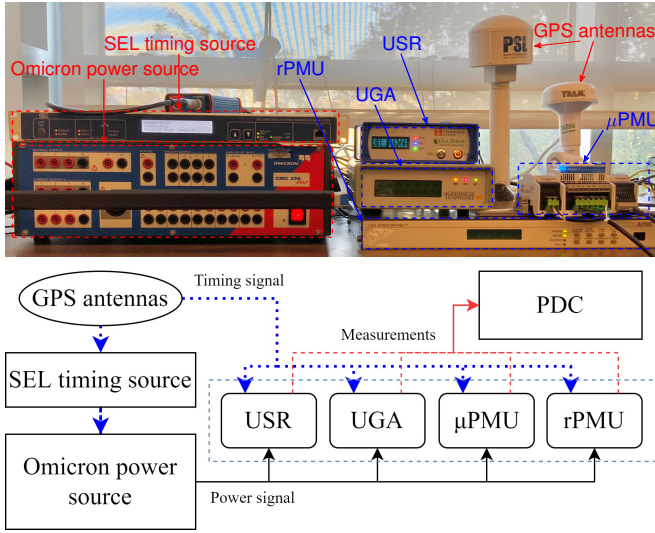Fig. 2. (a) Simulation TVE of UGA and USR in steady-state (b) The $f_{osc}$ and (c) bits number vs the simulation TVE in steady-state

are evaluated together by a synchrophasor metric, the total vector error (TVE).

$$TVE = \frac{|\vec{x} - \vec{x}_{gt}|}{|\vec{x}_{gt}|} \quad (10)$$

where $\vec{x}$ is the measured synchrophasor and $\vec{x}_{gt}$ is the ground truth value of the synchrophasor.

To be compliant with the standard, all the above metrics from the measurements of a PMU should meet the requirements. The standard also defines several test scenarios for compliance, steady-state, frequency ramp, step change of phase and magnitude, and modulation test. Each test scenario has specific requirements for FE, ROCOF, RFE and TVE, which will be compared in the experiment result section. Specially, the step change scenario introduces two metrics, measurement response time and delay time, used to identify the PMU response speed.

In order to demonstrate the performance of the UGA and USR, two other distribution-level commercial PMUs are introduced, a microPMU ($\mu$PMU) [8] and a rack-mountable PMU (rPMU) [7]. A real-world testbench has been built in the lab, as illustrated in Fig.1. The Omicron power source generates test signals according to the test scenario. The generated power signal, marked with black solid line in the diagram, is connected to the signal inputs of four PMUs in M class. Meanwhile, several GPS antennas and a SEL timing source are utilized to provides timing signal to the Omicron power source and the PMUs for synchronization, which are indicated by blue dotted line. All PMUs receive the power signal and report measurements to a PDC simultaneously. The report rates of all PMUs are configured to 60 frames per second because the change of the dynamic test happens in a short period of milliseconds level.
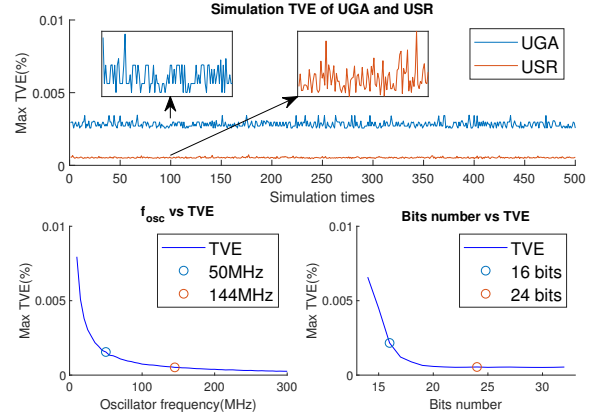
## IV. PERFORMANCE PREDICTION

Since the timing error and quantization error are calculated from the hardware parameters, the synchrophasor estimation error caused by them can be analyzed. Considering the existence of noise from the data acquisition, a synchrophasor can be represented as:

$$\vec{x}_n = X e^{j(2\pi f(t+T_{noise})+\phi)} \quad (11)$$

where $T_{noise}$ is a white noise signal, and their variances are selected as $T_{error}$ to simulate the error from timing. Applying a quantization function to $\vec{x}_n$, the quantized synchrophasor $\vec{x}_q$ equals to $[\vec{x}_n]$ and the data range is [$-2^{bits-1} + 1$, $+2^{bits-1}$]. By comparing the quantized synchrophasor $\vec{x}_q$ and the synchrophasor $\vec{x}_{gt}$, a simulated TVE is generated. As shown in Fig.2 (a), choosing the parameters of the UGA and USR, the average values of Max TVE in steady-state from 500 times simulation are $2.82 \times 10^{-5}$ and $5.31 \times 10^{-6}$, respectively. The quantization effect can be clearly observed in the enlarged plot of the UGA but it is invisible in the USR, because the higher bits of the sampler introduces less quantization error.

Fig.2 (b) and (c) indicate how the change of $f_{osc}$ and ADC bits number affect the synchrophasor estimation. Obviously, the increase of bits number from 14bits to 20bits quickly reduces the synchrophasor error, but the benefit of further employing higher bits of ADC is limited. Otherwise, the benefit of increasing the oscillator frequency is still worthy in current condition.

## V. EXPERIMENT RESULT AND ANALYSIS

### A. Steady-state scenario

In the steady-state scenario, the power source generates an ideal signal with nominal amplitude and frequency, and synchronized phase for testing.

$$\vec{x}_{gt} = X_0 e^{j(2\pi f_0 t + \phi_0)} \quad (12)$$

where $X_0$, $f_0$ and $\phi_0$ equal 120V, 60Hz and zero degree, respectively.
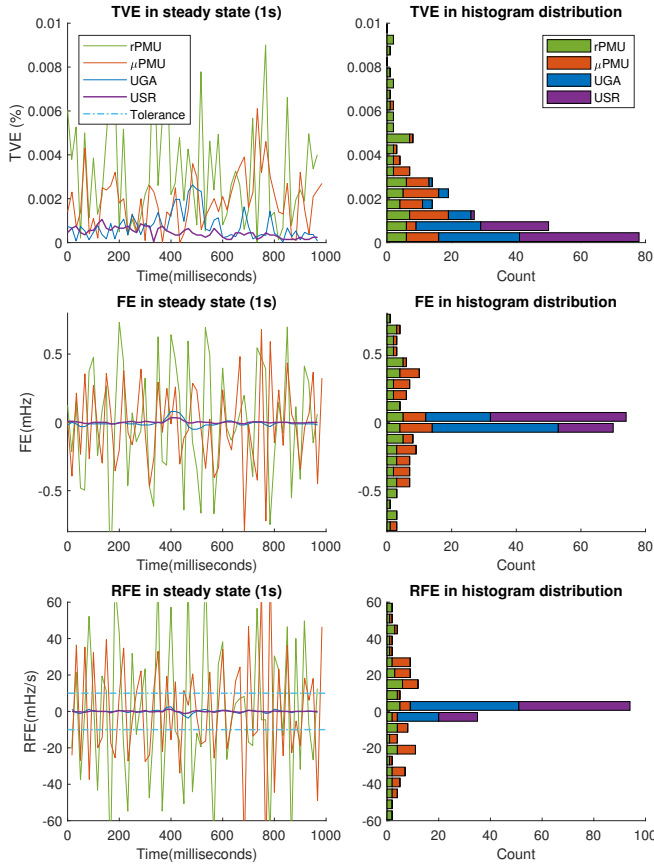
Fig. 3. The result and distribution of TVE, FE and RFE in steady-state test

Fig.3 shows the TVE(a), FE(b) and ROCOF(c) results calculated from the measurements of PMUs in the left column, and their stacked histogram distribution in the right column. The observation window length is marked in the title, and the results from different PMUs are depicted by distinct colors for visualization. Table II specifies the maximum error requirements for compliance from IEEE C37.118.1 standard in steady-state and corresponding metrics from PMUs. If the maximum error requirements are comparable to the results, they will be marked as "Tolerance" and drawn in a dotted line like Fig.3(c).

In the histogram distribution diagrams of Fig.3, 20 linear bins are used to categorized the results from PMUs. While the results of rPMU and $\mu$PMU have relative evenly distribution, the errors of the USR are concentrated in a very narrow range.

TABLE II
METRICS COMPARISON OF STEADY-STATE

| Metric (Unit) | Standard | UGA | USR | rPMU | $\mu$PMU |
|---|---|---|---|---|---|
| Max TVE(%) | 1.0 | 2.63e-3 | 1.06e-3 | 9.13e-3 | 6.10e-3 |
| Max FE(mHz) | 5.0 | 0.08 | 0.034 | 0.732 | 0.793 |
| Max RFE(mHz/s) | 10.0 | 3.72 | 1.2 | 86.04 | 84.01 |

Although all PMUs satisfy the TVE and FE requirements, the Max TVE and Max FE of USR are almost 80% and 95% less than two commercial PMUs respectively. As shown in Fig.3(c), only the UGA and USR satisfy the RFE requirement, which demonstrates the accuracy of frequency measurement algorithm in steady-state. Moreover, with the updated hardware, the USR has improved at least 50% on all metrics compared with the UGA.

Furthermore, considering the simulation result from performance prediction, the simulated TVE of the UGA is very approximate to the TVE of the UGA from experiment, which confirms the timing error and quantization error are the majority of the error of the UGA. For the USR, the value of simulated TVEs is 50% of the actual TVE. Since the bits number of the USR is larger than the UGA, it is reasonable that the quantization error is smaller and other unpredicted noises become significant. To perform better prediction, more error analyses should be considered.

### B. Step change of phase and amplitude

Following the standard, the step change test is actually a combination of two steady-states with nominal frequency, which have $\pm 10\%$ amplitude difference or $\pm 10°$ phase angle difference.

$$\vec{x}_{gt} = X_0[1 + k_x u_1(t)]e^{j[2\pi f_0 t + k_a u_2(t)]} \quad (13)$$

where the amplitude modulation parameter $k_x$ equals $\pm 10\%$, the phase angle modulation parameter $k_a$ equals $\pm 10°$, $u_1(t)$ and $u_2(t)$ represent two separate unit step functions.

The delay time is defined as the time interval between the occurrence of the step and the time when the testing value reaches 50% of the final value. The response time is the time when the metrics start exceeding the requirements of steady-state (TVE< 1%, FE<5mHz and RFE<10mHz/s) to the time when the metrics are lower than the limitation. Since the step can occur in any moment of one reporting interval $T_r$, the error of time estimation may be up to the reporting interval 16.67ms. To minimize this error, a fine time resolution is required and a series of time shifting step signals are designed. Each step change happens after the beginning of a second and lasts for two seconds. With a slight time delay, the occurrence time of the $n$th step can be represented as:

$$T_{occur}(n) = t_{begin} + (n-1) \times \frac{T_r}{N} \quad (14)$$

where $t_{begin}$ is the beginning of a second, and resolution fraction number $N$ is set to 10 according to the standard. Hence, the time resolution is reduced to 1.667ms and the minimum delay time can be identified.

The minimum delay time indicates the PMU sampling begins just after the step change happens. The sampled data at this moment can best reflect the PMU response to the step change. The minimum response time and the minimum delay time from two step tests, abbreviated as $RT$ and $DT$, are summarized in Table III. Fig.4 shows the detailed results from the USR and the $\mu$PMU at respective minimum delay

TABLE III
METRICS COMPARISON OF STEP CHANGE

| Step type | Metric (Unit) | UGA | USR | rPMU | $\mu$PMU |
|---|---|---|---|---|---|
| Phase angle | $DT$(ms) | 4.60 | 2.21 | 1.61 | 4.16 |
| | $RT_{TVE}$(ms) | 121.7 | 125.68 | 30.82 | 29.73 |
| | $RT_{FE}$(ms) | 128.56 | 124.32 | 78.76 | 182.47 |
| | $RT_{RFE}$(ms) | 0.16 | 129.66 | 232.52 | 344.22 |
| Amplitude | $DT$(ms) | 2.38 | 3.40 | 2.55 | 5.10 |
| | $RT_{TVE}$(ms) | 53.74 | 79.40 | 26.15 | 7.31 |
| | $RT_{FE}$(ms) | 0 | 40.06 | 4.63 | 140.84 |
| | $RT_{RFE}$(ms) | 127.84 | 95.07 | 230.21 | 290.52 |



Fig. 4. USR and $\mu$PMU response in phase angle and amplitude step change

time in two step tests. Different symbols are selected to avoid misleading. The step occurrence is marked by a red downward triangle, and the $50\%$ of the final value is marked by a yellow upward triangle. Since the $50\%$ of the final value may not exist in the actual samples, a linear interpolation is applied to the result and provides the most accurate delay time estimation. The observation window length is reduced to 0.5s to clearly show data points around the step occurrence. Respectively, the response time of TVE, FE and RFE are marked by the purple asterisk, green circle and magenta cross. Compared with the $\mu$PMU, the phasor response time of the USR in the phase angle step is relatively longer due to the $-1.3°$ overshoot, but the frequency and ROCOF response time are much shorter because of the accurate frequency measurement in the steady-state. In the amplitude step change, since the USR adopts 6 cycles data to estimate the amplitude, the gradient of amplitude is lower and also minimizes the overshoot to $-0.027$V. Correspondingly, the response times of the USR is reduced.

According to the requirement of M class PMU, the maximum absolute value of the delay time is 4.2ms, and the response time of TVE, FE and RFE for 60Hz reporting rate should be less than 79ms, 120ms and 129ms respectively. The delay times of all PMUs are smaller or closed to the requirements, which can be further minimized by approaching higher time resolution. The phasor response times of the UGA and USR in phase angle step change are higher than 79ms due to the overshoot, but the response times in amplitude step change are within the threshold. The frequency and ROCOF response times are varied for different PMU. Since the max RFE of the rPMU and the $\mu$PMU in steady-state already exceed the RFE requirement, the RFE response times of these two PMUs are significantly higher than the threshold. Meanwhile, the USR and UGA have all frequency[1] and ROCOF response times under the requirements of the standard.

### C. Frequency ramp

In the frequency ramp scenario, the recommend ramp rate $R_f$ is $\pm1Hz/s$ and the ramp range for M class is $\pm5Hz$. The

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[1]Specifically, the maximum FE of UGA during amplitude step change is 4.2mHz, which result in zero frequency response time under 5mHz criteria.
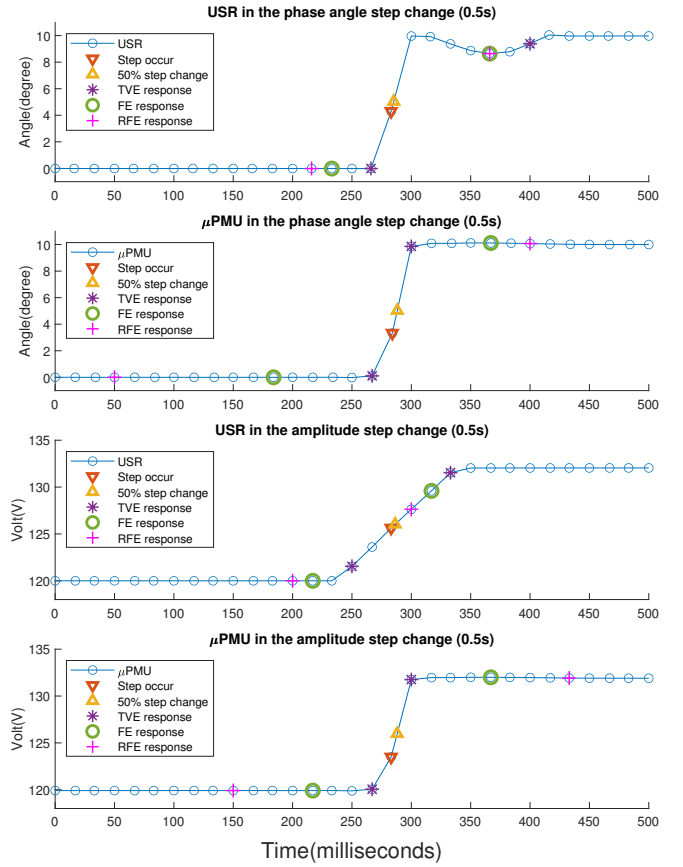
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test signal and corresponding frequency can be expressed as:

$$\vec{x}_{gt} = X_0 e^{j(2\pi f_0 t + \pi R_f t^2)} \tag{15}$$

$$f_{gt} = f_0 + R_f t \tag{16}$$

The test signal is generated by the power source and the frequency of test signal is displayed in Fig.5(a) as a reference. With the stable $\pm1Hz/s$ ramp rate, the signal frequency started from nominal 60Hz is increased to 65Hz, then reduces to 55Hz, and finally returns to 60Hz. Since the power source cannot perform the frequency perfectly at the frequency turning point as shown in the Enlarged plot of Fig.5(a), the frequencies at the $R_f$ change points are not exactly 60Hz, 65Hz and 55Hz, resulting in a sudden high FE and RFE for all PMUs. The following three diagrams are showing TVE(b), FE(c) and RFE(d) from the PMUs, and also the tolerance.

Except the Rf change points, the USR maintains very low errors on all the metrics consistently. The maximum TVE, FE and RFE of USR in frequency ramping are $0.39\%$, 0.966mHz and 43.8mHz/s respectively, which are much smaller than the requirements (TVE$< 1\%$, FE$<$5mHz and RFE$<$100mHz/s). The ability of USR to measure the off-nominal frequency in dynamic state is verified. The high RFE and FE of the rPMU indicate its frequency estimation may be unsuitable for rapid ramping frequency.
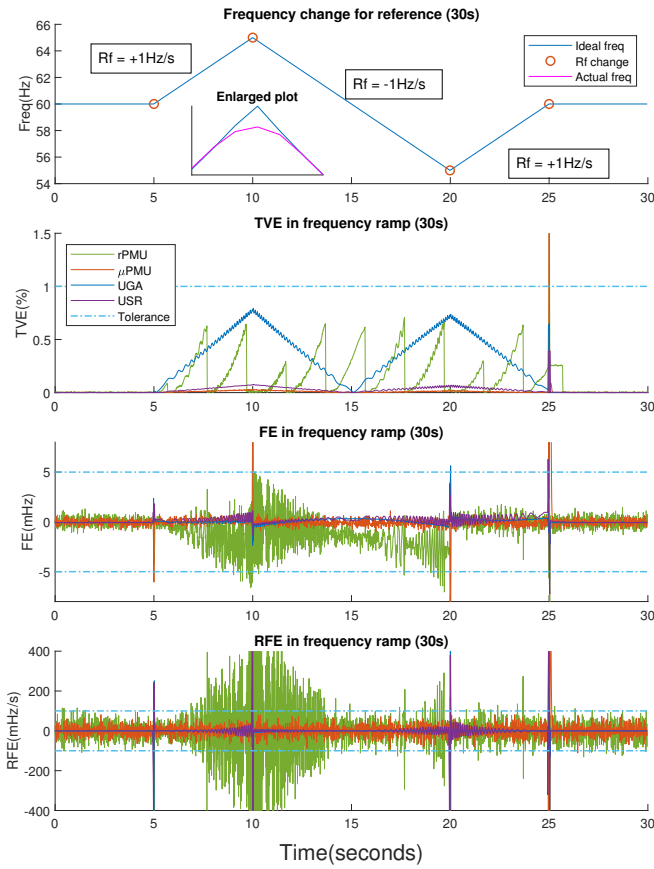
Fig. 5. Reference frequency, TVE, FE and RFE in frequency ramp test
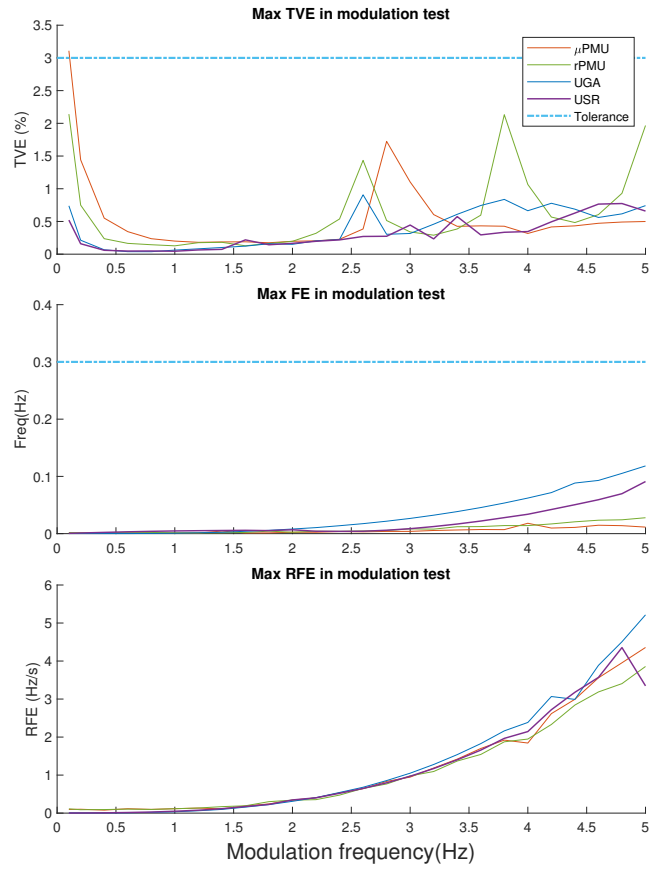


Fig. 6. Max TVE, FE and RFE in modulation test

## D. Modulation test

The aim of the modulation test, also called measurement bandwidth, is to determine the synchrophasor bandwidth by modulated sinusoidal phase angle and amplitude signal. The modulated signal can be represented as:

$$\vec{x}_{gt} = X_0(1+k_x \cos 2\pi f_m t) \times e^{j[2\pi f_0 t+k_a \cos(2\pi f_m t-\pi)]} \quad (17)$$

where $f_m$ is the modulation frequency. These modulation parameters, $k_x$ and $k_a$, are set to $10\%$ and 0.1 radian respectively. According to the standard, the modulation frequency should be varied from 0.1Hz to 5Hz with 0.2Hz difference in each round, therefore total 26 modulation test signals are generated.

As shown in Fig.6, all PMUs satisfy the requirements about frequency (max FE<0.3Hz and max RFE<30Hz/s), but the rapid frequency change of high modulation frequency leads to the increasing of the FE and RFE. Similarly, the high modulation frequency also affects the amplitude and phase estimation and causes occasional high TVE of rPU and $\mu$PMU. Although most PMUs satisfy the $3\%$ TVE requirement, the TVE result at low modulation frequency is slightly higher, because the long periods up to 10s amplify any mismatch of phase angle.

## VI. CONCLUSION

In this paper, a series of PMUs are compared from the hardware ability to the performance under the steady-state and dynamic tests following the IEEE C37.118-1 standard. In all test scenarios, the measurements accuracy of the USR on frequency and synchrophasor measurement is proved. During the tests, the USR consistently maintains much lower frequency error and ROCOF error than the requirements of the standard and other PMUs, especially the steady-state. Meanwhile, the synchrophasor estimation of the USR is closed to the ground truth value of the test synchrophasor, resulting in relatively low TVE. This satisfactory performance benefits from the hardware improvement. Since the computation algorithms of the USR and UGA are basically the same, the reducing of error metrics directly reflects the effect of updates. An error analysis based on data sampling is applied to the UGA and USR and is verified by the experiment result. It reveals the relationship between PMU performance and hardware capabilities and is applicable to all PMUs. Furthermore, a complete model is under development and will be used for completed sensitivity analysis which can guide future PMU design.

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