Decoupled Modulation With Common-Mode Load-Voltage Control for Three-Phase Four-Leg Three-Level Inverter

Li Zhang, *Senior Member, IEEE*, Haoxin Yang, Yi Tang, *Senior Member, IEEE*, Josep Pou, *Fellow, IEEE*, and Leon M. Tolbert, *Fellow, IEEE*

***Abstract*—Three-phase four-leg four-wire (3P4L4W) three -level (3L) inverters have the ability to supply both balanced and unbalanced loads. This letter establishes common-mode (CM) and differential-mode (DM) circuit models for the 3P4L4W 3L inverter. It is revealed that the 3L phase-leg CM voltage is determined by the voltage balancing control (VBC) for the split dc bus voltages, that the DM load voltages are subject to the DM voltage control for the 3L phase leg, and that the CM load voltage is subject to the control for the fourth phase leg. On this basis, a decoupled modulation is proposed where the 3L phase legs are modulated to attain VBC and closed-loop DM load-voltage control, whereas the fourth phase leg is independently modulated to realize the closed-loop CM load-voltage control. The proposed work has been experimentally verified, showing that the 3P4L4W 3L inverter with this decoupled modulation scheme can provide well-balanced ac load voltages and low total harmonic distortion for any type of ac loads: balanced, unbalanced, linear, and nonlinear.**

***Index Terms*—Closed loop, common mode (CM), differential mode (DM), four-leg four wire, three level, three phase.**

I. Introduction

THREE-LEVEL (3L) inverters have been fashionable in high-voltage and high-power industrial applications over the past few decades [1]–[4]. The basic three-phase three-leg three-wire (3P3L3W) 3L inverter is only effective for feeding balanced ac loads. In the presence of unbalanced and/or nonlinear ac loads, however, a neutral wire is required to create the flow for the zero-sequence load current [5].

The three-phase four-leg four-wire (3P4L4W) 3L inverter circulates the neutral current by a fourth phase leg. Compared with the three-phase three-leg four-wire (3P3L4W) 3L inverter [6], the size of the dc bus capacitor bank is significantly reduced because the split-capacitor leg does not need to carry the neutral current [7], [8].

The modulation scheme is one of the most critical challenges that should be addressed for 3P4L4W 3L inverters. The most popular one is the three-dimensional space-vector modulation (3D-SVM) [9]–[11], which allows complete control of the common-mode (CM) and differential-mode (DM) parts in the three-phase load voltages. Although effective, the 3D-SVM itself is complex for implementation because of the computational demands for processing numerical voltage vectors [12], [13]. By independently modulating the fourth phase leg with an offset zero-sequence voltage, the carrier-based modulation successfully decouples the modulation of the fourth phase leg from that of the remaining three phase legs, significantly simplifying the implementation complexity [14]. Nonetheless, the offset zero-sequence voltage, which is specifically designed for benefitting the inverter with higher dc-link voltage utilization [15], reduced switching losses [16], or lower electromagnetic interference noises [17], is online calculated in an open-loop manner leading the CM part in the three load voltages to be open-loop regulated. As a result, the load voltages might be unbalanced and/or distorted when feeding unbalanced and/or nonlinear ac loads. The load-current feedforward control is often employed to eliminate the voltage distortion [18]. Nonetheless, extra current sensors are required to measure the load currents.

Combining the advantage of the 3D-SVM with the closed-loop control for the CM part in the load voltages and the advantage of the carrier-based modulation scheme with the low complexity for implementation, this letter proposes a closed-loop CM load-voltage control that incorporates a decoupled modulation scheme (CL-DMS) for the 3P4L4W 3L inverter. The proposed work aims at eliminating the CM part in the load voltages rather than the CM part in all phase-leg outputs (which equivalently mitigates the neutral-to-ground voltage). The attractive features of the proposed work include the following three aspects.

1) Reveals the physical concept of the control loops by using the derived CM and DM circuit models.
2) Retains the feature of the carrier-based modulation with the fourth phase leg modulated independently from the remaining three 3L phase legs.
3) Enables the carrier-based modulation with the closed-loop CM load-voltage control for improving the voltage quality in feeding unbalanced and/or nonlinear ac loads.

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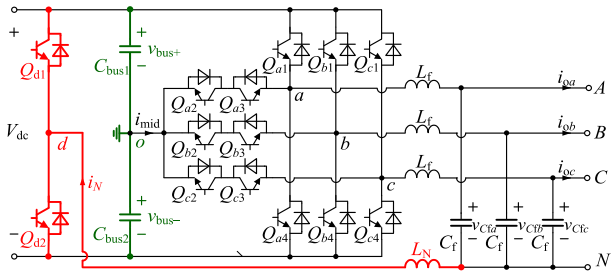

Fig. 1. Topology of the 3P4L4W 3L inverter.

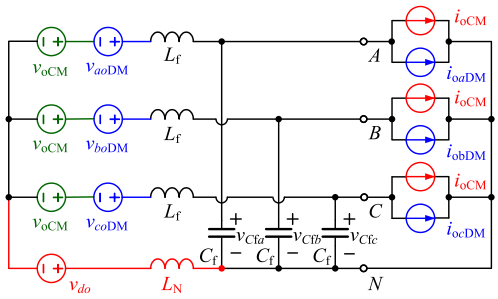

Fig. 2. Circuit model with v_{xo} and i_{ox} replaced by their CM and DM parts.

The rest of the letter is organized as follows. In Section II, CM and DM circuit models are derived for the 3P4L4W 3L inverter. On this basis, CL-DMS is proposed in Section III. The experimental results are presented in Section IV. Finally, Section V concludes this letter.

II. CM and DM Circuit Models

Fig. 1 shows the topology of the 3P4L4W 3L T-type inverter studied in this letter, where Q_{x1}–Q_{x4} ($x = a$, b, and c) form the three-phase 3L T-type phase legs, $C_{\rm bus1}$ and $C_{\rm bus2}$ are the split-capacitor legs, and $L_{\rm f}$ and $C_{\rm f}$ are the L–C filters. For reducing the power losses of the fourth phase leg and also being cost effective, an SiC 2L phase leg, formed by Q_{d1} and Q_{d2}, is used in this letter. Here, level-shifted sinusoidal pulsewidth modulation (LS-SPWM) [5] is employed to modulate Q_{x1}–Q_{x4}.

For the sake of simplicity, $v_{\rm oCM}$ and $v_{xo\rm DM}$ are defined as the CM and DM parts in v_{xo} ($x = a$, b, and c), respectively; $v_{C\rm fCM}$ and $v_{C\rm fDM}$ are the CM and DM parts in v_{Cfx}, respectively; $i_{\rm oCM}$ and $i_{ox\rm DM}$ are the CM and DM parts in $i_{\rm ox}$, respectively; and $i_{L\rm fCM}$ and $i_{L\rm fDM}$ are the CM and DM parts in i_{Lfx}, respectively. In the following analysis, the high switching frequency harmonics in the voltages and currents are neglected.

Replacing v_{xo} and $i_{\rm ox}$ with their CM and DM parts, the 3P4L4W 3L inverter can be represented by using the circuit model as given in Fig. 2. By applying Kirchhoff's voltage and current laws to each phase, one obtains

$$\begin{cases} v_{\rm oCM}+v_{ao\rm DM}=v_{Cfa}+v_{do}+L_{\rm f}\frac{di_{Lfa}}{dt}+L_{\rm N}\frac{di_{LN}}{dt} \\ v_{\rm oCM}+v_{bo\rm DM}=v_{Cfb}+v_{do}+L_{\rm f}\frac{di_{Lfb}}{dt}+L_{\rm N}\frac{di_{LN}}{dt} \\ v_{\rm oCM}+v_{co\rm DM}=v_{Cfc}+v_{do}+L_{\rm f}\frac{di_{Lfc}}{dt}+L_{\rm N}\frac{di_{LN}}{dt} \end{cases} \tag{1}$$

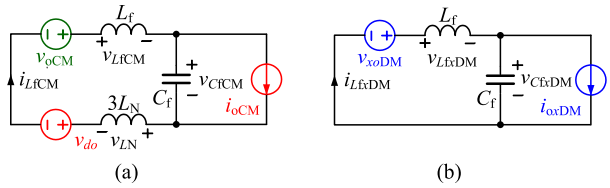

Fig. 3. Circuit model. (a) CM circuit model. (b) DM circuit model.

$$\begin{cases} C_{\rm f}\frac{dv_{Cfa}}{dt}=i_{Lfa}-(i_{\rm oCM}+i_{oa\rm DM}) \\ C_{\rm f}\frac{dv_{Cfb}}{dt}=i_{Lfb}-(i_{\rm oCM}+i_{ob\rm DM}) \\ C_{\rm f}\frac{dv_{Cfc}}{dt}=i_{Lfc}-(i_{\rm oCM}+i_{oc\rm DM}) \end{cases} \tag{2}$$

where $i_{LN}=i_{Lfa}+i_{Lfb}+i_{Lfc}=3i_{L\rm fCM}$ is the neutral inductor current.

From (1), summing up the left- and right-hand side terms of the three voltage equations leads to

$$v_{\rm oCM}=v_{C\rm fCM}+v_{do}+(L_{\rm f}+3L_{\rm N})\frac{di_{L\rm fCM}}{dt}. \tag{3}$$

Likewise, from (2), it can be derived

$$C_{\rm f}\frac{dv_{C\rm fCM}}{dt}=i_{L\rm fCM}-i_{\rm oCM}. \tag{4}$$

From (3) and (4), the CM circuit model for the 3P4L4W 3L inverter can be obtained, as shown in Fig. 3(a).

Subtracting (3) from each equation in (1) and (4) from each equation in (2) yields

$$\begin{cases} v_{oa\rm DM}=v_{Cfa\rm DM}+L_{\rm f}\frac{di_{Lfa\rm DM}}{dt} \\ v_{ob\rm DM}=v_{Cfb\rm DM}+L_{\rm f}\frac{di_{Lfb\rm DM}}{dt} \\ v_{oc\rm DM}=v_{Cfc\rm DM}+L_{\rm f}\frac{di_{Lfc\rm DM}}{dt} \end{cases} \tag{5}$$

$$\begin{cases} C_{\rm f}\frac{dv_{Cfa\rm DM}}{dt}=i_{Lfa\rm DM}-i_{oa\rm DM} \\ C_{\rm f}\frac{dv_{Cfb\rm DM}}{dt}=i_{Lfb\rm DM}-i_{ob\rm DM} \\ C_{\rm f}\frac{dv_{Cfc\rm DM}}{dt}=i_{Lfc\rm DM}-i_{oc\rm DM}. \end{cases} \tag{6}$$

From (5) and (6), the DM circuit model for the 3P4L4W 3L inverter can be obtained, as shown in Fig. 3(b).

Different from the average large-signal circuit model reported in [9], the derived CM and DM circuit models in this letter show how the CM and DM parts in the load voltages are formed, and these models aid in revealing the physical concept of different control loops as described in Section III.

III. CL-DMS With CM Load-Voltage Control for the 3P4L4W 3L Inverter

With the LS-SPWM for the 3L phase legs, v_{xo} in each switching cycle is obtained as follows [5]:

$$v_{xo}=\begin{cases} v_{\rm bus+}\cdot v_{\rm Mx}, & v_{\rm Mx}>0 \\ v_{\rm bus-}\cdot v_{\rm Mx}, & v_{\rm Mx}<0 \end{cases} \tag{7}$$

where v_{Mx} is the modulation voltage for each phase. Accordingly, $v_{\rm oCM}$ can be written as (8) at the bottom of this page, where $v_{\rm oCM}=(v_{Ma}+v_{Mb}+v_{Mc})V_{\rm dc}/6=0$, if $v_{\rm bus+}=v_{\rm bus-}=V_{\rm dc}/2$. This indicates that the CM part of the three 3L phase-leg outputs will be zero, if $v_{\rm bus+}$ is perfectly balanced with $v_{\rm bus-}$.

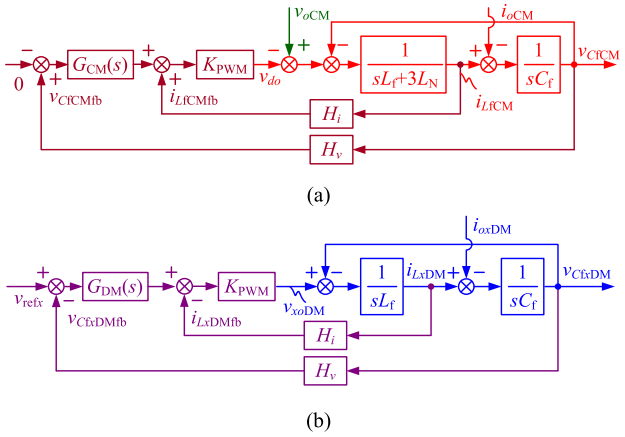

Fig. 4. Control block diagram of (a) CM load-voltage control and (b) DM load-voltage control.

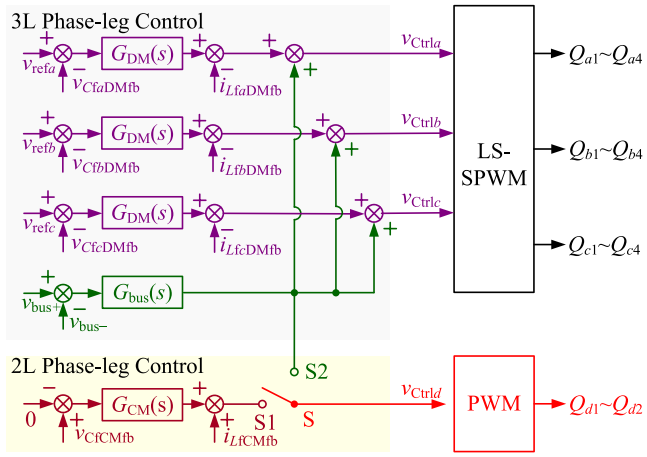

Fig. 5. Decoupled modulation for the 3P4L4W 3L inverter.

Applying Kirchhoff's voltage law to Fig. 3(a) yields

$$v_{CfCM} = v_{oCM} - (v_{LN} + v_{LfCM}) - v_{do} \tag{9}$$

where v_{LN} and v_{LfCM} are the voltage drop across L_N and L_f produced by i_{LfCM}, respectively. This indicates that the CM part in the load voltages, i.e., v_{CfCM}, is subject to the control for the fourth phase leg. In practice, v_{CfCM} is expected to be zero, for preventing the ac load voltages from unbalance and/or distortion under various load conditions. To attain this objective, v_{CfCM} is closed-loop controlled in this letter. In doing so, the average voltage of the fourth phase-leg output, i.e., v_{do}, could exactly counteract v_{oCM}, v_{LN}, and v_{LfCM} so that v_{CfCM} is regulated to be zero.

From the CM circuit model given in Fig. 3(a), the block diagram for the closed-loop CM load-voltage control can be derived, as shown in Fig. 4(a). Obviously, i_{oCM} and v_{oCM} are the perturbations that need to be rejected. For unbalanced linear loads, i_{oCM} only has a fundamental current. For balanced nonlinear loads, i_{oCM} is formed by odd triplen currents. For unbalanced nonlinear loads, i_{oCM} is composed of odd harmonic currents. On the other hand, a small amount of fundamental and third-order harmonics might be left in v_{oCM} because of the finite voltage balancing control loop gain. To reject all these disturbances, multiple proportional-resonant (PR) controllers can be used as the voltage regulator, i.e., $G_{CM}(s)$, for increasing the voltage loop gain at the concerned harmonic frequencies.

Applying Kirchhoff's voltage law to the circuit, as shown in Fig. 3(b), one obtains

$$v_{Cfx\mathrm{DM}} = v_{xo\mathrm{DM}} - v_{Lfx\mathrm{DM}} \tag{10}$$

where $v_{Lfx\mathrm{DM}}$ is the voltage drop across L_f produced by $i_{Lfx\mathrm{DM}}$. This indicates that the DM parts in the load voltages, i.e., $v_{Cfx\mathrm{DM}}$, are subject to the control for the 3L phase legs. Based on the DM circuit model given in Fig. 3(b), the block diagram for the closed-loop DM load-voltage control can be derived, as shown in Fig. 4(b). Obviously, i_{oxDM} is the perturbation that should be rejected. For linear ac loads, i_{oxDM} only has a fundamental current. Thus, the PR controller, with the resonant frequency at f_o, can be used as the voltage regulator, i.e., $G_{DM}(s)$, for each phase. For nonlinear loads, i_{oxDM} is mainly constituted by odd harmonic currents. To reduce any harmonic content, multiple PR controllers can also be adopted in order to increase the voltage loop gain at the concerned harmonic frequencies [19].

From the aforementioned theoretical discussions, one can draw the following conclusions.

1) The voltage balancing control for v_{bus+} and v_{bus-} determines the CM part of the three 3L phase-leg outputs.
2) The control of the fourth phase leg is equivalent to the control of the CM load voltage.
3) The control of the 3L phase legs is equivalent to the control of the three DM load voltages.

By integrating the split-capacitor voltage balancing control loop with the closed-loop DM load-voltage control to modulate the 3L phase legs and applying the closed-loop CM load-voltage control to modulate the fourth phase leg, the control block diagram for the proposed CL-DMS is obtained, as shown in Fig. 5 with S closed to S1. For comparison, the decoupled modulation with the fourth phase leg being modulated for balancing the split-capacitor voltages, namely, open-loop CM load-voltage control incorporated decoupled modulation scheme (OL-DMS) in this letter, is also illustrated in Fig. 5 with S closed to S2. Intuitively, v_{do} is open-loop set at v_{oCM}, incapable of counteracting v_{LN} and v_{LfCM} resulting from i_{LfCM}. This way, the CM part in the load voltages will be severely disturbed when the

$$v_{oCM} = (v_{ao} + v_{bo} + v_{co})/3 = \begin{cases} (v_{bus+} \cdot v_{Ma} + v_{bus-} \cdot v_{Mb} + v_{bus+} \cdot v_{Mc})/3 \ \omega t, \in (0, \pi/3) \\ (v_{bus+} \cdot v_{Ma} + v_{bus-} \cdot v_{Mb} + v_{bus-} \cdot v_{Mc})/3 \ \omega t, \in (\pi/3, 2/3) \\ (v_{bus+} \cdot v_{Ma} + v_{bus+} \cdot v_{Mb} + v_{bus-} \cdot v_{Mc})/3 \ \omega t, \in (2\pi/3, \pi) \\ (v_{bus-} \cdot v_{Ma} + v_{bus+} \cdot v_{Mb} + v_{bus-} \cdot v_{Mc})/3 \ \omega t, \in (\pi, 4\pi/3) \\ (v_{bus-} \cdot v_{Ma} + v_{bus+} \cdot v_{Mb} + v_{bus+} \cdot v_{Mc})/3 \ \omega t, \in (4\pi/3, 5\pi/3) \\ (v_{bus-} \cdot v_{Ma} + v_{bus-} \cdot v_{Mb} + v_{bus+} \cdot v_{Mc})/3 \ \omega t, \in (5\pi/3, 2\pi) \end{cases} \tag{8}$$

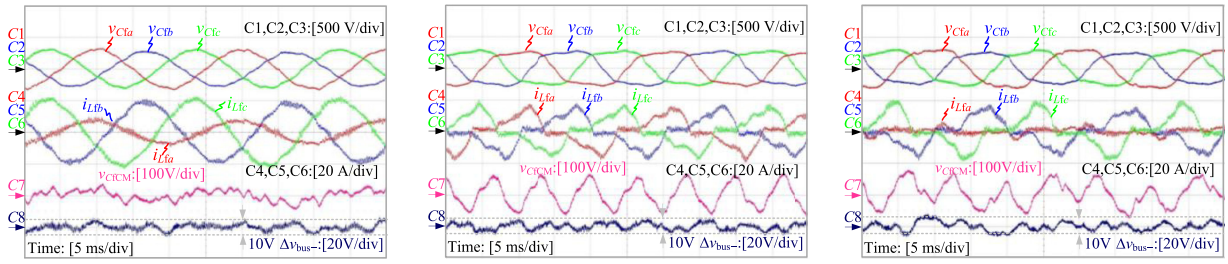

Fig. 6. Steady-state waveforms for the inverter with OL-DMS. (a) Unbalanced linear load. (b) Balanced rectifier load. (c) Unbalanced rectifier load.

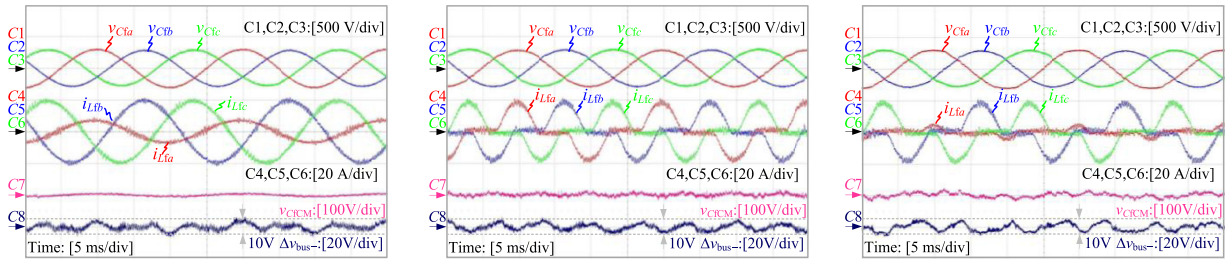

Fig. 7. Steady-state waveforms for the inverter with CL-DMS. (a) Unbalanced linear load. (b) Balanced rectifier load. (c) Unbalanced rectifier load.

TABLE I
PROTOTYPE PARAMETERS

Parameter	Symbol	Value
DC Input Voltage	V_{dc}	800 V
AC Phase Voltage	V_{Cfx}	220 V (RMS)
Output Frequency	f_o	50 Hz
Switching Frequency	f_s	10 kHz
Apparent Power	S	10 kVA
DC-Bus Capacitor	C_{bus1}/C_{bus2}	250 μF
AC Filter Inductor	L_f	2.4 mH
Neutral Inductor	L_N	2.4 mH
AC Filter Capacitor	C_f	10 μF

TABLE II
MEASURED THD AND VUF FOR AC LOAD VOLTAGES

Load Type	Modulation	THD (%) Ph A	THD (%) Ph B	THD (%) Ph C	VUF (%)
Unbalanced Res. Loads	OL-DMS	1.43	1.45	1.44	5.98
	CL-DMS	0.54	0.58	0.62	1.57
Balanced Rect. Loads	OL-DMS	17.65	17.62	17.63	0.05
	CL-DMS	1.50	1.52	1.50	0.01
Unbalanced Rect. Loads	OL-DMS	11.24	14.31	13.81	9.27
	CL-DMS	1.79	1.98	1.82	1.60

ac loads are highly unbalanced and/or nonlinear [20]. Hence, the proposed CL-DMS will benefit the 3P4LW 3L inverter with better voltage quality over the OL-DMS for feeding unbalanced and/or nonlinear ac loads.

IV. EXPERIMENTAL RESULTS

In this section, a 10-kVA 3P4L4W 3L T-type inverter is built and tested to demonstrate the feasibility and the advantages of the proposed work. Table I lists the main prototype parameters.

Fig. 6 shows steady-state waveforms for the 3P4L4W 3L T-type inverter with OL-DMS feeding unbalanced linear load, balanced rectifier load, and unbalanced rectifier load, respectively. As shown, the upper/lower dc bus capacitor voltage ripple has been effectively limited within 10 V by the tight regulation of the voltage balancing loop. Suffering from the loss of the closed-loop CM load-voltage control, the three-phase ac load voltages has a high CM part, leading to voltage unbalance and/or distortion when feeding unbalanced and/or nonlinear ac loads.

Fig. 7 shows steady-state waveforms for the 3P4L4W 3L T-type inverter with CL-DMS feeding the same ac loads as the ones that are tested in Fig. 6. With the closed-loop control of the CM load voltage, the CM part in the ac load voltages is significantly reduced with respect to the one with OL-DMS. Therefore, the three-phase ac load voltages become balanced and sinusoidal even when feeding unbalanced and/or nonlinear ac loads.

According to the test waveforms given in Figs. 6 and 7, Table II lists the measured total harmonic distortion (THD) and the voltage unbalanced factor (VUF) for the ac load voltages when feeding different types of loads. As seen, the proposed CL-DMS provides the 3P4LW 3L inverter with high-quality ac load voltages, with both THD and VUF less than 2% when feeding unbalanced and/or nonlinear ac loads in this study, satisfying the voltage quality requirement in the Standard EN 50160.

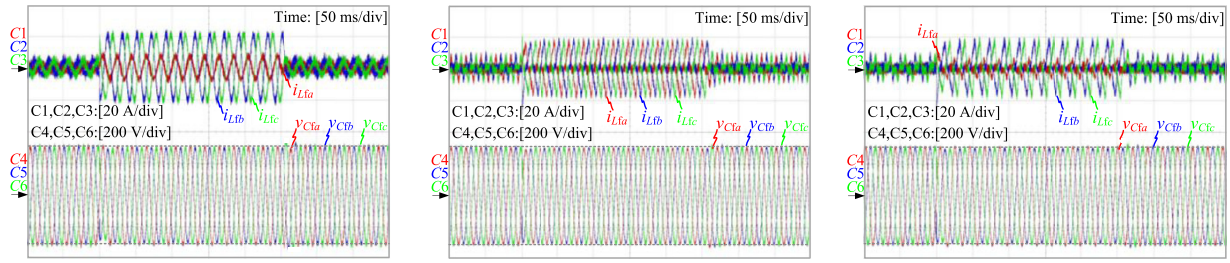

Fig. 8. Load transient waveforms for the inverter with CL-DMS. (a) Unbalanced linear load. (b) Balanced rectifier load. (c) Unbalanced rectifier load.

Fig. 8 shows load transient waveforms for the 3P4L4W 3L T-type inverter with CL-DMS under unbalanced linear load, balanced rectifier load, and unbalanced rectifier load. As shown, the ac output voltages in each test scenario are able to recover to the steady state within half a line cycle with the voltage overshoot/undershoot less than 20 V in response to the step-up or step-down load, complying with the expected dynamic performance as stipulated in Standard EN 50160. This demonstrates that the inverter with CL-DMS has a satisfactory dynamic performance under the tested ac loads.

V. Conclusion

In this letter, the CM and DM circuit models were built for the 3P4L4W 3L inverter, showing that the split-capacitor voltage balancing control determined the CM voltage of three outputs by 3L phase legs, the DM voltage control for the 3L phase legs was equivalent to the control of the three DM load voltages, and the control for the fourth phase leg was equivalent to the control of the CM load voltage. On these bases, the CL-DMS was proposed for the 3P4L4W 3L inverter, with which the 3L phase legs were modulated to attain both the split-capacitor voltage balancing control and the closed-loop DM load-voltage control, whereas the fourth phase leg was independently modulated to attain the closed-loop CM load-voltage control. The proposed work had been validated on a 10-kVA 3P4L4W 3L T-type inverter. The test results demonstrated that the proposed CL-DMS benefitted the 3P4LW 3L inverter with high-quality ac load voltages, with both THD and VUF less than 2%, for feeding unbalanced and/or nonlinear ac loads.

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