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BACKGROUND AND OBJECTIVES

- MV SiC MOSFETs enable on reducing stages & volume of MV DC/DC converters and bring more challenge on the insulation design & parasitics control.
- Leakage integration in MV transformer eliminates the bulky insulated series inductor but may introduce high loss due to leakage flux.
- Parasitic capacitances interact w/ front-end converter, grounding loop, generating EMI.

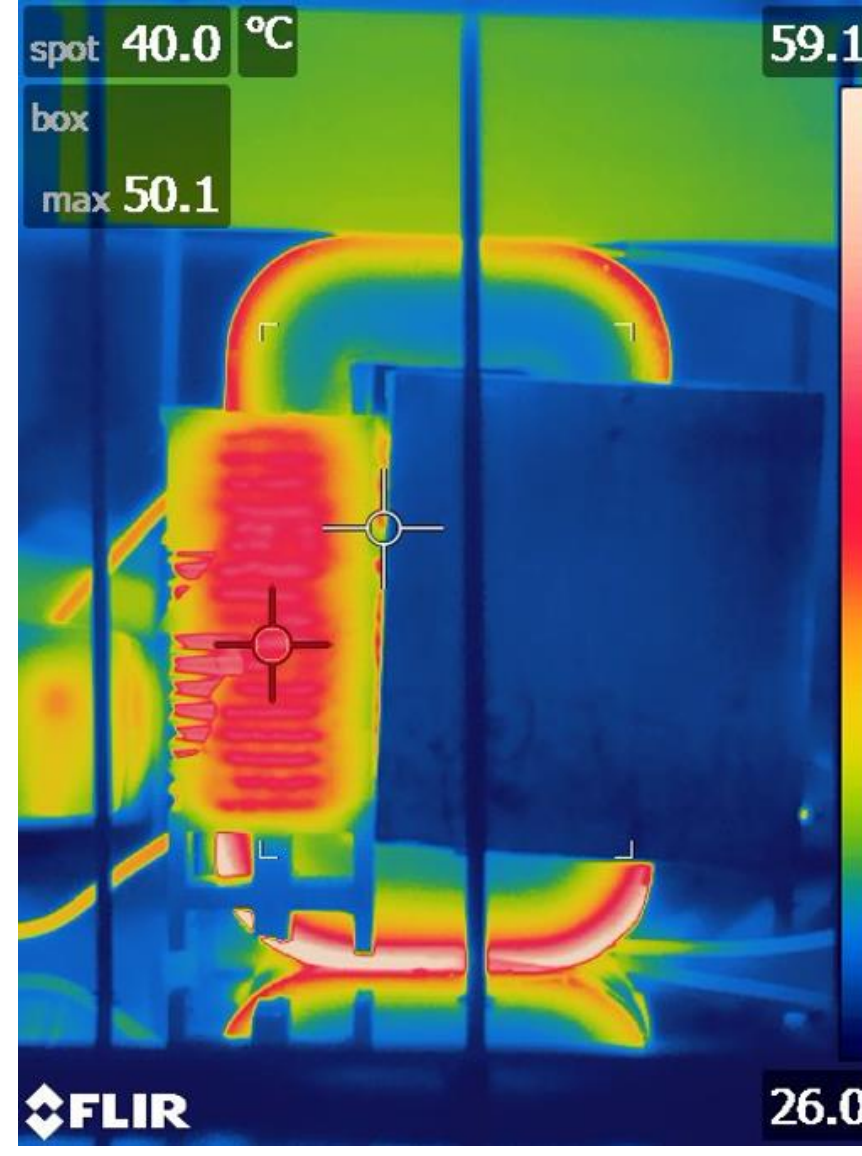


Fig. 1: Thermal image w/ leakage induced eddy current

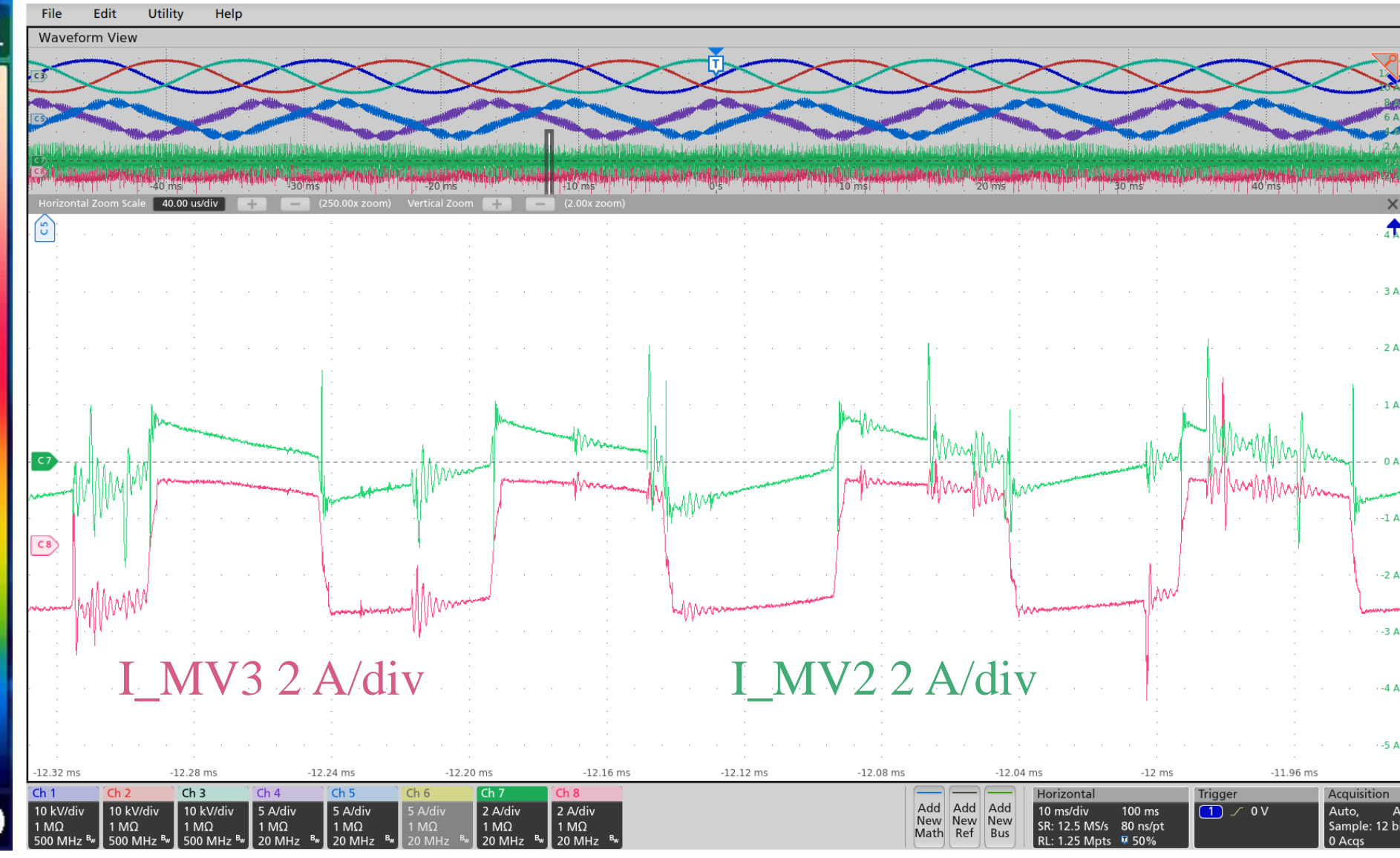


Fig. 2: Waveform of MV transformer current w/ impact of parasitic capacitances

LEAGUE INTEGRATION WITH REDUCED EDDY CURRENT LOSS

- Shell-type transformer, interleaved winding for LV winding to reduce leakage inductance.
- Ferrite bridges added to generate extra leakage flux. The leakage inductance can be tuned by the air gap in ferrite bridges.
- Cores can be further sliced to reduce eddy current.

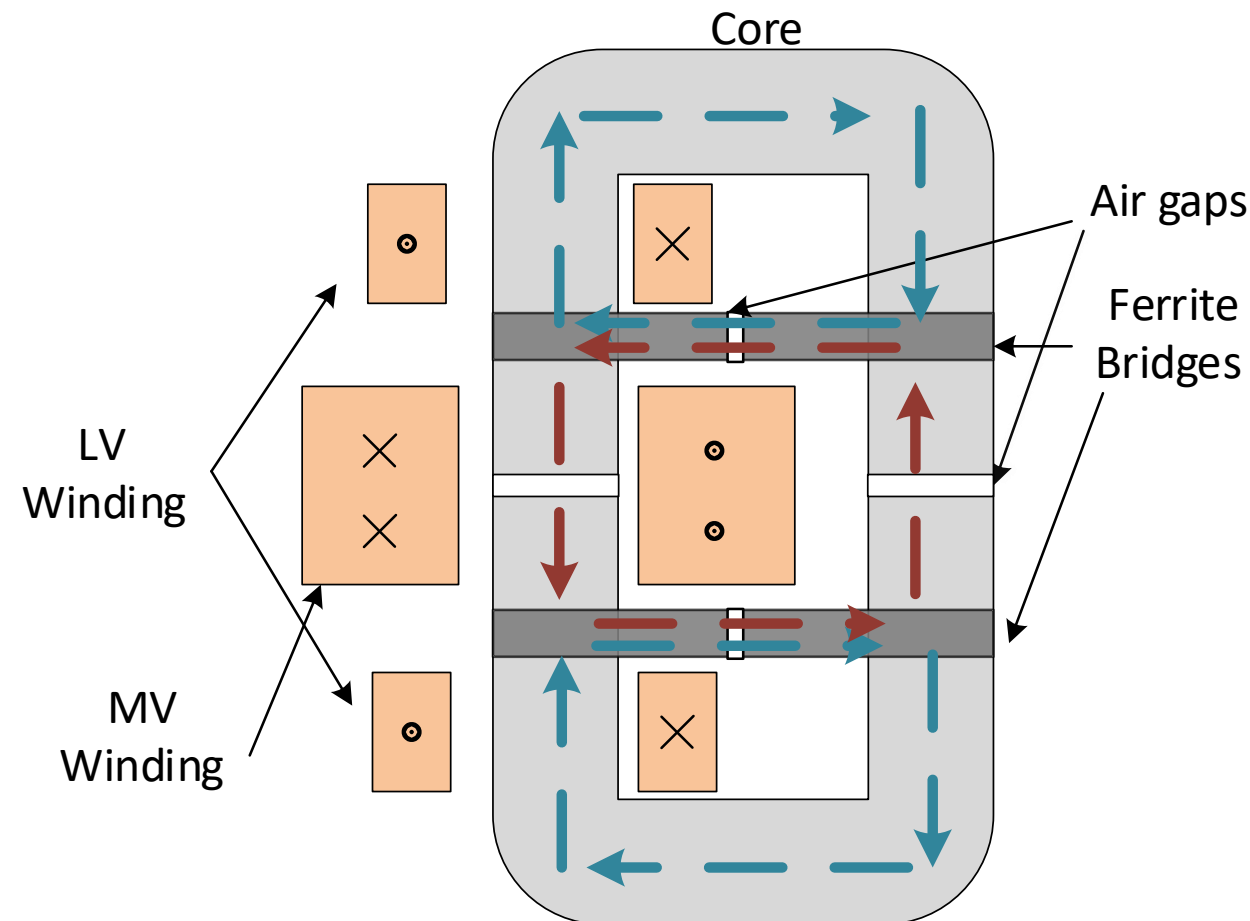


Fig. 3: Structure of proposed transformer

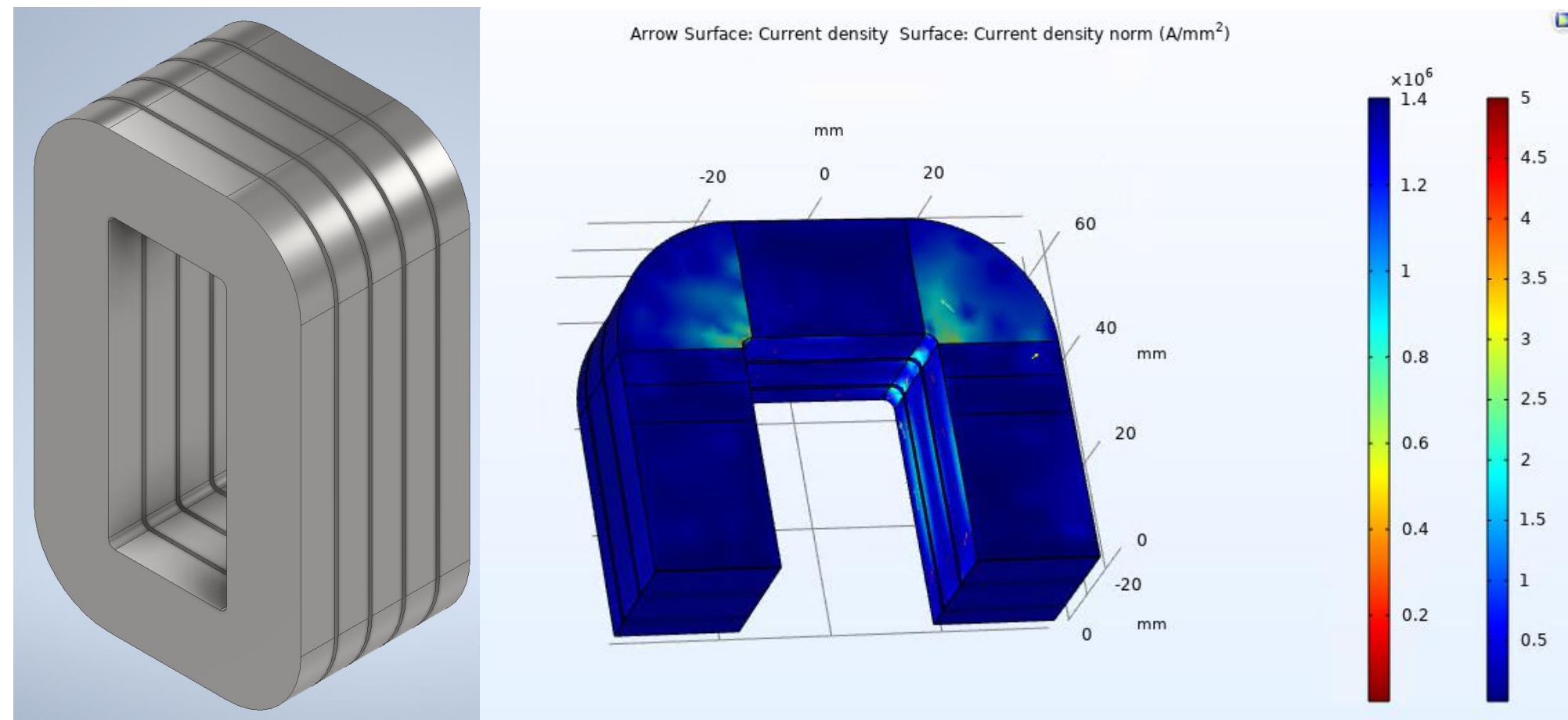


Fig. 4: Sliced cores and eddy current simulation result

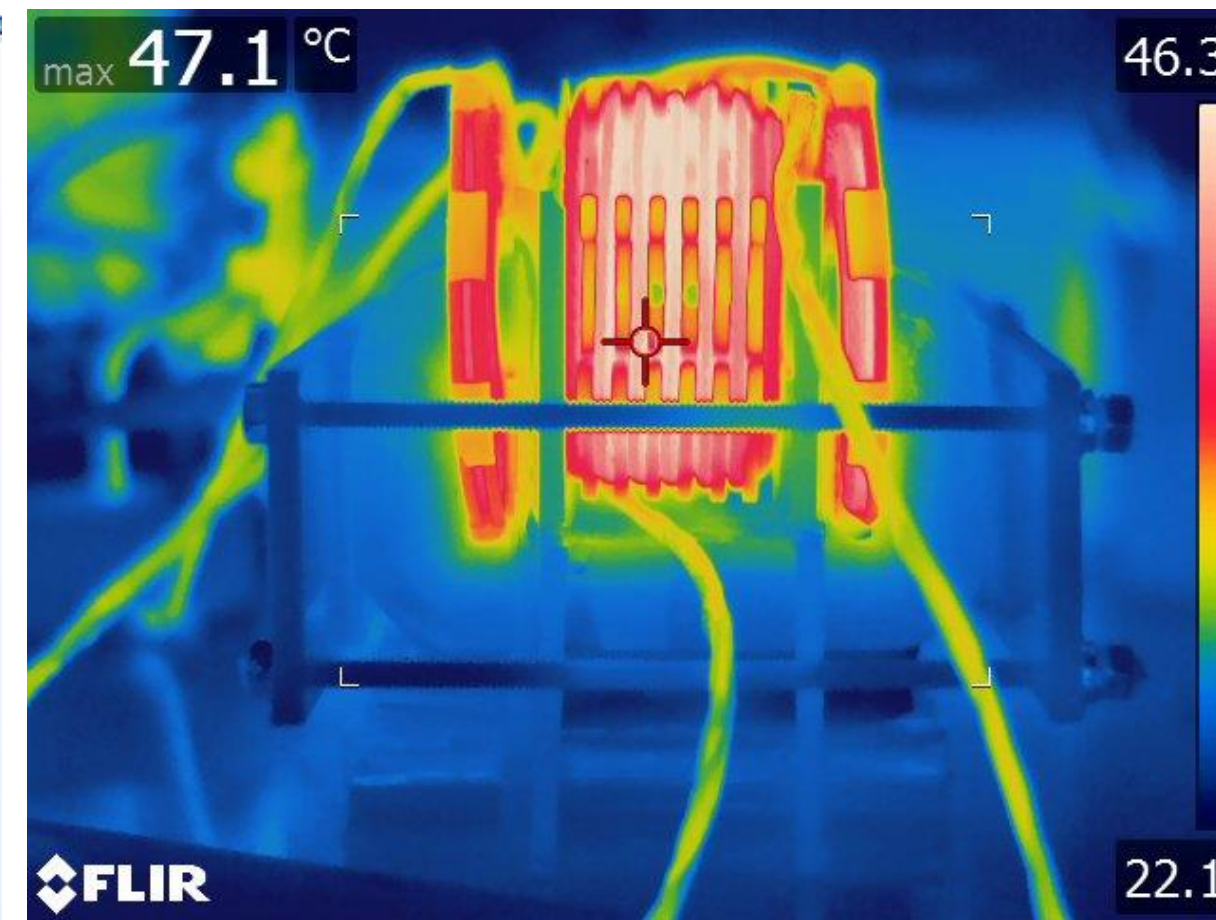


Fig. 5: Thermal image of reduced eddy current loss

INSULATION WITH REDUCED PARASITIC CAPACITANCE

- Partially shielding used to confine only part of electric field.
- “Edge termination” needed for shielding boundary.

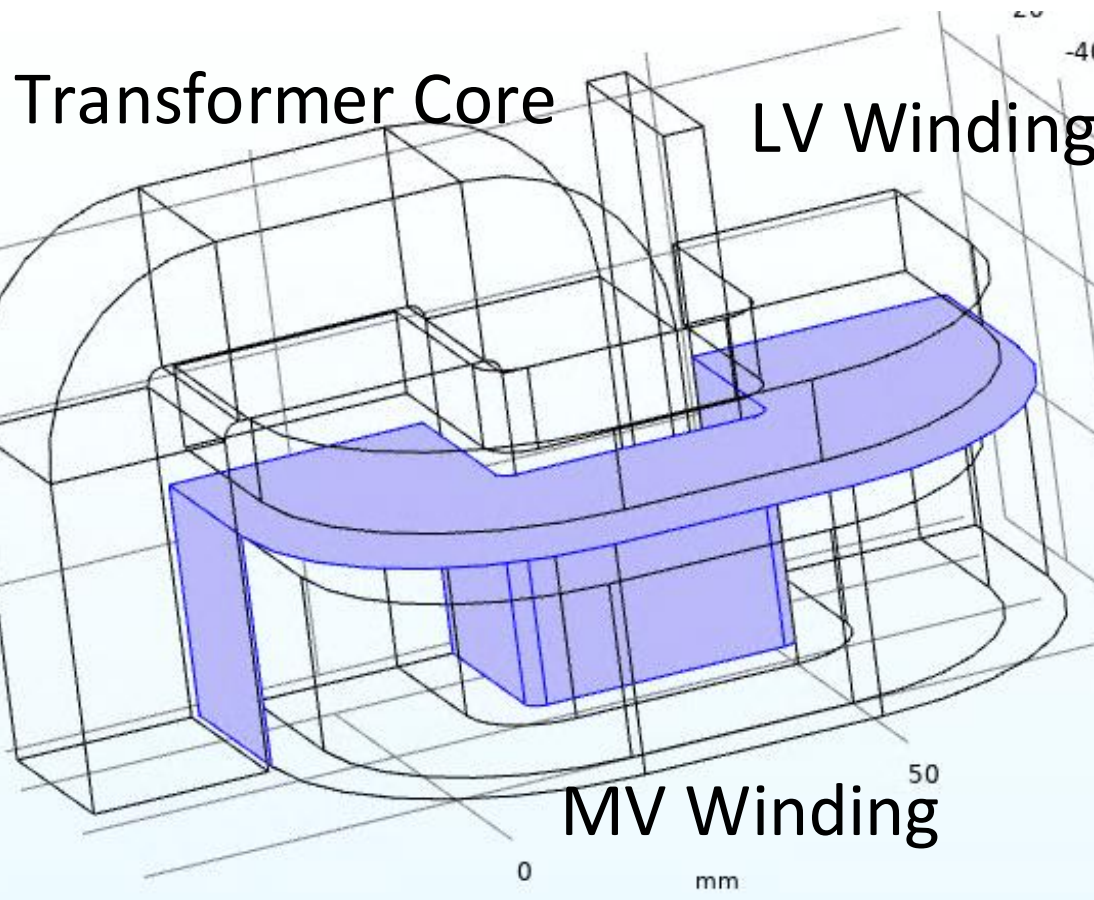


Fig. 6: Partial shielding for MV winding

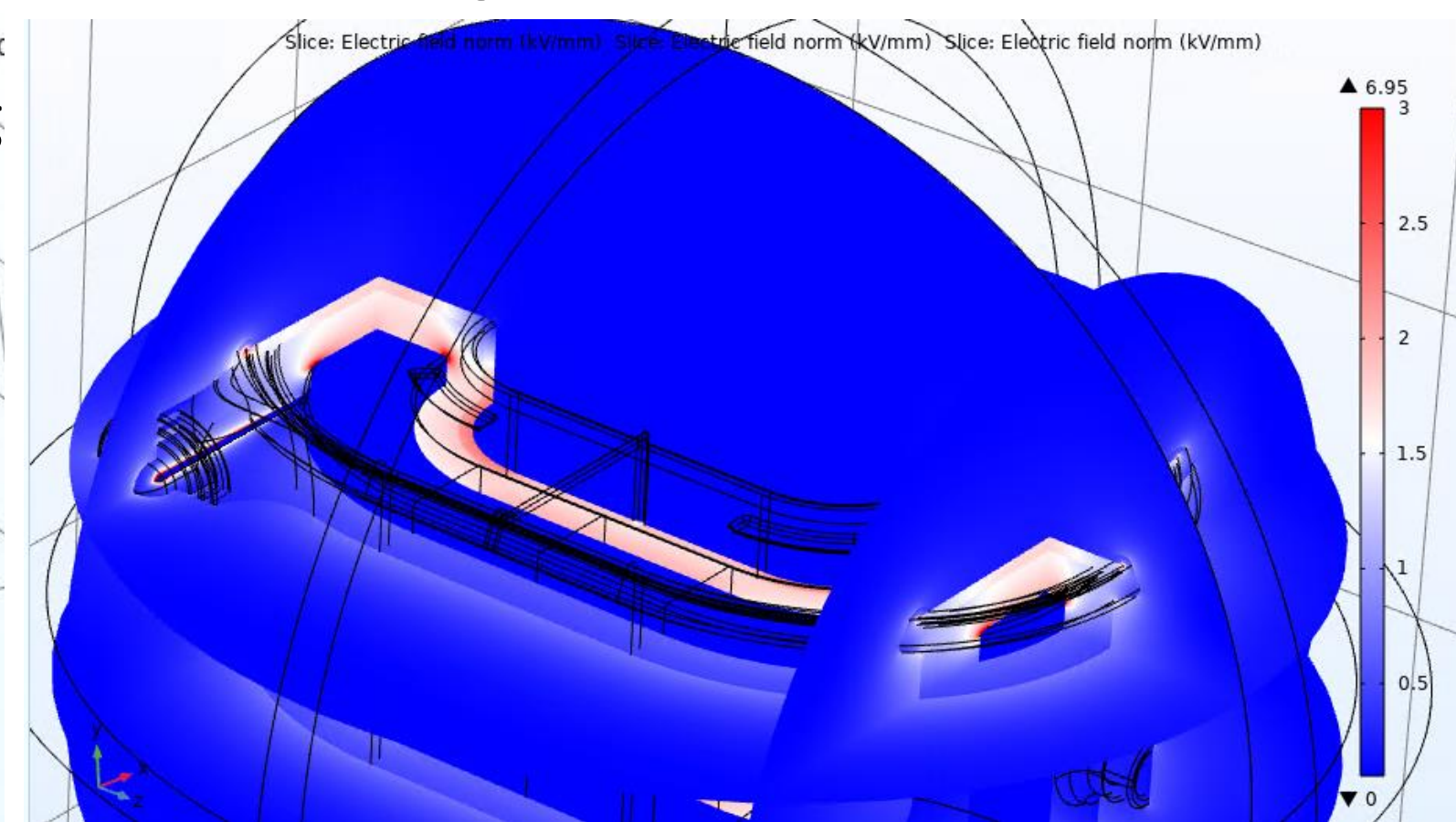


Fig. 7: Electric field simulation result

EXPERIMENTAL TEST

- Prototype built for 850/6700-V 16.7-kW DAB converters using 10-kV SiC devices.

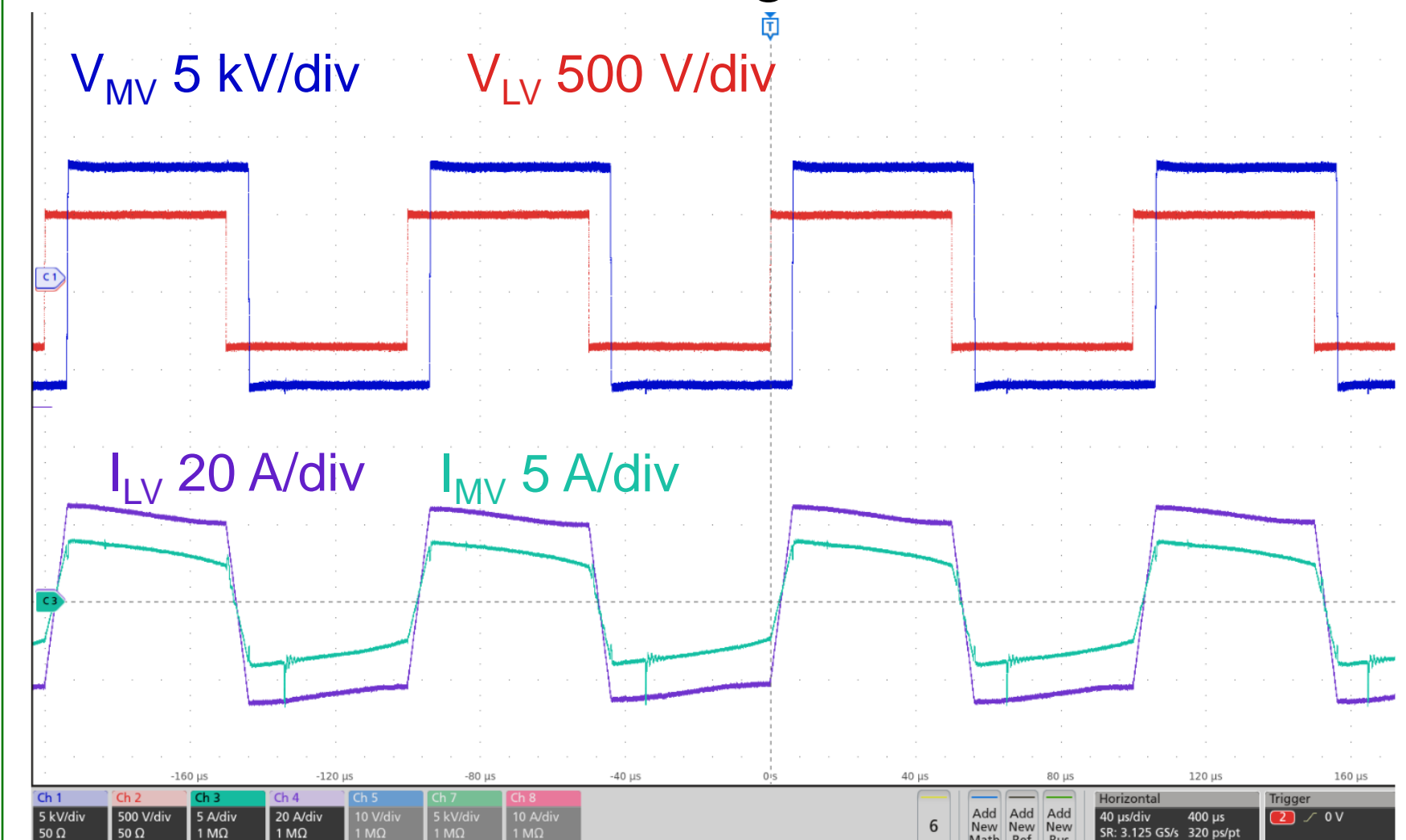


Fig. 8: Test waveform at full-load

CONCLUSION

- Ferrite bridges can efficiently integrate the leakage inductance. The leakage eddy current loss can be further reduced by slicing cores.
- Partial shielding reduces capacitance for shielded winding, while edge termination is needed for field shaping.