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Design and Optimization of a High Gravimetric Power Density Receiver for Wireless Charging of Drones

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***Abstract*—This article presents the weight optimization of a receiver for wireless drone charging applications. There is need for comprehensive modeling to minimize the onboard weight on the flying drone platform. A systematic approach that codesigns all stages of the wireless charger, based on comprehensive loss, weight, and thermal modeling, is put forward to minimize the on-board weight for drone wireless charging applications. A 200 W, GaN-based prototype is implemented to validate the modeling. The prototype has been tested up to 204 W without any active cooling. The receiver achieves a gravimetric power density of 8.3 W/g excluding the weight of connectors, sensing, and control.**

***Index Terms*—Wireless power transfer (WPT), power density, synchronous rectifier.**

I. Introduction

Unmanned aerial vehicles (UAVs) have become prevalent in recent years. This makes it possible to improve commercial services such as package delivery, inspection, search and rescue, etc., [1]–[4]. Wireless charging of small UAVs, or drones, has received considerable interest as a technology to allow fully autonomous operation of UAV fleets [1]. The goal of the wireless power transfer (WPT) system-level design is to reduce the weight of on-board components, such as the Rx coil, rectifier, and any receiver-side dc-dc converters, to maximize drone flight time. Simultaneously, high output power is desirable to decrease charging time and allow for maximum uptime. Combining these two, high gravimetric power density of receiver side components is the primary design goal; high efficiency of the receiver is desirable only insofar as it allows reduced weight of thermal management. The transmitter-side (Tx) components are not required to be lightweight, but instead can be designed to assist in minimizing onboard receiver weight. Many studies have provided detailed optimization of power stage volumetric power density [5] or area, volume, and weight-related power density of magnetic [2]–[4] or capacitive couplers [6] in WPT applications.

Reviewing the literature, a systematic approach that codesigns all stages of the wireless charger, based on comprehensive loss, weight, and thermal modeling, is required to minimize the on-board weight for drone wireless charging applications. Therefore, this article focuses on a systematic design and optimization method to maximize gravimetric power density of the wireless receiver as shown in Fig. 1.

The power losses of the various stages of the on-board receiver are modeled in Section II. Also, this section presents the thermal modeling of the receiver power stage without any external cooling, and the Rx coil thermal model. Section II concludes with the weight models of the receiver stages. In Section III, all the stages of the receiver, modelled in Section II are designed and co-optimized to achieve high gravimetric power density of the overall receiver. Section IV presents the experimental results. Finally, Section V concludes this article.

II. System Structure and Modeling

The equivalent circuit of the entire WPT system, operating from a dc supply, is shown in Fig. 1. The receiver side consists of the Rx coil, series matching capacitors, a full-bridge (FB)

TABLE I
System Specifications

Parameter	Specification
$f_{s,wpt}$	160 kHz
V_{out}	22.2 V
P_{out}	200 W
Tx coil	15 turns of 260/38 AWG Litz

TABLE II
Parameters used in Ellison's Model

Plate orientation	$L_{ch}(m)$	f	n
A horizontal plate facing upward	$WL/2(W+L)$	1.0	0.33
A horizontal plate facing downward	$WL/2(W+L)$	0.5	0.33
A vertical plate	Th	1.22	0.35

W, L and Th are width, length and thickness of the plate, respectively.

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synchronous rectifier, and a synchronous buck converter. Only this topology is studied in this work, though other designs are being considered in future work. The transmitter side is composed of a FB inverter and a Tx coil with series compensation. The specifications of an example wireless charging system, which will be used for the analysis and design in this article are given in Table I. For the rectifier and buck converter, eGaN FETs from EPC and GaN Systems are considered. Among these candidates, due to their chip-scale packaging, the transistor selection has minimal impact on PCB area or weight except as dictated by thermal modeling. Though package size varies significantly among these components, their weight is minimal compared to the PCB and passive components, and the PCB area is dominated by power stage and gate drive routing, auxiliary components, and thermal design.

The buck inductor is implemented from a database of prefabricated SMD inductors ranging from 50 nH to 10 μH. Suitable candidates are selected based on adequate saturation current, then optimized for system weight in the final design.

A. Receiver Electrical Modeling

1) Synchronous Rectifier Loss Model: The rectifier is modeled for operation at near-resistive load operation, with minimal phase-shift as necessary for ZVS. Neglecting the impact of dead time on the overall waveform, and applying a fundamental harmonic approximation, the rectifier input current i_{rec} is

$$i_{rec} = \frac{\pi P_{out}}{2V_{mid}} \sin(\omega_{s,wpt} t) \tag{1}$$

where $\omega_{s,wpt}$ is switching frequency of the rectifier.

To achieve zero voltage turn on of all the FETs the required minimum dead time is [7]

$$dt_{rec} = \frac{1}{\omega_{s,wpt}} \cos^{-1}\left(1 - \frac{C_{eq,Q,rec} V_{mid} \omega_{s,wpt}}{I_{rec}}\right) \tag{2}$$

where the nonlinear C_{oss} capacitance is approximate by the charge equivalent linear capacitance, $C_{eq,Q,rec}$ [8], and $I_{rec} = \pi P_{out}(2V_{mid})^{-1}$ is the amplitude of i_{rec}. Operating with minimal deadtime to achieve soft switching at near-resistive rectifier phase minimizes rectifier thermal management requirements. Due to ZVS operation of rectifier FETs, the only source of switching loss considered is the gate charge loss,

$$P_{g,rec} = 4 Q_{g,rec} V_{dr} f_{s,wpt} \tag{3}$$

where $Q_{g,rec}$ is the gate charge of one rectifier FET and V_{dr} is the gate drive voltage.

The total conduction loss for the rectifier switches is

$$P_{cond,rec} = R_{ds,rec} I_{rec}^2 \tag{4}$$

where $R_{ds,rec}$ is the ON-resistance of one transistor.

2) Synchronous Buck Loss Model: The output current ripple of the synchronous buck converter is

$$\Delta i_{out} = \frac{I_{out}(1-D)}{8 C_{out} L f_{s,buck}^2} \tag{5}$$

where $I_{out} = P_{out}/V_{out}$ is the average value of i_{out} and D is the duty ratio of the buck. i_{out} is restricted to 10 % of the maximum charging current with any value of buck inductance (L) by setting the corresponding minimum value of C_{out}. The buck switching frequency ($f_{s,buck}$) is varied from 100 kHz to 1 MHz.

The buck inductor current ripple is

$$\Delta i_L = \frac{V_{out}(1-D)}{L f_{s,buck}} \tag{6}$$

The root mean square (RMS) value of i_L is

$$I_{L,rms} = I_{out} \sqrt{1 + \frac{1}{3}\left(\frac{\Delta i_L}{2 I_{out}^2}\right)} \tag{7}$$

The total conduction loss of the buck half-bridge (HB) is then

$$P_{cond,buck} = R_{ds,buck} I_{L,rms}^2 \tag{8}$$

where $R_{ds,buck}$ is the ON-resistance of one buck FET. The buck switching loss model includes gate charge loss, switch output capacitance loss and turn-on overlap loss. The gate charge loss for the buck HB is

$$P_{g,buck} = 2 Q_{g,buck} V_{dr} f_{s,buck} \tag{9}$$

where $Q_{g,buck}$ is the gate charge of one buck FET and V_{dr} is the gate drive voltage. The switch output capacitance loss is

$$P_{coss,buck} = f_{s,buck} C_{eq,Q,buck} V_{mid}^2 \tag{10}$$

where $C_{eq,Q,buck}$ is the charge equivalent linear capacitance of the buck FET. The turn-on overlap loss is approximately

$$\begin{aligned} P_{ov,buck} &= 0.5 V_{mid} I_{L,min} t_{ov} f_{s,buck} \\ &= 0.5 V_{mid} \frac{(I_{out} - \frac{1}{2}\Delta i_L) Q_{ov}}{(V_{dr} - V_{gs(th)})/R_G} f_{s,buck} \end{aligned} \tag{11}$$

where $I_{L,min}$ is the minimum inductor current, which is the high side switch current at the turn-on instant. t_{ov} is the duration for which the voltage and current overlap when the switch turns on, Q_{ov} is the charge supplied to the deivce gate during the overlap period, $V_{gs(th)}$ is the gate threshold voltage of the FET, and R_G is the total gate resistance in the turn-on path.

3) Rx coil Loss Model: The receiver coil is modeled considering Litz wire of varying AWG and number of turns. With minimum pitch between windings, the length of the winding is

$$l_{rx} = \pi N_{rx}(d_{out,rx} + d_{in,rx})/2 \tag{12}$$

where $d_{in,rx}$ and $d_{out,rx}$ are the inner and outer diameters of the coil, respectively. The dc resistance of a Litz wire coil is then

$$R_{dc} = \rho_{cu} \frac{l_{rx}}{a_{w,rx}} \tag{13}$$

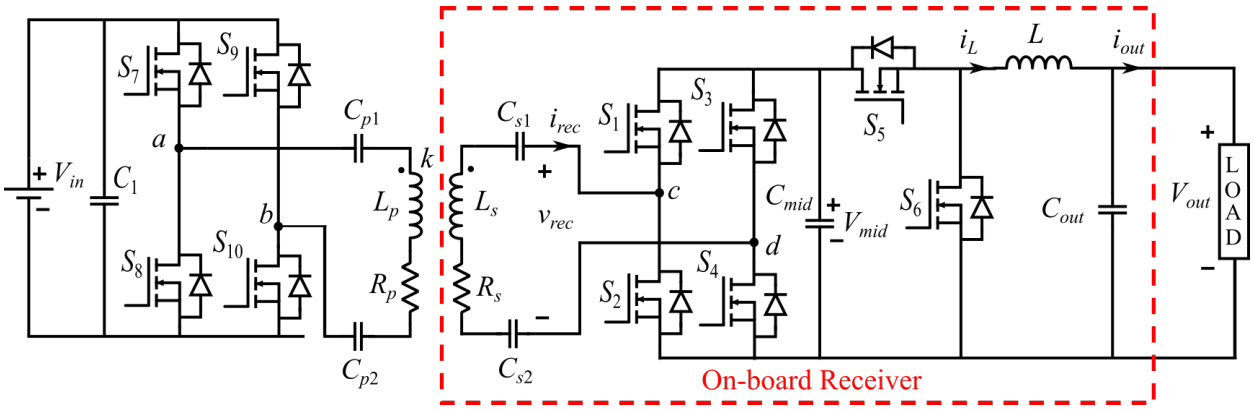


Fig. 1. Circuit schematic of the WPT system, including inverter, Tx and Rx coils, rectifier, and buck.

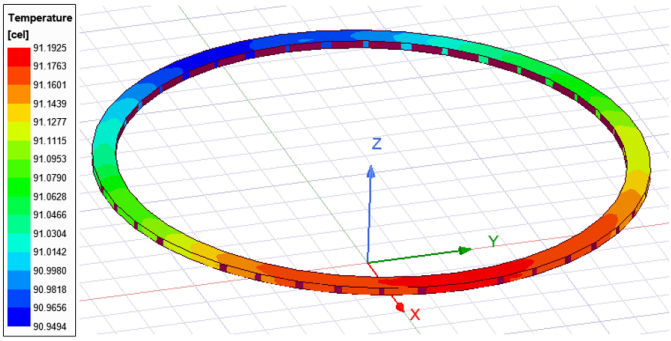


Fig. 2. Thermal simulation of Rx coil in Ansys Icepak.

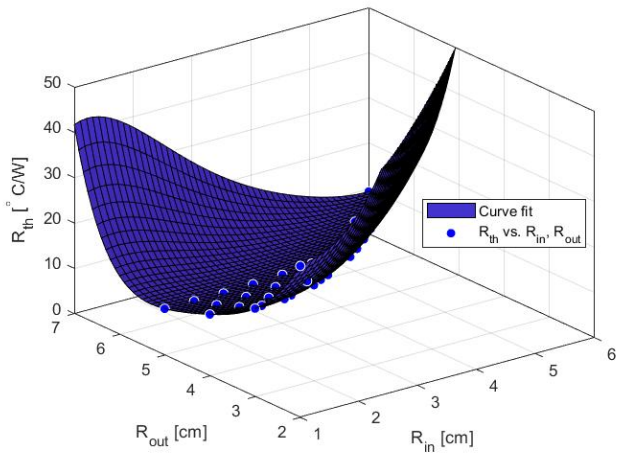


Fig. 3. Curve fitting of coil thermal Resistance for varying coil inner and outer radii, based on Ansys Icepak simulation results.

where $a_{w,rx}$ is the bare copper cross-sectional area of the wire and ρ_{cu} is the resistivity of copper.

To model the impact of skin and eddy currents, the AC resistance factor [9] of the coil is

$$F_R = \frac{R_{ac}}{R_{dc}} = 1 + \frac{(\pi n_{rx} N_{rx})^2 d_s^6}{192 \delta_{rx}^4 b_{rx}^2}. \tag{14}$$

where n_{rx} and N_{rx} are the number of strands and number of turns, d_s is the strand diameter, δ_{rx} and b_{rx} are the skin depth and winding breadth of the coil. The Rx coil losses are then

$$P_{rx} = \frac{1}{2} {I_{rec}}^2 R_{dc} F_R \tag{15}$$

B. Receiver Thermal Modeling

Based on existing prototypes for comparable applications and power levels [1]–[4], gravimetric power densities approaching 10 W/g are considered an optimistic design goal for this design. With only 20 g available for the receiver-side components at an output power of 200 W, most traditional active-cooling solutions are infeasible within this weight limit. Lightweight heatsinks suitable for natural convection exist but may not have sufficiently low thermal resistance at the low weights required in this application. Instead, this work foregoes the use of any additional thermal components, and instead designs the system loss and geometry such that thermal limits are not exceeded in the targeted lightweight design.

1) PCB Thermal Model: Ellison [10] presents a model for convective heat transfer coefficients in a natural convection condition for small devices as

$$h_c = 0.83 f (\Delta T / L_{ch})^n \tag{16}$$

where ΔT is the temperature difference between the component case and the ambient, L_{ch} is the characteristic length, and f and n are the constants, defined in Table II.

Ellison's model is used in this work to approximate the thermal resistance at natural convection of the entire receiver PCB, assuming that the PCB is placed flat, has relatively small component surface area relative to the PCB surface area, and has large copper pours on the top side that result in significantly lower thermal resistance across the face of the PCB than between the PCB and ambient. Under these assumptions, only the dimensions of the PCB are needed to calculate the approximate thermal resistance to ambient.

2) Rx Coil Thermal Model: The temperature rises of the different coil geometries are

$$\Delta T_{rx} = \frac{{I_{rec}}^2 F_R R_{dc,amb} R_{th}}{2 - \alpha_{cu} {I_{rec}}^2 F_R R_{dc,amb} R_{th}} \tag{17}$$

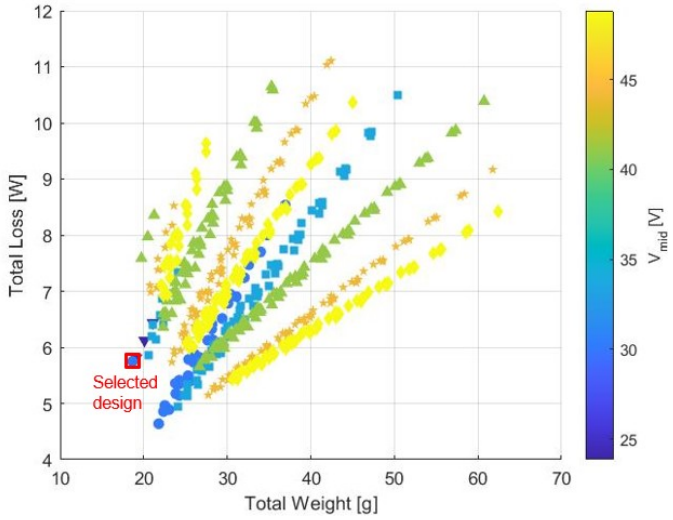


Fig. 4. Design space for system-level optimization of receiver.

where $R_{dc,amb}$ is the dc resistance of the coil at ambient temperature, R_{th} is the thermal resistance of the coil, and α_{cu} is the temperature coefficient of resistance for copper [11].

R_{th} values for the various coil geometries are obtained through curve-fitting FEA simulation data from Ansys Icepak thermal simulations. In this work, R_{th} values are only obtained for equivalent wire diameter of AWG 22. Each coil is approximated as a rectangular cross-section toroid, an example of which is shown in Fig. 2. The inner and outer radii of the toroid are swept over a range of values and resimulated to generate data that sufficiently spans the design range. The curve fit model equation is

$$R_{th} = \sum_{m=0}^{5} \sum_{n=0}^{5} P_{mn} R_{in}^{m} R_{out}^{n} \tag{18}$$

where P_{mn} are the fitted coefficients, and R_{in} and R_{out} are the inner and outer radii of the Rx coil, respectively. The curve fit is shown in Fig. 3.

C. Weight Models

The PCB weight is modeled considering 31 mils overall thickness, FR4 dielectric, and 4 layers of 1 oz copper with fill factors of 70% for two layers and 20% for the other two layers. The buck inductor weights are taken from their respective datasheets.

The model for Rx coil weight is

$$m_{rx} = \sigma_{cu} a_{w,rx} l_{rx} + \sigma_{ins} l_{rx} \tag{19}$$

where σ_{cu} is the density of copper and σ_{ins} is the linear density of the insulating material.

III. System-level Design and Optimization

The goal of the WPT system-level design is to optimize all stages of the receiver, modeled in Section II, simultaneously, to achieve high gravimetric power density of the overall receiver.

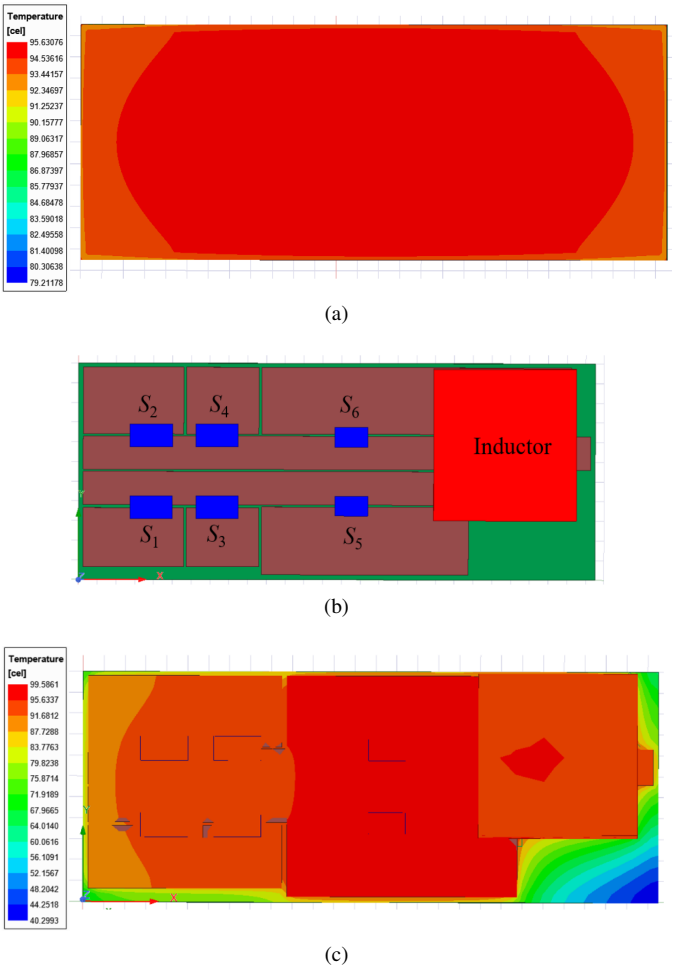


Fig. 5. Ansys Icepak thermal simulation result for power stage models at varying fidelity. (a) Total power stage loss applied to a 70 × 29 mm copper plane on the top layer of a PCB, (b) Layout diagram of PCB design for prototype, and (c) Icepak thermal simulation of detailed PCB layout.

To design the Rx coil, the number of turns is iterated from 1 to 15, and $d_{in,rx}$ is varied from 3 cm to 10 cm. Litz wire of 38 AWG individual strands and equivalent diameters ranging from AWG 26 to AWG 14 are considered (based on availability of parts) to reduce AC losses. The objective is not to design the lightest Rx coil in isolation, but to to design a Rx coil, having a maximum temperature rise of 80°C, that will result in the lightest on-board receiver.

For the PCB, Ellison's correlation model (16) is applied to calculate the copper pour area on the PCB required to dissipate, by means of natural convection, the heat generated by the power stage (buck and rectifier stages). During the design stage, the PCB is assumed to be square, though the aspect ratio may change during layout. The design increases the PCB area as necessary for each implementation to limit the temperature rise of the power stage to 80° C.

In the design and optimization, the receiver weight is assumed to be dominated by the Rx coil weight, PCB weight, and buck inductor weight. Fig. 4 shows the results of a design sweep, limited to V_{mid} from 22 V to 50 V. In the optimization,

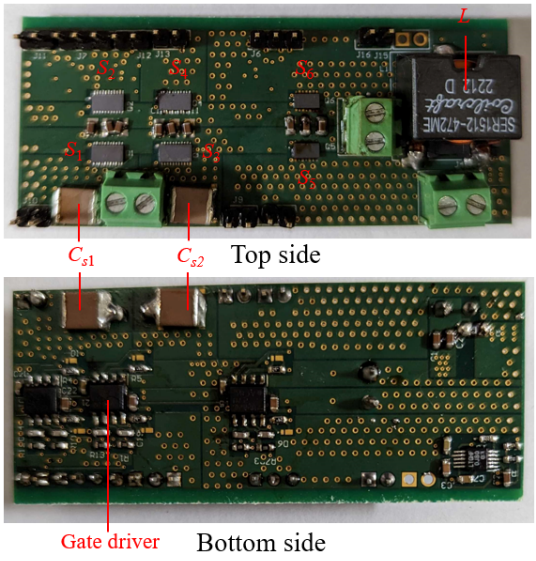


Fig. 6. Photograph of the receiver power stage.

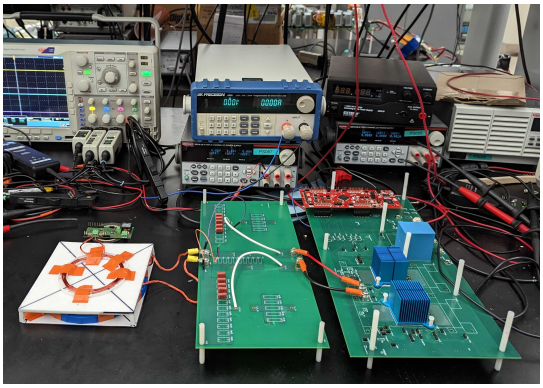


Fig. 7. System test setup.

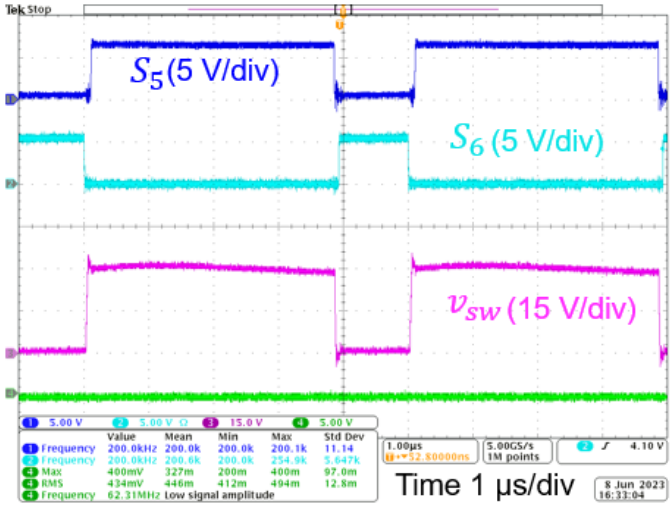


Fig. 8. Gate pulses and switch node voltage v_{sw} of the buck at 200 W for one full period.

the rectifier FET is chosen to minimize the device loss at at each value of V_{mid}. The buck FET and inductor are selected such that the PCB weight plus the inductor weight is minimized at each V_{mid}. Finally, the Rx coil geometries are iterated for each operating point, generated at each value of V_{mid}, combining the buck and rectifier stages.

For V_{mid} of 22 V to 30 V the Rx coil weight dominates the total weight of the receiver due to large current in the coil. Above 30 V the power stage weight dominates due to the increasing losses in the power stage.

The minimum weight operating point combining the power stage and Rx coil is found to occur at the point labeled in Fig. 4 with V_{mid} =30 V. Details of the design are given in Table III. The weights of the optimal PCB, inductor and Rx coil are 3.65 g, 7 g (from datasheet), and 8.01 g, respectively. The optimal Rx coil could be made arbitrarily lightweight by having a minimum area and number of turns. However, doing so requires increased transmitter current beyond feasible limits. The optimization is bounded by the allowed maximum temperature rise of 80°C for the Tx coil.

During PCB layout, to facilitate reduced switching parasitics and improved electrical performance, a 70 × 29 mm PCB is designed. This PCB area is the same as the optimal design, but in a non-square aspect ratio. To validate the application of the simplified thermal model, results of the model and a detailed Icepak thermal simulation are compared in Fig. 5, using the natural convection solver without any additional airflow. A thermal simulation for the total power stage loss applied to a 70 × 29 mm copper patch is shown in Fig. 5(a). In Fig. 5(c), the thermal simulation instead uses the top-layer copper pour and component geometry from the prototype layout. Comparing these two models, there is relatively minor error in maximum temperature, indicating the suitability of the simplified modeling framework used during the design stage.

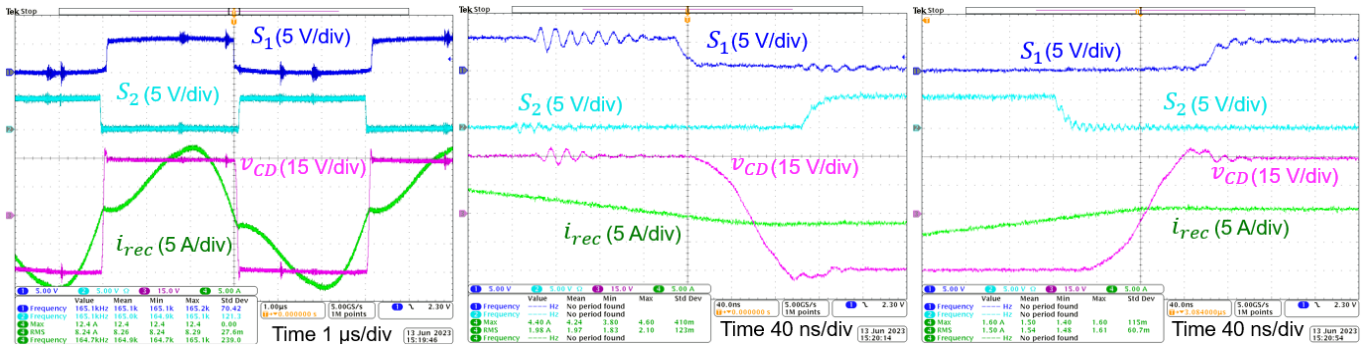
IV. Experimental Results

To verify the system modeling and design method, a 200 W prototype is constructed using the optimized parameters of every stage. The components are listed in Table IV. A photograph of the receiver power stage is given in Fig. 6. Fig. 7 shows the system experimental setup. The power stage has been tested with an electronic load at the output. The prototype has been tested up to 204 W without any additional cooling. The measured buck waveforms at full power are shown in Fig. 8. Measured waveforms of the rectifier at full power are shown in Fig. 9. From the zoomed-in waveforms in Fig. 9(b-c), it is evident that all the FETs turn on at zero voltage. Thermal photographs of the power stage, buck inductor, and Tx and Rx coils working at full power without any additional cooling are given in Fig. 10.

Fig. 11 details the weight breakdown of the receiver. The gravimetric power density of the entire receiver, excluding the weight of the connectors and headers, is 8.3 W/g. Including the weight of the connectors and headers, the gravimetric power density is 7.1 W/g. In both cases, the controller is excluded,

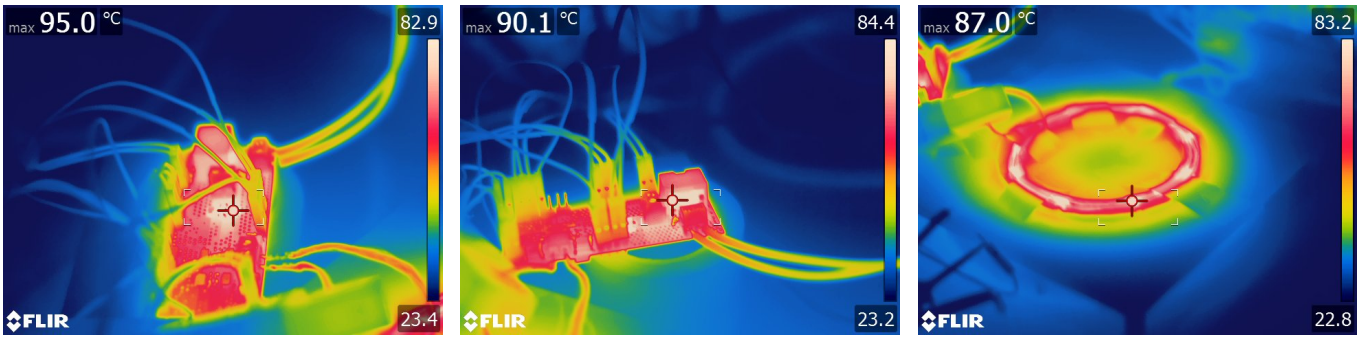
TABLE III
DETAILS OF THE SELECTED DESIGN

Rectifier FET	V_{mid}	Buck FET	Inductor	$f_{s,buck}$	PCB area	Rx coil	Rx coil wire
EPC2071	30 V	EPC2218	SER1512-472 4.7 μH	200 kHz	45 $\times$ 45 mm	4 turns, $d_{in,rx}$ = 7 cm	64/38 AWG Litz



(a) (b) (c)

Fig. 9. Gate pulses, i_{rec} and v_{cd} of the rectifier at 200 W: (a) one full period, (b) zoomed-in view of S_1 going low and S_2 going high transition, and (c) zoomed-in view of S_1 going high and S_2 going low transition.



(a) (b) (c)

Fig. 10. Thermal photographs at full power: (a) power stage thermal image focusing on the FETs, (b) power stage thermal image focusing on the inductor, and (c) thermal image of coils.

TABLE IV
PROTOTYPE COMPONENTS AND PARAMETERS

Component	Part number	Parameter	Value
S_5 and S_6	EPC2218	C_{s1} = C_{s2}	666.8 nF
S_1 – S_4	EPC2071	C_{mid}	90 μF
Inductor	SER1512-472	C_{out}	20 μF
Gate drivers	UCC27282-Q1	Rx coil	4 turns, $d_{in,rx}$ = 7 cm, 64/38 AWG Litz

though gate drivers and auxiliary power supplies are included on the PCB.

The measured and calculated dc-dc power transfer efficiency from inverter input to buck output at various output powers are shown in Fig. 12. The measured dc-dc efficiency at the full load operating point is 86.4 % and the peak efficiency is 87.9 %. This sweep is measured using a constant load resistance at the output and not at a constant V_{mid} or V_{out}.

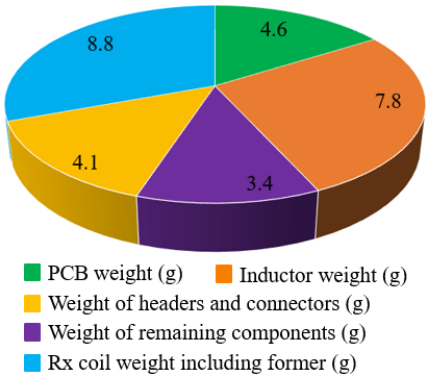


Fig. 11. Weight breakdown of the receiver.

The efficiency is relatively low, as expected, due to the design optimization prioritizing low weight as long as components remain within thermal limits.

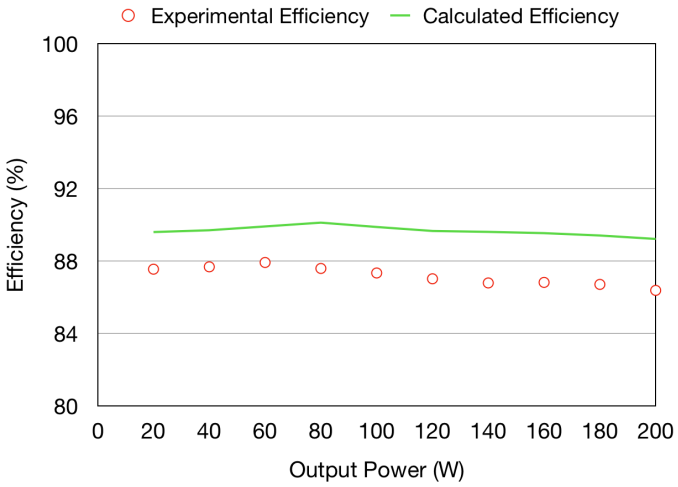


Fig. 12. Measured and calculated dc-dc prototype efficiency.

TABLE V
MEASURED OPERATING POINT VS. DESIGNED

Parameter	Designed	Calculated	Measured
$P_{loss,inv}$ [W]	–	2.94	–
P_{tx} [W]	–	12.28	–
P_{rx} [W]	3.24	5.19	–
L_s [μH]	2.97	–	2.56
$R_{ac,amb}$ [mΩ]	45.8	–	60
ΔT_{rx} [$^\circ$ C]	79.3	–	67
Rx coil weight[1][g]	8.01	–	8.8
$f_{s,wpt}$ [kHz]	160	–	165
$P_{loss,rec}$ [W]	0.39	0.66	–
V_{mid} [V]	30	–	29.72
$P_{buck,rec}$ [W]	2.16	2.35	–
$f_{s,buck}$ [kHz]	200	–	200
V_{out} [V]	22.2	–	22.2
ΔT [$^\circ$ C]	80	–	75
PCB weight [g]	3.65	–	4.6
Inductor weight [g]	7[†]	–	7.8
Power stage component weight [g]	–	–	7.5
P_{out} [W]	200	200	200
Receiver losses [W]	5.79	8.2	–
System losses [W]	–	23.42	31.59

[1] including coil former
[†] datasheet value

The measured operating point, along with the calculated (using prototype parameters) and the optimal design at 200 W, are summarized in Table V. The designed power stage loss is close to the calculation. Also, the prediction for power stage temperature rise is validated by the thermal simulations shown in Fig. 5, and prototype thermal performance. The designed and measured weights of the various components agree quite well. It is evident that the main source of discrepancy between the optimal design and calculation is the Rx coil loss and thermal model.

The Rx coil loss model is developed for a sinusoidal current and 1-D field. Also, the models assume near-resistive phase operation for the rectifier. These will result in inconsistency between the predicted and calculated losses of the Rx coil. Additionally, the additional impedance of the leads of the prototype Rx coil are not included in the model and design, causing discrepancy due to the low number of turns.

The coil thermal model is based on Ansys Icepak simulation results. The predicted temperature rise, which uses an R_{th} value for equivalent wire diameter of AWG 22, is higher than the simulation in Fig. 2 since the simulation is run for the actual equivalent wire diameter of AWG 20.

V. CONCLUSION

This article has shown that high gravimetric power density of a receiver for wireless drone charging application can be achieved through a systematic design and optimization method. From the results of the system-level design considering all stages simultaneously, a system is selected for experimental verification. The PCB, inductor and Rx coil weights have been modeled and validated by measurement. Also, measurements demonstrate the accuracy of the adopted power stage thermal model, and design method. The prototype has been tested up to 204 W without any external cooling. The gravimetric power density of the receiver excluding the weight of the connectors and headers is 8.3 W/g, and the power density is 7.1 W/g including the weight of the connectors and headers. In both measurements, sensing and control are excluded. The measured dc-dc system efficiency at 200 W is 86.4 % and the peak efficiency is 87.9 %. The designed power stage loss is close to the calculation. Efforts are being made to develop a better loss and thermal model for Litz wire coils. Also, in the future capacitor ESR and PCB trace resistance will be incorporated in the loss model to make the system loss model more accurate.

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