Fully Compensated Self-Resonant Coil with Low E-field and Low Profile for Consumer Electronics Wireless Charging

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***Abstract*—This paper details a fully compensated self-resonant coil (FSRC) with series LC resonance and reduced surface electric field for application in wireless power transfer for consumer electronics. By having a repeated series LC connection along the entire coil trace, the proposed series resonant structure achieves high-Q, low E-field, and thin profile simultaneously. The impact of ferrite shielding is also studied. Different E-field compensation coil geometries are studied, and a systematic design method is presented for optimal coil performance. Experimental tests verify the coil function, modeling, and design.**

***Index Terms*—self-resonant coil, WPT, low electric field, consumer electronics**

I. Introduction

In wireless power transfer (WPT) for consumer electronics applications like cell phones or laptops, onboard receiver coils must be designed to be low-profile and exhibit low stray field. The limited space available in compact mobile devices prevents the use of thick solid copper wire to reduce power loss. Both the WPT operation and nearby components are sensitive to leakage magnetic field and electric field. Magnetic leakage field causes eddy currents in neighboring metal or PCB traces, potentially destroying the magnetic coupling with the transmitter side.

Fig. 1 shows a prototype multi-receiver 6.78 MHz wireless charging station [1]. When a 50 W receiver is placed under an aluminum-body laptop, the induced voltage after rectification reduces 30-fold compared to results without the laptop, preventing charging. Prior research examines methods for integrating receiver coils into metal-chassis mobile devices using careful patterning of the case [2]–[5]. To protect magnetic coupling and reducing interference with neighbouring objects, without requiring patterning of the metal case, ferrite shielding can be employed on an external coil. The addition of ferrite to the system changes the coil induced voltage and self-inductance and must be considered when designing the coil.

In addition to the leakage magnetic field, the electric field, generated due to the voltage drop along the length of the coil, can interact with nearby sensitive electronics, including capacitive touch screens [6]. The leakage electric field also potentially causes dielectric loss in neighboring materials, such as the coil substrate, neighboring circuits, and ferrite shielding. To reduce leakage electric field, discrete distributed capacitors may be used to compensate the voltage potential of each turn [6]. Current commercial Airfuel receivers use distributed lumped capacitors, which introduces additional parasitic ESR as analyzed in [7]. The physical size of the capacitor (typically 0805 packages) significantly increases the coil height.

Fig. 1. Prototype WPT to a laptop with metal case.

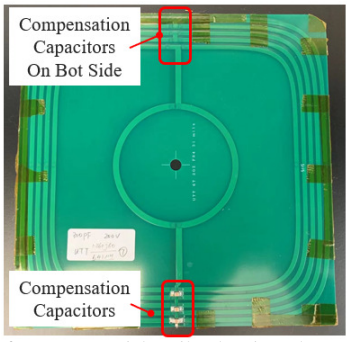
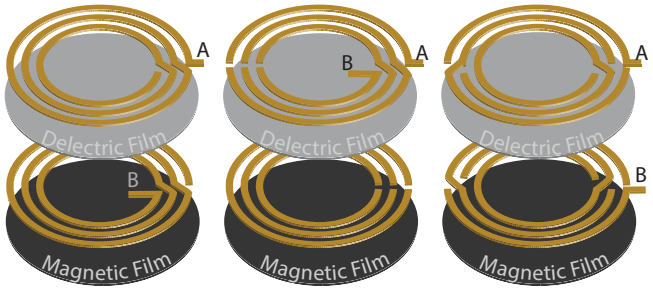


Fig. 2. Picture of a commercial coil, showing the repeated distributed compensation.

This paper presents the receiver coil and receiver-side design for laptop applications. The ferrite impact is modeled and included. In Section II, a novel self-resonant coil is proposed to achieve low profile, low E-field, and high Q. Complete electrical modeling and systematic design of the coil are detailed in Section III. Section IV presents a prototype that



a b c

Fig. 3. Comparison of self-resonant coil structures; (a) traditional series-self-resonant coil; (b) compensated series-self-resonant coil; (c) symmetric compensated series-self-resonant coil

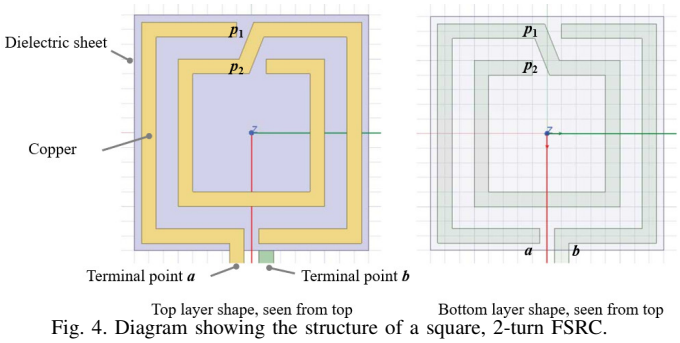


Fig. 4. Diagram showing the structure of a square, 2-turn FSRC.

validates the coil operation, modeling, and systematic design.

II. Proposed Coil Structure and Working Principles

In order to address the need for a thin coil with compensated electric field and shielded magnetic field, a new symmetric fully-compensated self-resonant coil structure is developed in this work. The structure is derived from prior two-layer series-self-resonant coil [8], and multi-layer series-self resonant coil [9] structures.

Fig. 3(a) gives an exploded view of a circular, 3-turn convention series self-resonant coil (CSRC) from [8] with magnetic shielding. The coil is formed by two copper spirals and a dielectric layer sandwiched between them. The terminals of the coil, A and B, are on opposite layers and opposite ends of the spirals. Any ac current path between terminals A and B traverses the 3-turn spiral once and crosses the dielectric layer once. Fig. 3(b) shows a half-turn compensated version of the series self-resonant coil. Gaps are places in each copper spiral such that the current paths between the coil terminals now cross the dielectric film multiple repeatedly every half-turn of the coil. This repeated crossing of the dielectric creates a distributed electric field compensation in the same manner as the multiple discrete capacitors in [6]. In this design, terminals are on the same layer, but opposite ends of the spiral. In height-contrained applictions, this terminal arrangement presents a challeng as an additional conductor layer is required to bring terminal B back to outside of the coil to connect to the power stage. Fig. 3(c) shows a symmetric version of the compensated coil. By aligning the gaps with the turn-to-turn connections, this implementation allows both terminals of the device to be on the outside of the coil.

Fig. 4 shows greater detail of a 2-turn, square, symmetric fully-compensated self-resonant coil structure (FSRC). The structure is created using a double-sided copper-clad dielectric laminate. The shape of the two copper coils is carefully designed to provide resonant inductance. The surface area of the copper and the dielectric material is carefully designed to form the resonant capacitors between the two copper layers. Terminals a and b on the outer extent of the coil and on opposite layers are connected to the ac source (e.g., WPT inverter).

Due to the complete separation of the two conducting layers by the dielectric, the coil is an open circuit for a dc source. When an ac source is applied, current flows from one terminal to the other crossing through the dielectric multiple times, resulting in a repeated series LC connection, and the total capacitance consists of three distributed parasitic capacitances in series. The three parasitic capacitor sections are: 1) point a to p_1, 2) point p_1 to p_2, and 3) point p_2 to b.

Similar to a parallel-plate capacitor, the current transitions between two layers in the form of displacement current $J_d = \varepsilon_r \varepsilon_0 \partial E/\partial t$ where ε_r is the relative permittivity of the dielectric material. As in the uncompensated conventional series self-resonant coil, [8], the electric field between the two copper layers is constant within each capacitor section, which leads to the uniform distribution of J_d along the length and width of the trace in each section.

Due to the uniform J_d in each capacitor section, the input current linearly transitions from the input terminal a on the top to the end of the first half turn, to the bottom layer at point p_1. At point a and p_1, the entire coil current flows through one of the conductors, with zero in the opposite conductor. In the next section, the current linearly transitions from the p_1 on the bottom conductor to the end of the inner turn to the top layer at point p_2. Then, the current linearly transitions from the p_2 on the top conductor to the end of the outer turn to the bottom layer at point b. At point p_2 and b, the entire coil current flows through one of the conductors, with zero in the opposite conductor.

The proposed current distribution on the two conductor layers is summarized in Fig. 5 showing current crossing the dielectric between top and bottom layers multiple times, resulting in series LC characteristic with distributed capacitance and reducing nearby fringing E-field [6].

Full-wave FEA simulation is used to verify the current distribution pattern. The results are shown in Fig. 6, which agree with the analyzed current distribution.

In Fig. 4 each half turn is compensated by a parasitic capacitor forming a fully compensated self-resonant coil. This structure potentially can be combined with conventional planar coil to for a new structure that compensates every other turn, forming a hybrid self-resonant coil (HSRC). Fig. 7

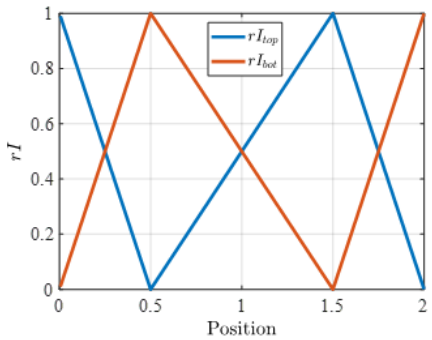
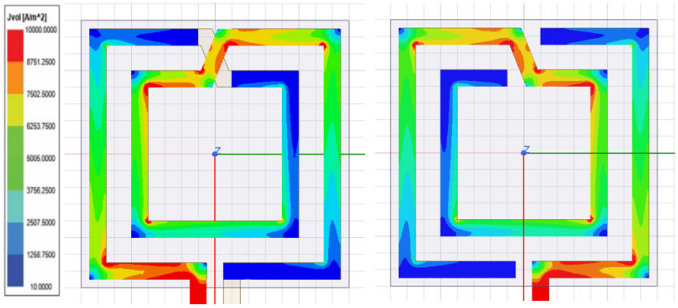
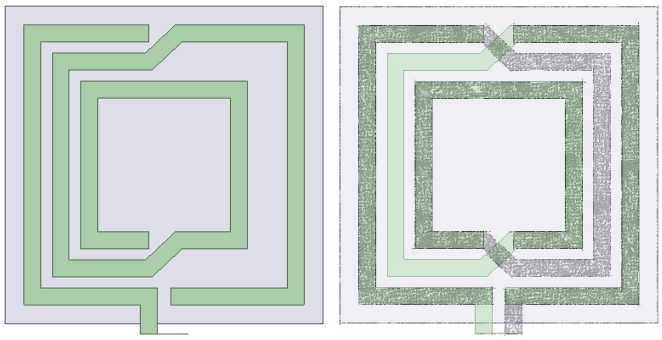


Fig. 5. Diagram showing the current distribution along the longitude change of coil length. rI is the fraction of the terminal coil current and the Position axis is relative to the number of turns in the coil.



a b

Fig. 6. Simulated current density distribution (a) top view, and (b) bottom view.



a b

Fig. 7. HSRC structure top view (a), and top view with transparent dielectric (b). The dashed grey trace represents the bottom layer seen through from the top.

shows a three-turn example where the voltage potential of the outermost and innermost turn is compensated by parasitic capacitors, but the middle turn is not compensated.

The symmetric FSRC has an additional series capacitance for each half-turn of the coil. Thus the total equivalent capacitance is small and it may be difficult to acquire the target capacitance and coil resonant frequency given geometric constraint. Compared to other self-resonant coils without repeated series capacitances, the FSRC will require thin, high-permittivity dielectric materials to achieve the same resonant frequency. Compared to the FSRC, the HSRC has a reduced

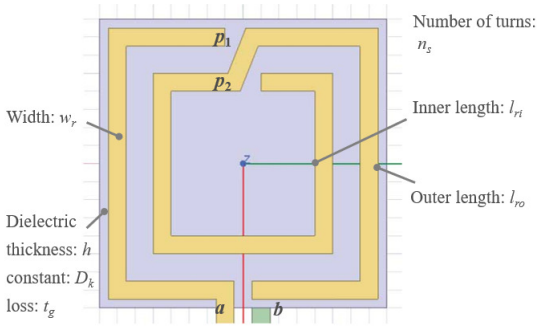


Fig. 8. Geometry of the proposed coil.

number of series capacitances, thus the maximum achievable capacitance is larger than FSRC with the same dielectric and geometry. Due to the reduced compensation, the leakage electric field for HSRC is larger than FSRC but is smaller than conventional coils.

III. Coil Modeling and Design Procedures

A. Coil LCR Modeling

The geometric parameters of the coil are shown in Fig. 8. w_r is the width of each turn, l_i is the inner length, and l_o is the outer length. n_s is the number of turns of one layer, and h_r is the thickness of the dielectric layer. t is the copper thickness. The dielectric constant and loss tangent are D_k and t_g, respectively.

To examine the performance capabilities, analytical models for the inductance, capacitance and resistance are developed based on results from the literature and FEA-assisted simulations. L is analyzed based on magnetic field simulation. C and R are analyzed based on comparison to existing self-resonant coils.

1) Inductance

The top and bottom layers of the proposed coil have identical current flow directions (i.e. from input terminal towards output terminal). Compared to a conventional PCB coil, the current flow in the proposed coil differs only in that it crosses vertically through the dielectric layer. When the dielectric thickness is thin relative to the width, the magnetic flux distribution of the proposed self-resonant coil and the traditional PCB coil are nearly identical. Fig. 9 is a magnetic field simulation comparing the flux distribution between a conventional single-layer coil (a) and a self-resonant coil (b), assuming both coils conduct 1 A 6.78 MHz current. Due to the identical flux distribution, the two coils have the same inductance.

The inductance of a conventional planar coil is modeled empirically in [10] with an error of less than 3%,

$$L_s = \frac{1.27\mu n^2(l_{ri}+l_{ro})}{4}\left(\ln\frac{2.07(l_{ri}+l_{ro})}{l_{ro}-l_{ri}} + 0.18\frac{l_{ro}-l_{ri}}{l_{ro}+l_{ri}} + 0.13\left(\frac{l_{ro}-l_{ri}}{l_{ro}+l_{ri}}\right)^2\right) \quad (1)$$

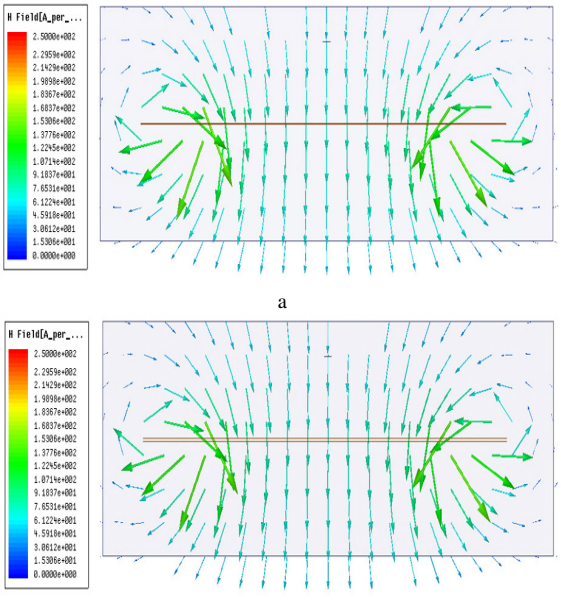


Fig. 9. Flux distribution of traditional coil (a), and the proposed self-resonant coil (b) when conducting 1 A, 6.78 MHz current .

where l_{ro} and l_{ri} are the outer and inner turn radii, respectively, as shown in 8.

2) Capacitance

Compared to a conventional self-resonant coil, FSRC has the same parallel-plate structure in each capacitor section of each half-turn. Thus, the capacitance of each section is modeled using the same method as a CSRC, which has been detailed in [8].

The i^{th} turn capacitance of a CSRC is [8]

$$C_i = \frac{D_k \varepsilon_0 w_r 4 l_{ri}}{h_r}\left[1+\frac{h_r}{\pi w_r}\ln\frac{2\pi h_r}{w_r}+ \frac{h_r}{\pi w_r}\ln\left(1+\frac{h_r}{2w_r}+2\sqrt{\frac{t}{h_r}+\left(\frac{t}{h_r}\right)^2}\right)\right] \tag{2}$$

For FSRC, the total capacitance is the series connection of each half turn and the innermost turn

$$C_{fsrc} = \frac{1}{\sum_{i=2}^{n_r}\frac{4}{C_i}+\frac{1}{C_1}} \tag{3}$$

For HSRC, the total capacitance is the serial connection of each half-turn that has a self-resonant structure, excluding the non-self-resonant turns. For HSRC, if the self-resonant turn is the odd number of turns, the capacitance is

$$C_{hsrc} = \begin{cases} \dfrac{1}{\sum_{i=2}^{n_r/2}\frac{4}{C_{(2*i-1)}}+\frac{1}{C_1}} & , n_r = 2k \\ \pm\dfrac{1}{\sum_{i=2}^{(n_r+1)/2}\frac{4}{C_{(2*i-3)}}+\frac{1}{C_1}} & , n_r = 2k+1 \end{cases} \tag{4}$$

where k is integer starting from 3.

3) Coil ESR

The total loss of the proposed self-resonant coil consists of copper loss and dielectric loss. The copper loss is modeled as skin-effect loss plus proximity effect loss [11]. The skin effect loss is calculated through the integration of the loss density over the whole coil. The proximity loss is through the calculation of the proximity field on each turn, and calculation of the proximity loss afterward.

As has been discussed, the input current linearly transitions from the top to bottom spiral over the whole length in each capacitor section, which is the same as in CSRC. Thus, skin-effect ESR of the i^{th} turn is, if configured as a self-resonant structure [8]

$$R_{skin,i} = \frac{2\rho_{copper} 4 l_{ri}}{3 w_r \delta (1-e^{-\frac{t}{\delta}})} \tag{5}$$

If the i^{th} turn is configured as a conventional structure as in a HSRC, the skin-effect ESR is

$$R_{skin,i} = \frac{\rho_{copper} 4 l_{ri}}{w_r \delta (1-e^{-\frac{t}{\delta}})} \tag{6}$$

The total skin-effect ESR is $R_{skin} = \sum_{i=1}^{n_r} R_{skin,i}$.

In addition to the skin effect, the time-varying H-field around the coil traces causes eddy current loss in the copper foil. Since the H-field in the FSRC coil has an almost identical H-field compared to a conventional coil (as shown in Fig. 9), the magnetic field distribution and the proximity related ESR are calculated using the same method as in a CSRC [8].

H_c is the H-field strength at the center point. H_{in} is the H-field strength at the innermost point. H_{out} is the outermost field. The H-field strength drop on each turn $dH = H_{in} - H_{out})/n$. According to [8],

$$H_c = \frac{nI_{in}}{(l_{ro}-l_{ri})}\ln\frac{\sqrt{l_{ro}^2+t^2}+l_{ro}}{\sqrt{l_{ri}^2+h^2}+l_{ri}} \tag{7}$$

$$H_{in} = H_c \exp^{\frac{l_{ri}}{l_{ro}}\left(0.4+0.15\ln\frac{l_{ro}}{4t+2h}\right)} \tag{8}$$

$$H_{out} = -H_c\left(0.4+0.08\ln\frac{l_{ro}}{4t+2h}\right)\exp^{\frac{l_{ri}}{l_{ro}}\left(1+0.125\ln\frac{l_{ro}}{4t+2h}\right)} \tag{9}$$

After obtaining the field distribution information, the proximity effect loss is calculated using the standard formula for eddy-currents in a lamination [11]

$$P_{prox,i} = \frac{B_{avg,i}^2 w_s^2 t^2}{24\rho} Vol_i \tag{10}$$

where Vol_i is the copper volume of the i^{th} turn,

$$Vol_i = 4(l_{i,in}^2 - l_{i,out}^2)t \tag{11}$$

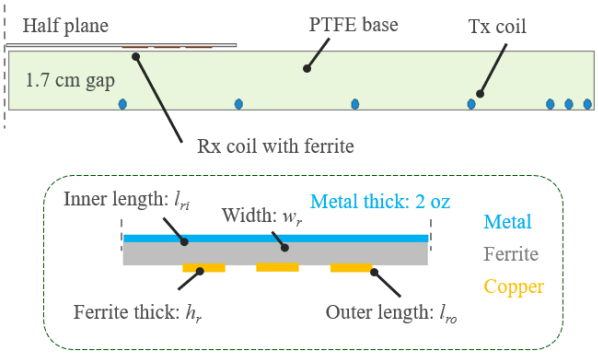


Fig. 10. Schematic showing Maxwell ferrite simulation [13].

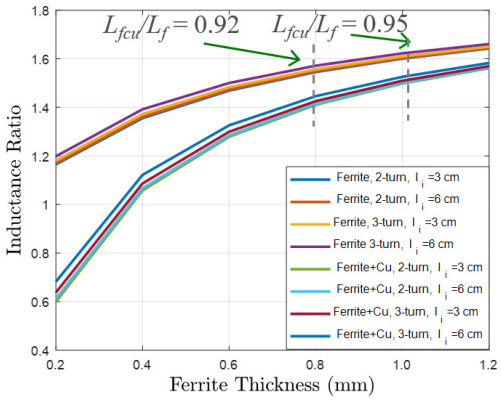


Fig. 11. Simulated ferrite impact on inductance

and $B^2_{avg,i}$ is the average peak flux density square of the proximal H-field

$$B^2_{avg,i} = \int_0^{w_r} \frac{\mu(Hl(i) + dH/w_r dl))^2}{w_r} = \mu^2 \left(Hl(i)^2 + \frac{(Hl(i) - Hr(i))^2}{3} + \Big(Hl(i) - Hr(i)\Big) Hl(i) \right) \quad (12)$$

The proximity effect ESR of i^{th} turn is

$$R_{prox,i} = \frac{2\sum_{i=1}^{n} P_{prox,i}}{I^2_{in}/2} \quad (13)$$

The total proximity-effect related ESR is $R_{prox} = \sum_{i=1}^{n_r} R_{prox,i}$.

The dielectric loss is calculated based on the loss tangent t_g of the dielectric material

$$R_c = \frac{t_g}{2\pi f C_s} \quad (14)$$

Finally, the total equivalent series resistance (ESR) of the coil is

$$R_s = R_{skin} + R_{prox} + R_c \quad (15)$$

B. Magnetic Shielding Effect

As mentioned previously, the neighboring metal may destroy magnetic coupling and requires ferrite shielding, which impacts the receiver coil inductance and induced voltage. To facilitate the proposed self-resonant coil design, FEA simulation using Ansys Maxwell 2D is used to quantify the impact. The simulated geometry is shown in Fig. 10, which includes the transmitter coil with a uniform magnetic field [1]. Due to the uniform magnetic field, the coupling is constant if the receiver coil is placed on other positions on the transmitter surface, or if the transmitter coil is configured with other geometries as long as the field is uniform. The ferrite is a high-frequency, low-loss material [12] with a permeability of 120. The metal is a 2 oz copper layer representing a 2-layer PCB. The length of the coil is 17.8 cm (7 inch) and the maximum height is 1.02 mm (0.04 inch).

In the simulation, the geometry of the coil and the thickness of ferrite are swept to evaluate the shielding effect of various ferrite thicknesses. The inner radius is swept from 3 cm to 6 cm. The number of turns is swept from 2 to 3. The width is designed for each geometry leaving a 2 mm gap between adjacent turns. The outer length is fixed at 8.9 cm (3.5 inch) based on the space available on the laptop. The inductance and induced voltage are evaluated and compared for two situations: 1) with ferrite only, and 2) with ferrite+copper. The results are shown in Fig. 11.

In Fig. 11 the inductance ratio is the inductance with ferrite only L_f over the inductance of the coil without any shielding L_0, or the inductance with ferrite and copper L_{fcu} over L_0. Without the copper layer, the ferrite shielding enhances the magnetic field, thus increasing the coil inductance for all ferrite thicknesses. The ferrite also forms a low impedance loop that facilitates more magnetic flux penetrating the Rx coil, leading to an increased induced voltage. With the copper layer, part of the magnetic flux that penetrates through the ferrite causes eddy currents leading to a reduced inductance and induced voltage if the ferrite is thin. Increasing the ferrite thickness reduces the penetrating flux to the copper and thus increases inductance and induced voltage. A 1 mm ferrite is sufficient to reduce L_{fcu}/L_f to 5 % and yields a voltage ratio of 0.95, and the improvement becomes increasing slow after this thickness. Considering this, a ferrite thickness of 1 mm is selected, which is also approaching the height limit of 1.02 mm. Both voltage and inductance ratios will be used in the systematic design.

C. Coil Design

The FSRC and HSRC coils developed in the prior sections are compared to conventional coil geometries in a target 6.78 MHz, 50 W receiver [1]. For each of the self-resonant coils, Rogers RO3003 dielectric is used. The substrate is 0.13 mm thick and has $D_k = 3$ and $t_g = .001$. Wurth 364003 RF ferrite sheet [12] is used for the magnetic shielding layer.

In the internal stage design, geometric iteration is used to calculate coil circuit parameters under application geometric requirements. Four types of coils are compared 1) solid copper

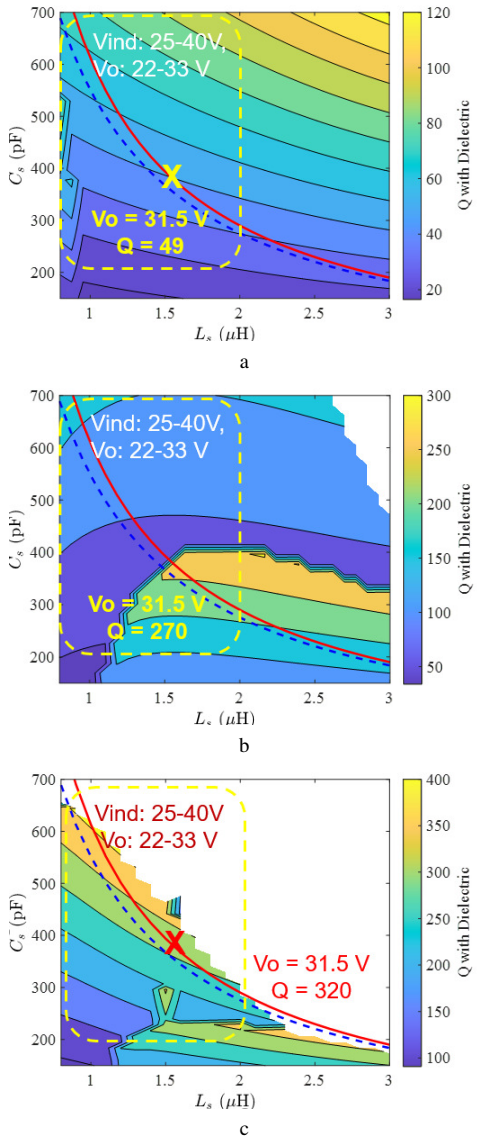


Fig. 12. Calculated coil circuit parameters for (a) CSRC, (b) HSRC, and (c) FSRC.

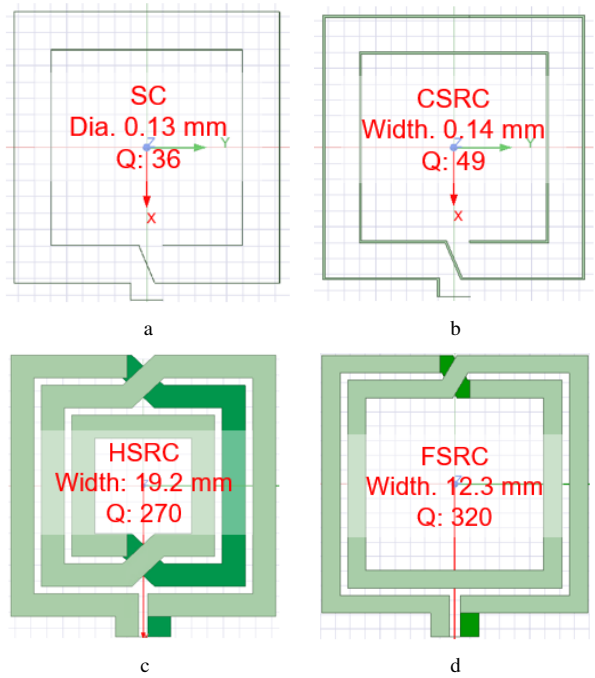


Fig. 13. Schematic showing 4 coil structures corresponding to x marker, SC (a), CSRC (b), HSRC (c), and FSRC (d).

wire coil, 2) conventional self-resonant coil (CSRC), 3) HSRC, and 4) FSRC. The modeling of 2) was reported in [8].

The design result for CSRC, HSRC, and FSRC are shown in Fig. 12, all resulting from geometric iteration.

The x symbols in Fig. 12 are designs with 1.60 μH, 360 pF, and 36 V induced voltage, which meet the requirements of the target applicaiton. A set of coil schematic corresponding to the x symbols are shown in Fig. 13.

With limited thickness, solid copper can only use thin wire and have limited conduction area, thus limiting the Q. CSRC configures the capacitors of every turn in parallel, requiring a limited capacitance from each turn, thus resulting in the thin width design. In comparison, HSRC and FSRC configure the capacitance of each turn (if any) in series, expanding the required capacitance of each turn, thus resulting in a wider traces than CSRC.

Combining the four coils, the resulting LCR design space is shown in Fig. 14(a) only showing the minimum ESR. The type of coil is shown in Fig. 14(b). Number 1 to 4 represents SC, CSRC, HSRC, and FSRC.

The complete coil performance capabilities shown in Fig. 14(a) are integrated into the prototype multi-receiver system from [1]. The optimal design is B_0 = 21 μT and yields a power loss of 6.94 W when 100 W are transferred two receivers. Note that the fabricated transmitter is configured at B_0 = 20 μT and results in a close power loss of 6.99 W. The receiver will be optimized for B_0 = 20 μT considering the tiny difference to the optimal point.

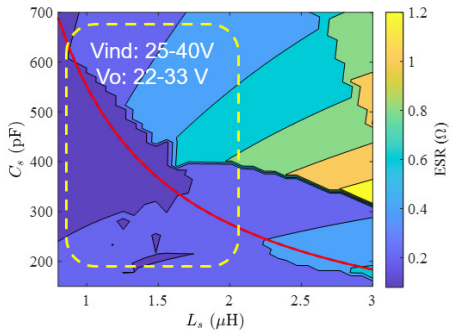
The design result for the metal-body laptop receiver are: L_s = 1.6 μH, C_s = 360 pF, ESR = 0.18 Ω, and V_o = 31.5 V. The target V_o is 31.5 V. The receiver coil structure is selected to be FSRC, with l_{ri}=5.47 cm, l_{ro} = 8.89 cm, w_r = 1.23 mm, and $n_r = 2$.

IV. Simulation and Experimental Verification

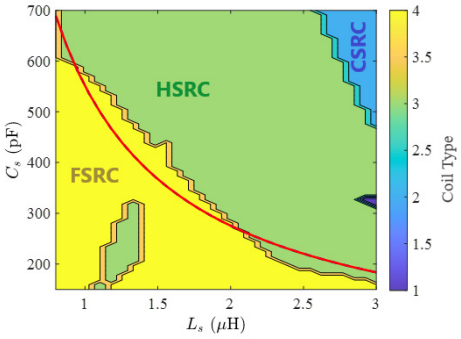
A. FEA Simulation Result

The proposed coils are simulated using Ansys HFSS. The top view of the schematic in the simulation is shown in Fig. 15. The bottom layer, viewed from the bottom, appears identical to the top layer due to the symmetric structure.

The impedance curve of the FSRC coil is shown in Fig. 16 directly imported from HFSS, showing series LC resonance. The y-axis is the impedance. The x-axis is the frequency range from 5.5 to 8.5 MHz. The simulated resonant frequency is 6.60 MHz (-0.5 %). Another simulation was done at 1 kHz, extracting the capacitance to be 378 pF(+5 %). From the



a



b

Fig. 14. Minimum ESR for each LC combination (a), and the corresponding type of coil (b)

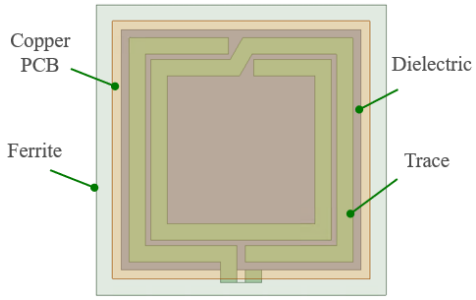


Fig. 15. HFSS simulation schematic.

simulated resonant frequency and capacitance, the inductance is calculated to be 1.54 μH(-3.8 %), illustrating the accuracy of the modeling. The FSRC coil alone, removing ferrite and copper, is also simulated. The results are summarized in Table. I, showing high accuracy. The ESR measurement of FSRC with ferrite is not accurate, due to additional ferrite loss which is not modeled.

B. Experimental Verification

To verify the coil design, a FSRC is fabricated using Rogers 3003 low-loss PCB laminate, as shown in Fig. 17(a). The coil impedance parameters are measured using an Agilent 4294A impedance analyzer and compared with the modeled and simulated predictions. As shown in Table I, the measurement results match well with the FEA simulation.

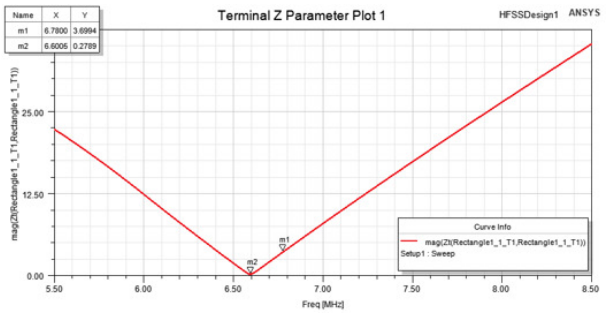


Fig. 16. HFSS simulation of the impedance.

TABLE I. Comparison of the measured and calculated circuit parameters.

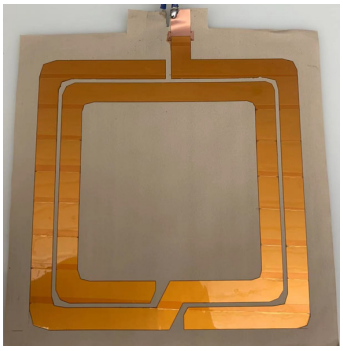
Parameters	Design	FEA	Measurement
FSRC resonance $f_{2,s}$ with shield (MHz)	6.63	6.6 (-0.5%)	6.61(-0.3%)
FSRC inductance $L_{2,s}$ with shield (μH)	1.60	1.54 (-3.8%)	1.56 (-2.5%)
FSRC capacitance $C_{2,s}$(pF)	360	378 (+5%)	372 (+5.7%)
FSRC ESR $R_{2,s}(\Omega)$	0.19	0.23 (+21%)	–
FSRC resonance $f_{2,s}$ w/o shield (MHz)	8.12	8.10 (-0.12%)	8.19 (-0.86%)
FSRC inductance $L_{2,ns}$ w/o shield (μH)	1.07	1.02 (-4.7%)	1.03 (-3.7%)
FSRC capacitance $C_{2,ns}$ w/o shield (pF)	360	380 (+5.6%)	370 (+3.3%)
FSRC ESR $R_{2,ns}$ w/o shield (Ω)	0.19	0.20 (+5.3%)	0.18 (-5.3%)

Fig. 17(b) presents the experimental setup, where the FSRC is implemented with the proposed rectifier and is tested with a 100 W 6.78 MHz wireless charging station as shown in Fig. 17b [1]. The FSRC implements one 50 W receiver used to power an aluminum-body laptop, while a solid-core coil with no ferrite is used for a second 50 W receiver used to power a plastic-body computer monitor.

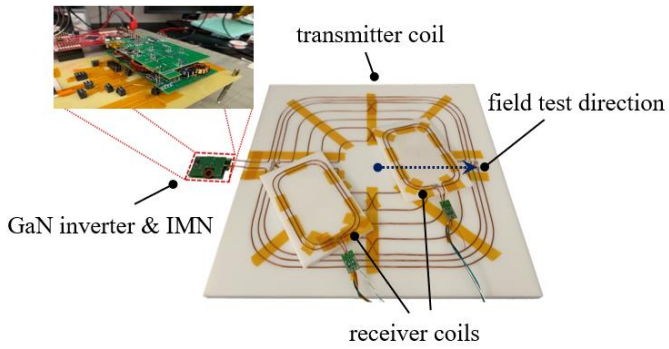
The system efficiency is defined as the total DC output power from all receivers divided by the transmitter side DC input power. Measured DC voltages and powers at the full load operating point are summarized in Table II, together with a comparison to the model predictions. The measured power loss is 7.94 W compared to the calculation value of 6.99, proving the accuracy of the system modeling and design. The additional loss might be caused by ferrite. According to the manufacturer, [12], the ferrite typically has a loss tangent smaller than 2 %. However, no detailed modeling of how the power loss changes with B was provided to accurately quantify ferrite loss. Another possible reason is that the ferrite increases FSRC coil ESR, as shown in the simulation. The measured system efficiency is 92.7 %.

V. Conclusions

This paper presents a novel self-resonant coil design for WPT charging of mobile electronics such as a laptop. The new structure achieves a high-Q, low E-field, and thin profile. The design results are verified experimentally for the proposed FSRC. The systematic design of a multi-receiver system wirelessly charging both a laptop and computer monitor is detailed



a Fabricated FSRC coil prototype.



b 100W wireless charging station.

Fig. 17. Hardware prototype and experimental setup with two conventional receiver coils.

TABLE II. COMPARISON OF MEASURED AND CALCULATED CIRCUIT PARAMETERS

Parameters	Variable	Design	Measure
Transmitter input voltage (V)	V_{dc}	200	201 (+0.5%)
Transmitter input power (W)	P_{in}	107.69	108.54 (+0.37%)
1st receiver output voltage (V)	$V_{o,1}$	31.5	31.1 (-1.3%)
1st receiver output power (V)	$P_{o,1}$	50	47.93 (-4.1%)
New receiver output voltage (V)	$V_{o,2}$	31.5	32.1 (+1.9%)
New receiver output power (W)	$P_{o,2}$	50	52.68 (-5.4%)

and a complete prototype of the FSRC is experimentally shown to achieve high efficiency.

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