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Analysis of 10 kV SiC MOSFET Module Baseplate Parasitic Capacitance Impact on Switching Loss

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***Abstract* — The parasitic capacitance of a power module baseplate provides a path for displacement current during the switching transient of the power module, which causes extra switching loss and EMI noise. It becomes an increasing concern especially for emerging 10 kV SiC MOSFET modules due to their high voltage and fast switching speed. This paper presents an in-depth analysis of 10 kV SiC MOSFET module baseplate parasitic capacitance impact on switching loss. The turn-on switching energy is divided into four parts, and the module baseplate parasitic capacitance impact on each part of the energy is analyzed. In addition to a constant capacitive energy (i.e., $\frac{1}{2}CV^2$), the module baseplate parasitic capacitance also introduces extra V-I overlap energy during voltage fall stage of the turn-on switching transient because it increases voltage fall time. This portion of loss is modeled and quantified. The module baseplate parasitic capacitance impact on switching loss is experimentally evaluated at 6 kV dc voltage and 0 to 50 A currents. This 10 kV SiC MOSFET module baseplate capacitance contributed loss is in the 5 - 10% range.**

Keywords — 10 kV SiC MOSFET, parasitic capacitance, switching loss model.

I. Introduction

High voltage (HV, >3.3 kV) silicon carbide (SiC) power semiconductor devices show higher blocking voltage and faster switching speed compared to their silicon (Si) IGBT counterparts [1-3]. As a result, the HV SiC MOSFET based converters show great benefit in efficiency, size, weight, and control bandwidth compared to Si IGBT based converters [4-8].

The parasitic capacitance of module baseplate provides a path for displacement current during the switching transient of the power module, which causes extra switching loss and EMI noise. This becomes an increasing concern especially for emerging 10 kV SiC MOSFET modules due to their high voltage and fast switching speed.

In [7], the importance of parasitic capacitance impact on the loss of a 10 kV SiC MOSFET based 100 kW 13.8 kV converter has been stated and analyzed. In [9], the parasitic capacitance introduced energy in the MV double pulse test (DPT) setup is studied. However, the switching energy is estimated directly using the measured parasitic capacitance current. This approach neglects the parasitic capacitance's impact on slowing device switching transient which causes extra V-I overlap energy. In [10], the switching energy of two custom packaged 10 kV single-die SiC MOSFET modules with different baseplate parasitic capacitances are analyzed in detail. However, the parasitic capacitance introduced extra V-I overlap energy is also not quantified.

This paper presents in-depth analysis of the module baseplate parasitic capacitance impact on switching loss of the Wolfspeed 10 kV 100 A multi-die XHV-9 SiC MOSFET half-bridge module as shown in Fig. 1. Section II provides analysis of the module baseplate parasitic capacitance impact on the switching energy. A model is proposed to estimate the module baseplate parasitic capacitance contributed extra V-I overlap energy. Section III presents experimental evaluation of the module baseplate parasitic capacitance impact on switching loss of this 10 kV SiC MOSFET module. Section VI concludes this paper.

Fig. 1. Wolfspeed 10 kV XHV-9 SiC MOSFET power module.

II. Modeling of Baseplate Parasitic Capacitance Impact on Switching Energy

A. Baseplate Parasitic Capacitance Impact on Turn-on Switching Transient

The turn-on switching transient of a SiC MOSFET can be divided into four stages: (1) turn-on delay stage, (2) current rise stage, (3) voltage fall stage, and (4) ringing stage. Fig. 2 shows the turn-on waveform of the 10 kV SiC MOSFET module conducted at 6 kV 40 A with the four stages labeled. The turn-on delay stage and ringing stage will not generate energy while the current rise stage and voltage fall stage will generate energy loss.

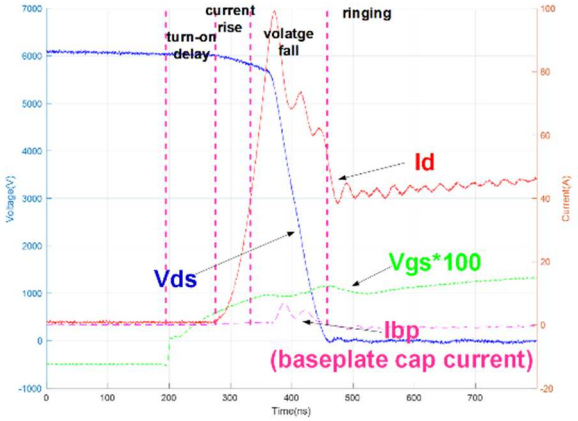


Fig. 2. Turn-on waveform of the 10 kV module conducted at 6 kV 40 A.

Fig. 3(a) describes the module baseplate parasitic capacitances of the studied 10 kV SiC MOSFET module. C_{ph} represents the module positive power terminal (module high side device drain terminal) to baseplate parasitic capacitance. C_{mh} and C_{gdmh} denotes the module middle power terminal (switching node) to baseplate parasitic capacitance and the module high side device gate driver to baseplate parasitic capacitance, respectively. C_{nh} and C_{gdnh} represents the module negative power terminal (module low side device source terminal) to baseplate parasitic capacitance and the module low side device gate driver to baseplate parasitic capacitance, respectively. Note that C_{gdmh} and C_{gdnh} are very small (e.g., < 1 pF) and can be neglected.

The baseplate is connected to the module negative power terminal. This helps to limit the switching node injected displacement current to within the module during switching transient and thus mitigating EMI noise. In the DPT setup, the module negative power terminal is grounded. Z_{gnd} denotes the impedance of the connection wire from baseplate to module negative power terminal.

Fig. 3 (b) shows the equivalent impedance network. Since Z_{gnd} is very small, the potential of the module baseplate is almost equal to ground potential. The baseplate displacement current during switching transient is mainly determined by C_{mh} and C_{gdmh} which is the parasitic capacitance between the switching node and baseplate. This parasitic capacitance is called baseplate capacitance C_{bp} for simplification. The measured C_{bp} of the studied 10 kV SiC MOSFET module is 55 ρF.

During voltage fall stage, the current paths are described as Fig. 4. i_{rr} denotes the high side device body diode reverse recovery current. i_{c_H} represents the high side device junction capacitance charging current. I_L is load current. i_{ch_L}, i_{C_L}, and i_{bp} are the low side device channel current, junction capacitance discharging current, and baseplate capacitance discharging current, respectively. Note that the DPT inductor parasitic capacitance is not shown in Fig. 4. It is in parallel with the high side device junction capacitance. If the DPT inductor parasitic capacitance is very small, its impact can be neglected.

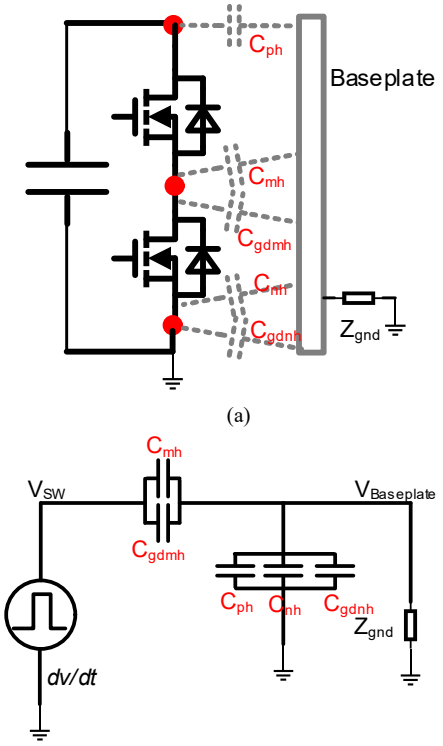


Fig. 3. (a) Baseplate related parasitic capacitances of the 10 kV half bridge module. (b) Equivalent impedance network.

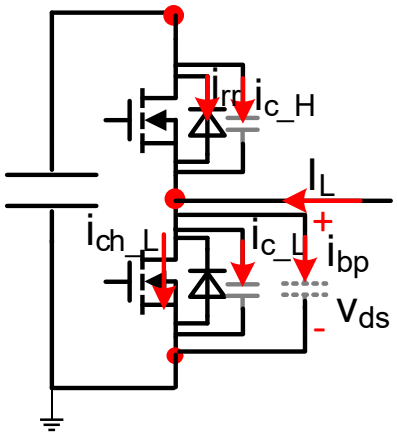


Fig. 4. Current paths during voltage fall stage of turn-on switching transient.

To help better understand baseplate capacitance impact on switching loss, the turn-on energy is separated into four parts.

(1) E_{on1}: V-I overlap energy during the current rise stage. The calculation of E_{on1} is expressed as

$$E_{on1} = \int_{t_{cr1}}^{t_{cr2}} v_{ds} i_d dt \quad (1)$$

where t_{cr1} and t_{cr2} represents the start and end time of the current rise stage, respectively. v_{ds} and i_d are the measured low side device drain-source voltage and drain current, respectively.

(2) E_{on2}: Constant load current contributed V-I overlap energy during the voltage fall stage. The calculation of E_{on2} is expressed as

$$E_{on2} = \int_{t_{vf1}}^{t_{vf2}} v_{ds} I_L dt \quad (2)$$

where t_{vf1} and t_{vf2} represents the start and end time of voltage fall stage, respectively.

(3) E_{on3}: High side device junction capacitance charging current and body diode reverse recovery current contributed energy during the voltage fall stage. Based on the direction defined in Fig. 4, the calculation of E_{on3} is expressed as

$$E_{on3} = \int_{t_{vf1}}^{t_{vf2}} v_{ds}(i_d - I_L) dt \quad (3)$$

(4) E_{on4} : Baseplate capacitance discharging energy during the voltage fall stage. The calculation of E_{on4} is expressed as

$$E_{on4} = \int_{t_{vf1}}^{t_{vf2}} v_{ds} i_{bp} dt = \frac{1}{2} C_{bp} V_{dc}^2 \quad (4)$$

E_{on1} is not impacted by the baseplate capacitance. During current rise stage, voltage v_{ds} is equal to dc bus voltage if neglecting the voltage drop on loop inductance. i_d is equal to the channel current which is determined by gate voltage. The gate voltage slew rate is determined by input capacitance which is not impacted by the baseplate capacitance.

E_{on2} is impacted by the baseplate capacitance. During voltage fall stage, baseplate capacitance discharge process will slow the voltage fall process. Although I_L is constant, v_{ds} is impacted by the baseplate capacitance. Thus, extra constant load current contributed V-I overlap energy is introduced, which is called E_{on2_extra}. Modeling of this part of loss is discussed in the next section.

The baseplate capacitance impact on E_{on3} is neglectable although the baseplate capacitance will impact the voltage fall process of voltage fall stage . E_{on3} contains two parts as

$$E_{on3} = E_{qoss} + E_{rr} \quad (5)$$

where E_{qoss} represents the high side device junction capacitance discharging current generated energy on low side device channel. E_{rr} is the high side device body diode reverse recovery current generated energy.

E_{qoss} is a capacitive energy and keeps constant for a given dc voltage since the stored charge on the capacitor only charges with the dc voltage. The change of voltage fall time will only result in the change in current magnitude that the parasitic capacitance are being charged.

Diode reverse recovery current is mainly determined by di_F/dt. i_{rr} can be considered not impacted by baseplate capacitance since the low side device channel current slew rate (which is the same as high side device body diode current slew rate) during current rise stage is determined by gate voltage which is not impacted by baseplate capacitance. E_{rr} could still be impacted by baseplate capacitance which need further investigation. However, for the 10 kV SiC MOSFET, E_{rr} is very small compared with E_{qoss}. Therefore, E_{on3} can be considered not impacted by baseplate capacitance.

The calculation of E_{rr} is briefly introduced. Based on (3) and (5), E_{rr} can be obtained if E_{qoss} is known. E_{qoss} can be estimated by

$$E_{qoss} = \int_0^{V_{dc}} (V_{dc} - v_{ds}) C_{oss} dv_{ds} \quad (6)$$

where C_{oss} is the device junction/output capacitance. Another simple and more accurate method to estimate E_{qoss} is to use the first pulse of DPT calculation. As the first pulse turn-on transient is actually zero current turn-on and there is no load current contributed V-I overlap energy and device body diode reverse recovery energy. Then E_{qoss} is calculated by

$$E_{qoss} = E_{pulse1} - E_{C_{bp}} \quad (7)$$

where E_{pulse1} is the total turn-on energy of the first pulse and $E_{C_{bp}}$ is the baseplate capacitance energy (i.e., $\frac{1}{2} C_{bp} V_{dc}^2$).

As an example, at 6 kV 40 A test points, the calculated E_{on3}, E_{qoss}, and E_{rr} are 13.63 mJ, 12.54 mJ, and 1.09 mJ, respectively. E_{rr} is only 8% of E_{on3}.

E_{on4} is a constant capacitive energy and is determined by baseplate capacitance and the given dc voltage.

B. Baseplate Capacitance Introduced Extra V-I overlap Energy Modeling

To quantify the baseplate capacitance introduced extra V-I overlap energy, how the baseplate capacitance impact v_{ds} during voltage fall stage need to be determined. Two cases – one with baseplate capacitance and another without baseplate capacitance – are investigated.

For the case with baseplate capacitance, based on Fig. 4, the low side device channel current i_{ch_L} can be expressed as

$$i_{ch\_L} = i_{c\_H} + i_{rr} + I_L - i_{c\_L} - i_{bp} \quad (8)$$

For the case without baseplate parasitic capacitance, the module lower device channel current i'_{ch_L} can be expressed as

$$i'_{ch\_L} = i'_{c\_H} + i'_{rr} + I_L - i'_{c\_L} \quad (9)$$

Based on the discussion in last section, i_{ch_L} and i'_{ch_L} can be considered equal. i_{rr} and i'_{rr} can be also considered equal.

Defining

$$i_{eq}(t) = i_{ch\_L} - I_L - i_{rr} \quad (10)$$
$$i'_{eq}(t) = i'_{ch\_L} - I_L - i'_{rr} \quad (11)$$

$i_{eq}(t)$ and $i'_{eq}(t)$ can be also considered equal for the two cases.

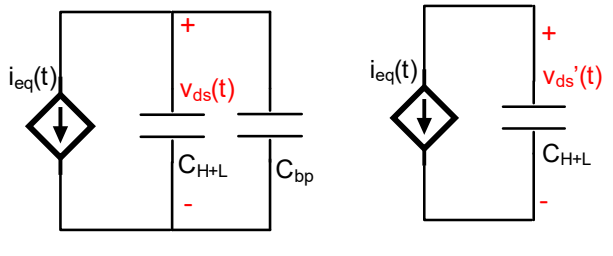
Based on (8)-(11), the equivalent circuit for the two cases is drawn as Fig. 5. C_{H+L} represents the switching node capacitance. The low side device junction capacitance C_L, high side device junction capacitance C_H (as a function of low side device voltage), and the total switching node capacitance C_{H+L} are shown in Fig. 6. $v_{ds}(t)$ and $v'_{ds}(t)$ represents the low side device drain-source voltages for the cases with and without baseplate parasitic capacitance, respectively. Since the current sources in the two cases are the same, the existence of baseplate current reduces the current flowing through C_{H+L} slowing the voltage fall transient and leading to higher constant load current V-I overlap loss.

$v'_{ds}(t)$ Using the backward Euler method, (12)-(15) are obtained.

$$i = \frac{dq}{dt} = \frac{d(C(v)\cdot v)}{dt} \quad (12)$$
$$i_{k+1} = C(v_k)\frac{v_{k+1} - v_k}{\Delta T} \quad (13)$$
$$C_{H+L}(v'_k)\frac{v'_{k+1} - v'_k}{\Delta T} = (C_{H+L}(v_k) + C_{bp})\frac{v_{k+1} - v_k}{\Delta T} \quad (14)$$
$$v'_{k+1} = \frac{(C_{H+L}(v_k) + C_{bp})}{C_{H+L}(v'_k)}(v_{k+1} - v_k) + v'_k \quad (15)$$

Thus,$v'_{ds}(t)$ can be estimated using measured $v_{ds}(t)$ for voltage fall stage based (15). Then, baseplate capacitance introduced extra constant load current V-I overlap E_{on2_extra} is calculated as

$$E_{on2\_extra} = \int_{t_{vf1}}^{t_{vf2}} (v'_{ds} - v_{ds}) I_L dt \quad (16)$$



(a) (b)

Fig. 5. Equivalent circuit during voltage fall stage. (a) With baseplate parasitic capacitance. (b) Without baseplate parasitic capacitance.

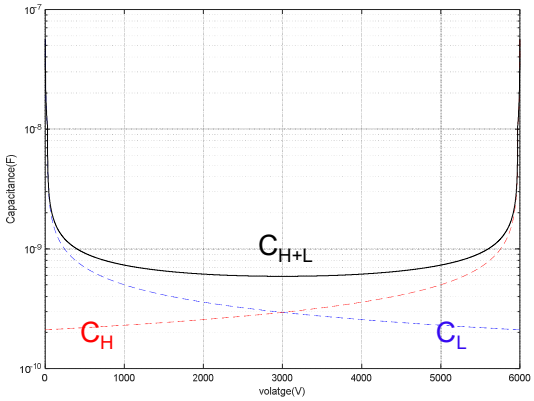


Fig. 6. Curves for C_L, C_H, and C_{H+L}

C. Turn-off Loss Discussion

The turn-off switching transient of a SiC MOSFET can also be divided into four stages: (1) turn-off delay stage, (2) voltage rise stage, (3) current fall stage, and (4) ringing stage. The analysis on baseplate capacitance impact on turn-off loss will be very similar to that of turn-on loss and is not repeated here.

Note that the baseplate capacitance charging current will not flow through the device channel and will not introduce joule heating during the turn-off switching transient. This part of energy is stored and dissipated during the next turn-on switching transient.

The channel current portion V-I overlap contributed energy will increase as the baseplate capacitance slows the voltage rise stage. However, the channel current will rapidly decrease to zero during the turn-off switching transient of this 10 kV SiC module, and this part of loss is very small. The turn-off switching transient is dominated by load current charging/discharging the junction capacitances process and this part of loss is not impacted by the baseplate capacitance.

Therefore, because the channel current portion V-I overlap energy is quite a small portion of total turn-off energy, the baseplate capacitance impact on turn-off loss is considerably small and does not have significant impact on the total turn-off loss. Note that the turn-off loss is also very small compared with turn-on loss of this 10 kV SiC MOSFET module.

III. Experimental Evaluation

Fig. 7 shows the DPT hardware setup with the studied 10 kV SiC module. DPT at 6 kV dc bus voltage and different load currents from 0 to 50 A are conducted. The turn-on waveforms at 6 kV 40 A test point is shown in Fig. 2. Based on the models developed in Section II A, the defined four parts of turn-on switching energy are shown in Fig. 8. E_{on2} and E_{on3} are the two dominant parts of turn-on switching

energy. E_{on1} and E_{on2} are load dependent while E_{on3} and E_{on4} are almost load independent.

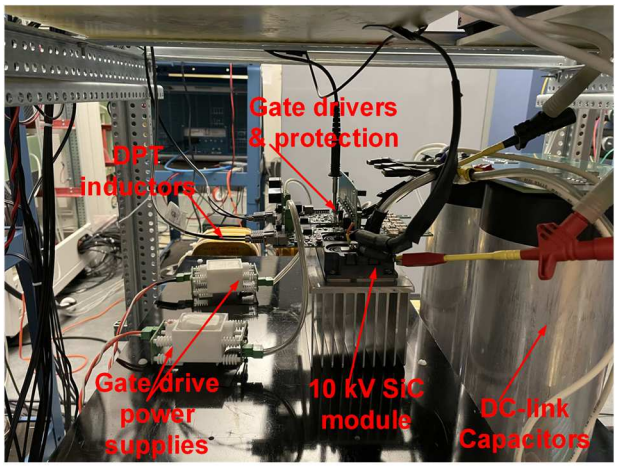


Fig. 7. 10 kV SiC module based DPT test platform.

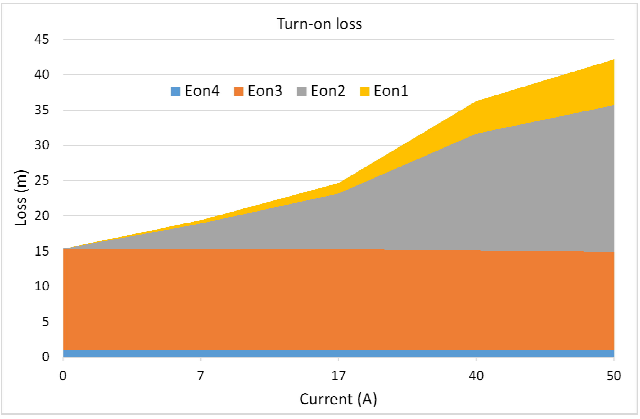


Fig. 8. The four parts of turn-on switching energy of the 10 kV SiC module at 6 kV voltage and different load currents.

Based on the models developed in Section II B, $v'_{ds}(t)$ is estimated based on the tested $v_{ds}(t)$ at 6 kV and different load currents. The 6 kV 40 A test point waveforms are shown in Fig. 9. Due to the existence of baseplate capacitance, $v_{ds}(t)$ is slowed compared with $v'_{ds}(t)$ during the voltage fall stage and extra constant load current contributed V-I overlap energy is introduced. At the 6 kV 40 A test point, the total turn on energy E_{on} is 35.77 mJ and E_{on1}, E_{on2}, E_{on3}, and E_{on4} are 4.63 mJ, 16.54 mJ, 13.63 mJ, and 0.97 mJ, respectively. The baseplate parasitic capacitance introduced extra constant load current contributed V-I overlap loss E_{on2_extra} is 1.29 mJ.

Fig. 10 summarizes the two portion of loss (E_{on4} and E_{on2_extra}) induced by the baseplate parasitic capacitance at 6 kV voltage and different loads. E_{on2} is almost load independent while E_{on2_extra} is load dependent. In general, the baseplate capacitance contributed loss is in the 5 - 10% range of the total switching loss at various loads (0 to 50 A) for this 10 kV SiC module.

Fig. 11 shows the turn-off energy at 6 kV voltage and different load currents. E_{oss} is the estimated device junction capacitances charging/discharging contributed energy during turn-off switching transient, and E_{off1} is the remaining V-I overlap energy.

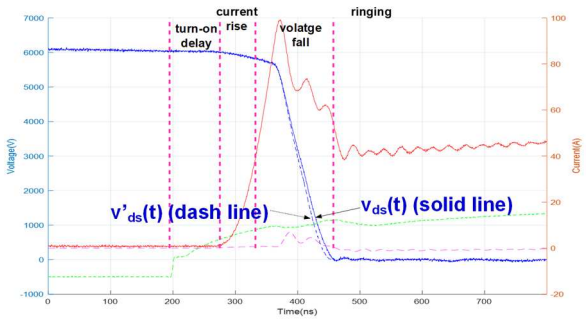


Fig. 9. Calculated $v'_{ds}(t)$ based on $v_{ds}(t)$ at 6 kV 40 A point.

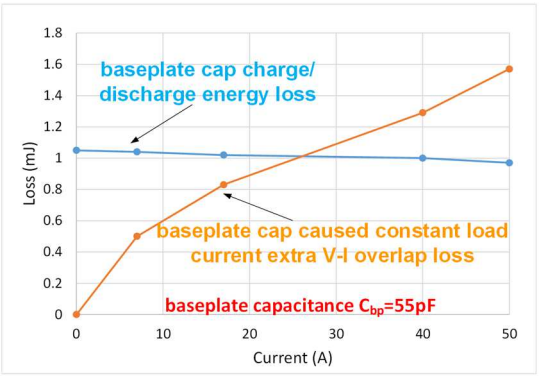


Fig. 10. Summary of baseplate capacitance introduced switching energy E_{on4} and E_{on2_extra} at 6 kV voltage and different load currents.

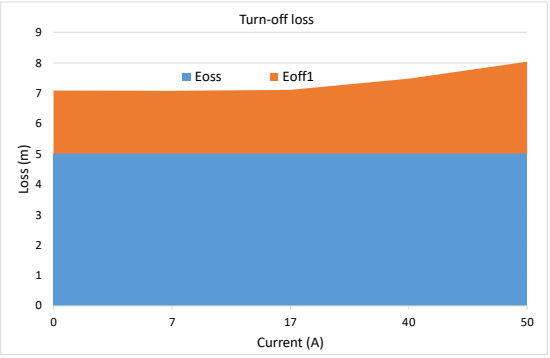


Fig. 11. Turn-off energy at 6 kV voltage and different load currents.

IV. Conclusion

This paper presents an in-depth analysis of 10 kV SiC MOSFET module baseplate parasitic capacitance impact on switching loss. The turn-on switching energy is divided into four parts, and the module baseplate parasitic capacitance impact on each part of the energy is analyzed. The module

baseplate parasitic capacitance will introduce not only a constant capacitive energy (E_{on4}) but also an extra constant load current contributed V-I overlap energy (E_{on2_extra}) during the voltage fall stage of turn-on switching transient because it slows the voltage fall transient. This portion of loss is quantified and experimentally evaluated at 6 kV voltage and different load currents. In general, this 10 kV SiC MOSFET module baseplate parasitic capacitance contributed switching loss is in the 5 - 10% range. The developed models and experimental evaluation provide better understanding of 10 kV SiC module baseplate impact on switching loss and accurate estimation of 10 kV SiC module based MV converter loss.

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