Design and Testing of a 6.5 kV Submodule Based on a 10 kV SiC Power Module

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2023 IEEE Energy Conversion Congress and Exposition (ECCE) | 979-8-3503-1644-5/23/$31.00 ©2023 IEEE | DOI: 10.1109/ECCE53617.2023.10362471

***Abstract*— This paper presents a half-bridge submodule design based on a 10 kV SiC MOSFET XHV-9 power module. The design of the gate driver, isolated power supply, and busbar are presented. High voltage insulation capability, fast short circuit protection, and resilience to EMI of the designed submodule are demonstrated through continuous power tests at 6.5 kV, 57 A and through a short circuit test. This submodule verification facilitates the adoption of high-voltage SiC MOSFETs in medium-voltage (MV) converters, shedding light on highly efficient power conditioning systems (PCS) for grid applications.**

Keywords—10 kV SiC MOSFET, Submodule, Isolated power supply, Busbar, Desat protection

I. INTRODUCTION

PCS serving as the interface between distributed energy resources (DER) and the MV distribution grid can support voltage and frequency ride through, mode transition, and isolation of unbalanced loads and faults [1][2]. Even though control strategies and grid level benefits have been widely researched [3], there is still not much hardware design discussion of the PCS converter [4]. The studied PCS converter consists of a back-to-back 1 MW 5-level MMC as shown in Fig. 1. Detailed specifications of the PCS are listed in Table I. By utilizing 10 kV SiC power modules, the PCS is able to reach 25 kV dc voltage with reduced number of switching devices. Also, its fast switching speed reduces switching loss and increases control bandwidth.

The MMC operation involves inserting and bypassing submodules to generate the required output voltage. The basic element of MMC, which is a submodule, is built and tested first to verify the feasibility of the design. Later, multiple submodules and arm inductors are assembled to form the full converter.

The MMC half bridge submodule consists of the power module, gate driver, auxiliary power supply (APS), busbar, submodule capacitors, cooling system, and a voltage sensor. The power module is a 10 kV, 100 A half bridge in XHV-9 packaging provided by Wolfspeed.

The submodule design poses several challenges, including the protection of devices, high voltage insulation, and EMI tolerance. SiC MOSFET has shorter overcurrent withstand time compared to Si counterpart due to its smaller die area. Thus, an effective and fast protection is necessary to prevent the device from damage. Desat protection has been verified for previous devices with lower voltage (1.7 kV [5]) or lower current rating (10 kV, 10 A [6]); it has not been demonstrated for 10 kV, 100 A devices.

APS and busbar require high voltage insulation, which is challenging as dielectric material degrades faster under high-frequency PWM voltage [7]. The state of art design of APS employing conventional transformer isolation usually encapsulates the transformer with high voltage insulation material under vacuum pressure potting to sustain high voltage PWM. In [8], a multiple layer laminated PCB busbar has a varied net-net internal layer spacing to constrain the electric field strength. This would require substantial simulation effort. In this design, the busbar structure is simplified by separating the AC midpoint from the busbar layers to reduce the exposure of PWM voltage on FR4 materials. Insulation coordination between components at different voltage potentials is also important in preventing potential arching faults [9].

The third challenge is the strong EMI noise induced by high switching frequency and fast switching transients of the 10 kV SiC MOSFET. High common mode current through the APS isolation capacitance result in interference to gate driver and APS and may cause malfunction of them. Isolation capacitance of APS is often required to be less than 5 pF for MV converter applications. Sensors are also prone to failure or inaccuracy in this type of harsh environment [10]. A robust voltage sensor with sufficient EMI tolerance and accuracy is critical for sampling submodule voltage and voltage balancing control.

In this paper, a 6.5 kV submodule is developed with desat protection, high insulation capability and EMI resilience. The design process of gate driver, APS, and busbar are discussed in section II, section III, and section IV, respectively. Finally, double pulse tests (DPTs) and continuous test results are presented in section V.

TABLE I - MMC Based PCS Specifications

Parameters	Values
Power rating	1 MVA
DC link voltage	25 kV
AC output voltage	13.8 kV
Submodule number per arm	4

Submodule voltage	6.5 kV
Submodule capacitance	90 uF
Arm inductance	5 mH

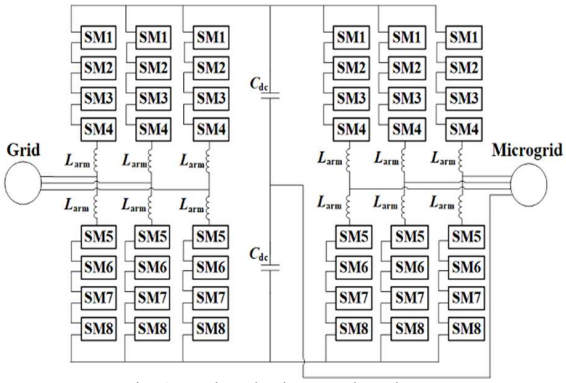


Fig. 1. Back-to-back MMC based PCS.

II. Gate Driver Design

Gate driver receives a switching signal from the controller and returns a feedback signal via optical fiber. Optical fiber achieves voltage isolation between the power device and control signal as well as maintaining signal integrity under high EMI environment. To effectively drive the power module, which has a large gate source capacitance due to six dies in parallel, sufficient driving voltage and current are necessary. Gate driver IC IXDD630YI is selected for its peak driving current of 25 A at 15 V input. Turn on voltage is +15 V and turn off voltage is -5 V respectively.

A. Desat Protection

The overcurrent protection function for SiC MOSFETs is realized through de-saturation (desat) protection because of its simplicity, good noise immunity, and fast response time. Other methods, for example, protection relying on Rogowski coil sensor demands much more strenuous isolation design between the Rogowski coil and power terminal in 10 kV power module [11].

The desat protection in this case has a threshold voltage of 7.5 V, which is device drain source voltage plus the voltage drop of desat diodes. The drain source voltage is based on the forward conduction characteristic tested at 100℃ in Fig. 2 to prevent false triggering at lower junction temperatures. Desat diode consists of three 3.3 kV SiC Schottky diodes in series to achieve the required blocking voltage as well as reducing parasitic capacitance to prevent mis triggering of desat protection [12]. Short circuit withstands time is 3.5 μs for this type of 10 kV power module with similar packaging. To protect the device from overcurrent as much as possible, the designed desat protection response time is less than 1 μs.

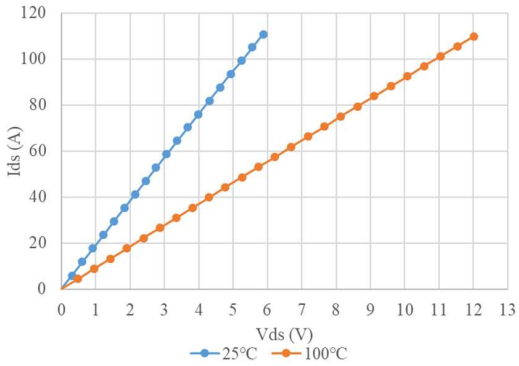


Fig. 2. Forward conduction curve of 10 kV SiC power module.

B. Gate Driver Layout

The gate driver boards are separated for the top device and the lower device. They are attached to the Kelvin source gate terminal of the power module, while the decoupling board and PCB busbar are attached to the power terminals. In this way, the gate loop is separated from the power loop to mitigate EMI disturbance. The desat diode board is placed vertically as shown in Fig. 3.

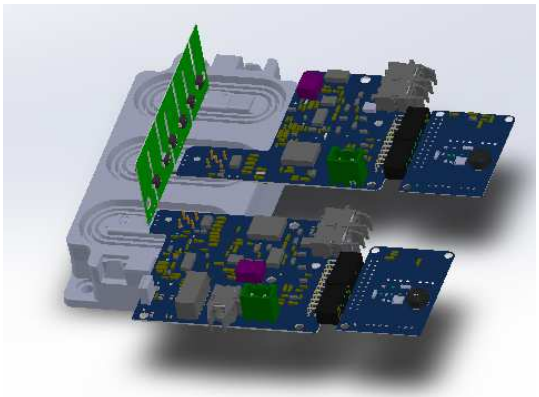


Fig. 3. Gate driver and desat diode board layout.

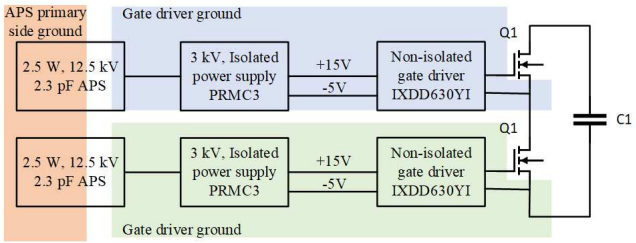


Fig. 4. Power architecture of gate driver.

III. Auxiliary Power Supply

The APS secondary side is connected to the submodule ground, thus the APS for the upper switch should sustain the full submodule dc link voltage in Fig. 4. For the topmost submodule connected to the 25 kV dc bus (with midpoint grounded), its APS has to have an insulation voltage of at least 12.5 kV. APS transformer encapsulated in material with a high breakdown strength of 20 kV/mm like silicone gel offers excellent

insulation capability. The material goes through a critical vacuum pressure potting process before curing to eliminate air bubbles and impurities trapped inside. Implementing high-voltage insulation material greatly reduces the clearance distance between the primary and secondary windings, thus shrinking the size of the APS. However, the PCBs exposed in the air still need to maintain clearance and creepage distance specified in UL 60950-1 standards.

Another important design aspect is to optimize the coupling capacitance between the primary side and secondary side of the APS to less than 5 pF, which suppresses the common mode noise current induced by the fast switching transient. The capacitance can be represented in (1), where C_{pc} is the capacitance between primary winding and the core, C_{sc} is capacitance between secondary winding and the core, and C_{ps} represents capacitance between primary and secondary windings [13]. The basic physics of capacitance leads to placing the windings away from the core, separating the windings as far as possible and minimizing the facing area in between.

$$C_{coupling} = \frac{C_{pc}C_{sc}}{C_{pc}+C_{sc}} + C_{ps} \quad (1)$$

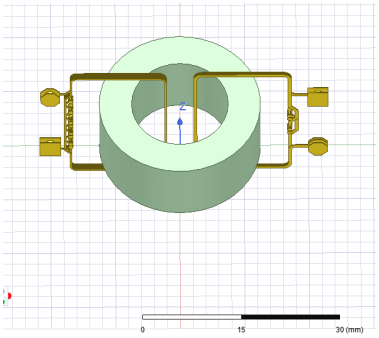
The core shape effect on coupling capacitance is investigated by comparing the toroidal core, U core, and E core. The core with relatively small size in each core shape category is selected. Larger cores may have smaller capacitance but they reduce APS power density. By controlling the winding parameters to be the same, such as trace width (0.5 mm and 0.25 mm), PCB winding turns (3:6), and winding distance (4 mm) from the core, the coupling capacitance of different core shapes is simulated in Ansys Maxwell 3D electrostatic analysis in Fig. 5. The voltage excitations are 10 kV on the secondary winding, 24 V on the primary winding and 0 V on the core respectively.

From Table II coupling capacitance is smaller in toroidal core than U core and E core. This can be explained by the fact that rectangular U core has a longer perimeter than toroidal core, thus larger capacitance. For E core, the distance between windings and core is constrained by the small winding area and its flat shape. Also, all four edges of winding are in parallel with the core, the overlapping area is larger than that of other core shapes, resulting in higher C_{pc} and C_{sc}. To optimize the coupling capacitance, toroidal core and U core are promising candidates.

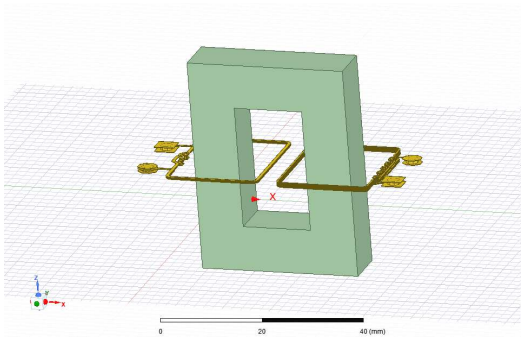
Unlike conventional transformers, this arrangement of winding and core inevitably leads to a transformer with large leakage inductance. The coupling coefficient is around 0.96. The tradeoff between achieving low coupling capacitance and sufficient magnetizing inductance is challenging as it depends on core size, material, core and winding distance, and geometry [14].

TABLE II. COUPLING CAPACITANCE COMPARISON

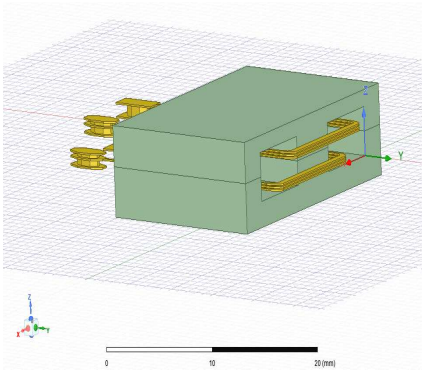
Core type	TX25/15/10	U33/22/9	E22/6/16
C_{pc} (pF)	0.93	1.18	1.48
C_{sc} (pF)	0.98	1.18	1.66
C_{ps} (pF)	0.17	0.17	0.56
$C_{coupling}$ (pF)	2.70	3.24	4.76



(a) TX25/15/10



(b) U33/22/9



(c) E22/6/16

Fig. 5. Different core shape coupling capacitance modeling.

IV. BUSBAR DESIGN

A. Loop Inductance

In this case, busbars connect the positive and negative terminals of submodule dc link with the power module. The 6.5 kV submodule dc link is made up of four 360 uF 2.5 kV capacitors (EPCOS B25690) in series. The capacitor terminals are connected by large polygons to conduct 57 A current between power modules effectively. The polygons on top layer and inner layer 1 are in parallel to reduce their respective inductances L_1, L_2 and L_3 by half in Fig. 6. When submodule is inserted in the phase leg, the current loop flows from DC+ to DC-. A vertical current loop is implemented in the PCB structure to reduce inductance by flux cancellation. Thus, polygons on inner layer 2 and bottom layer are designed to overlap top layer, which increases mutual inductance M_1 and M_2 that diminish the overall loop inductance in Fig. 7. The total busbar loop inductance simulated in Ansys Q3d is 154 nH with all the polygons connected together under the same net.

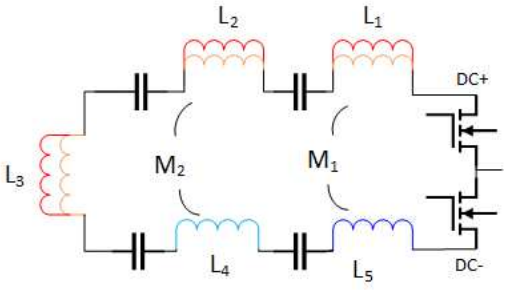
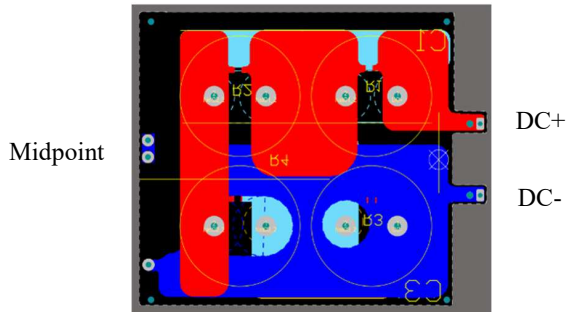
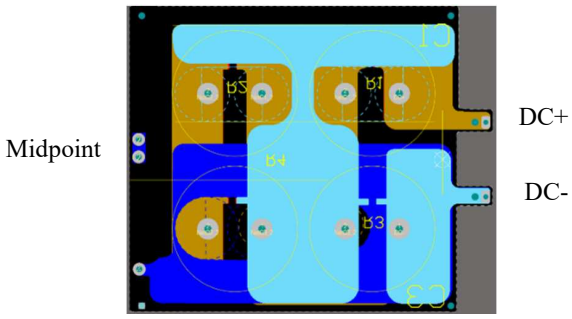


Fig. 6. PCB busbar inductance loop inductance.



(a) PCB busbar top and bottom layers.



(b) PCB busbar mid layers

Fig. 7. PCB busbar outer layers and mid layers.

The loop inductance measured by impedance analyzer is 180 nH. Its difference from the simulation (154 nH) is probably caused by via structures not incorporated in the conduction path of the Q3d simulation.

B. Copper Loss Estimation

The current that flows through capacitors is pulsating rather than continuous. FFT analysis is conducted for the capacitor current in Simulink simulation at full rating. The peak current at 60 Hz is 15 A. Also, there is a large second order 120 Hz circulating current at 6.7 A, which is typical in MMC applications. The switching frequency current at 10 kHz is merely 2.3 A. The copper loss of the busbar can be estimated by integrating the ohmic loss over the total volume in eddy current simulation with separate sinusoidal current excitation at 60 Hz, 15 A peak and 120 Hz, 6.7 A peak. With 1 oz copper, the loss is 1.07 W for 60 Hz and 0.21 W for 120 Hz. The loss is approximately reduced by half for 2 oz copper. The loss for 10 kHz current is 0.005 W in 2 oz copper PCB, which is negligible. This step is necessary, especially for high power busbar conducting large amount of current. Further analysis of heat distribution can be done to locate thermal weak point. In our case, the heat is very low for such large dimension (304 mm x 282 mm) busbar. It can dissipate heat effectively under natural convection, thus temperature simulation is not conducted here.

C. Insulation Design

The insulation design of PCB busbar can be divided into two parts, the horizontal insulation between polygons and terminals on the same layer of the PCB and vertical insulation between different layers of the PCB. The horizontal insulation design is based on IPC-2221B standard. For instance, exposed DC+ and DC- terminals have a creepage distance of 100 mm, longer than the required 50 mm distance for 10 kV isolation in the standard. The adjacent pads of the same capacitor have a 1.625 kV voltage difference, which are 30 mm apart.

The vertical insulation is determined by the voltage distribution, PCB material relative permittivity and PCB thickness. As the midpoint in one submodule is connected to the negative dc link of the adjacent submodule, there are two vias on the left side of the busbar for midpoint connection. It is placed 300 mm away from the dc link terminals without overlapping the polygons to avoid potential partial discharge of the PCB under high frequency switching voltage. As the busbar polygons withstand DC bus voltage instead of AC voltage, the voltage difference between the top layer and the bottom layer is stable. Thus, a conventional four-layer 90 mil PCB offers sufficient insulation. In the Fig. 8 Ansys Maxwell electrostatic simulation, the maximum electric field inside the PCB is located between the bottom layer and the second inner layer and is 9.8 kV/mm, well within 30 kV/mm dielectric strength of Isola 370HR material.

Four busbars are tested partial discharge (PD) free at 8.4 kV peak voltage, which supports operation at 6.5 kV. Partial discharge test detects accumulated electrons caused by the surface or air pocket within the insulation under a sinusoidal voltage excitation. The hipot test measures the leakage current

under DC voltage. From Fig. 9, leakage current is 0.12 μA at 10 kV, which also verifies the insulation effectiveness.

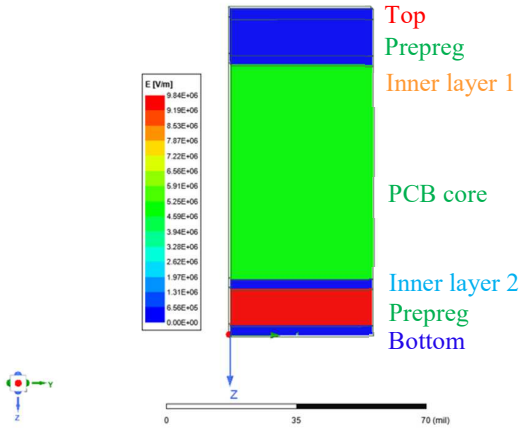


Fig. 8. Vertical electric field distribution between busbar layers.

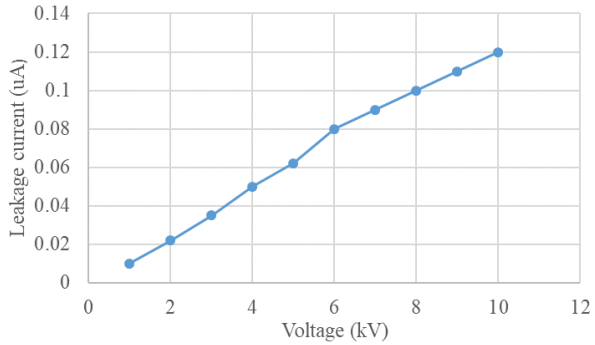


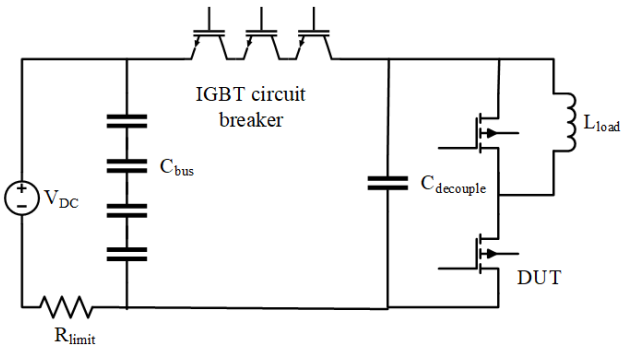
Fig. 9. Busbar hipot test with Phenix 4100-10.

V. Submodule Testing

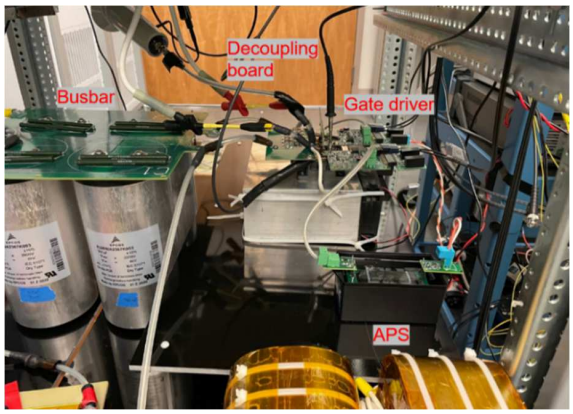
The DPT platform as shown in Fig. 10 (b) is built to test the submodule. The key components are described as follows. The dc link capacitor is 90 μF, the same as submodule capacitor. The dc link voltage can be adjusted from 0 to 7 kV. The load inductance is 5 mH. A circuit breaker with three Si IGBTs in series is connected into the main circuit to limit the maximum current in case a short circuit happens during testing.

Measurement probes with sufficient bandwidth and insulation are used. Drain source voltage is measured by high voltage differential probe DP20-10k (17.5 kVpk, 120 MHz). Device current is measured by PEM CWTMIni50HF Rogowski coil (50 MHz). Gate source voltage is measured by TPP1000 Tektronix voltage probe (1 GHz).

The DPT test is successful at 6.5 kV, 57 A as shown in Fig. 10. DPT at the same voltage with various currents are conducted from 25℃ to 125 ℃. From Fig. 11, turn on dv/dt increases with higher temperature and lower current. On the contrary, turn off dv/dt in Fig. 12 is not affected by temperature variance. Turn off dv/dt increases with larger current. Turn on dv/dt, which reaches over 100 V/ns at low current when temperature is above 50℃, is much higher than turn off dv/dt.



(a) DPT setup schematic.



(b) DPT hardware test platform.

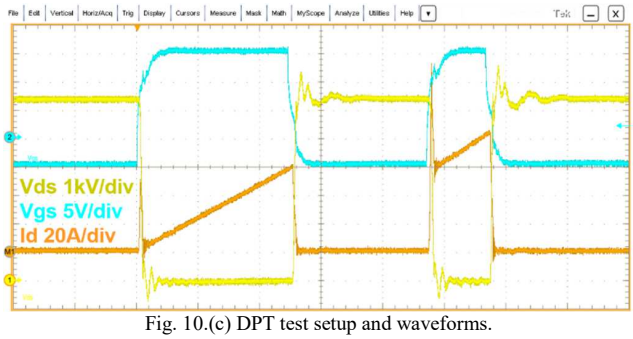


Fig. 10.(c) DPT test setup and waveforms.

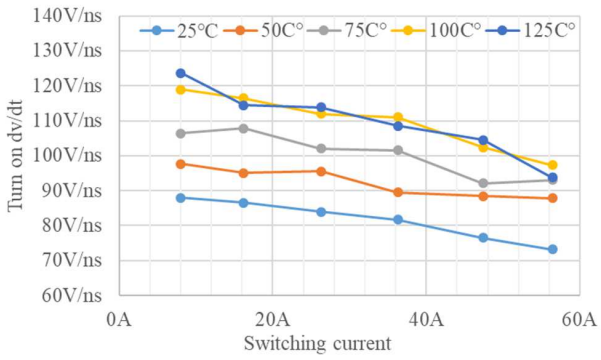


Fig. 11.Turn on dv/dt at different temperatures and current.

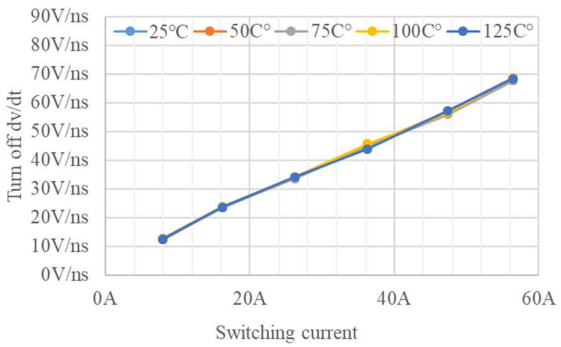


Fig. 12. Turn off dv/dt at different temperatures and current.

Continuous operation test run at 6.5 kV 57 A is shown in Fig. 13, which verifies the robustness of the submodule control and insulation design at high voltage.

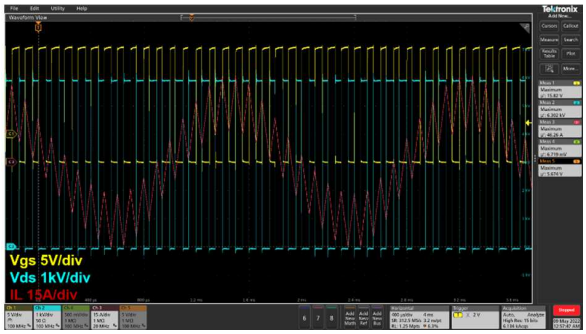


Fig. 13. Submodule continuous test run at 6.5 kV 57 A.

With the setup shown in Fig. 10, short circuit test of the submodule is conducted at 6 kV bus voltage as shown in Fig. 14. The desat protection triggered at less than 1us and soft turn-off the power module is achieved. With the help of the IGBT breaker mentioned earlier, the short circuit current is limited to within 300 A.

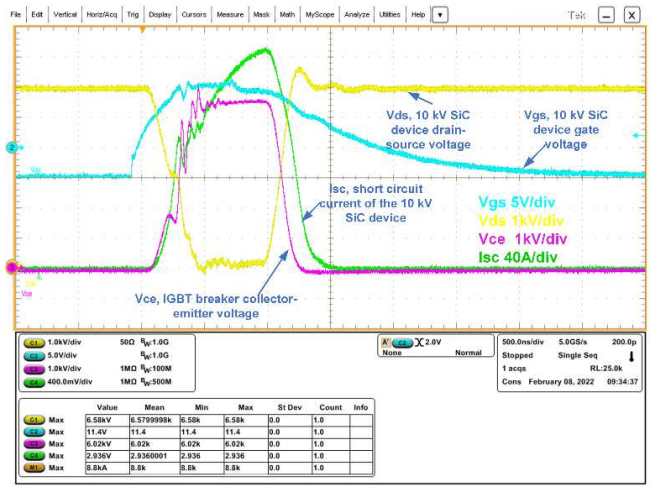


Fig. 14. Submodule short circuit test at 6 kV dc bus voltage.

VI. Conclusions and Future Work

This paper presents submodule development based on 10 kV SiC MOSFET XHV-9 module for medium voltage MMC in grid applications. The designed gate drive can support the fast switching of this 10 kV power module and dv/dt exceeding 100 v/ns is demonstrated in the DPT. Desat protection can effectively soft-turn-off the submodule within 1 us under 6 kV dc-link voltage while its noise immunity capability is verified through continuous power test at 6.5 kV voltage.

The APS is designed with a small capacitance of less than 3 pF. Coupling capacitance of a toroidal core, U core and E core are compared. The shape of the core affects the coupling capacitance due to the overlapping area between the core and the winding. The APS exhibits strong EMI immunity as the submodule is tested continuously at 6.5 kV, 57 A. Future work may investigate the gate driver and APS tolerance to radiated EMI when adjacent submodules are switching in a full converter setup.

Acknowledgment

This work was supported primarily by the Advanced Manufacturing Office (AMO), United States Department of Energy, under Award no. DE-EE0009134. The authors thank GE, EPB, ORNL, Southern Company, Wolfspeed, and Powerex for their contribution to the project. This work made use of the Engineering Research Center Shared Facilities supported by the Engineering Research Center Program of the National Science Foundation and DOE under NSF award number EEC-1041877 and the CURENT Industry Partnership Program.

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