

Automatic Layout Design and Implementation for Three Phase Voltage Source Converters

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Abstract—The converter level automatic layout is challenging because multiple types of components need to adhere to different placement rules. This paper proposes an implementation method for computers to automatically layout three three-phase voltage source converters. The proposed method utilizes a hierarchical tree to establish layout rules and prioritize components. The layout optimization process involves employing simulated annealing (SA) based heuristic optimization for the phase leg and applying specialized algorithms for different component groups. The layout of the phase leg is optimized for a minimum switching loop inductance. The layout of other components is solved as a floor plan problem or by directly following the design rules defined in the hierarchical tree. The whole converter layout can be visualized, and the switching node capacitance can be extracted. These parasitics enable more accurate switching performance evaluation for the design tool applications. Moreover, the proposed layout design can be easily extended to other types of converters.

Keywords—automatic layout, computer-aided design, converter layout optimization, switching loop optimization, heuristic optimization.

I. INTRODUCTION

Switching waveform calculation is a critical part of the design tool, which can determine the estimated overvoltage and switching loss, and influence the semiconductor devices selection and the thermal system design [1]. To perform the switching waveform calculation, the parasitic loop inductance and switching node capacitance are needed using the advanced switching models [2]-[3]. However, during the design stage, accurately obtaining parasitic inductance becomes challenging without the layout [4]. Thus, an automatic layout tool is significant in providing accurate parasitic values for the switching waveform calculation and converter design. Additionally, the visualization of the layout benefits the users' understanding of the design.

The automatic layout has become prevalent in very large-scale integration (VLSI) and power module designs. For the VLSI, the layout primarily involves standard cells that are relatively uniform in size, e.g., basic logic gates or small logic elements [5]-[6]. The power module layout is more complex due to the varied shapes of the components and insulation considerations [7]-[10]. The orientation needs to be considered for an optimized design. At the converter level, multiple types of components are involved in the layout design and the objective is not merely to place them as close as

possible. This complexity brings new challenges because different types of components need to adhere to different placement rules.

The reported automatic layout methods for the converter level remain quite limited. In [11], the sequence pair approach is extended into 3D to place components in a 3D structure. However, only the overall volume is optimized without considering the electrical performance impacted by the relationship between different components. Ref [12] optimizes the layout of a buck converter with only two surface-mounted components. However, the optimization is limited to adjusting the distance of the two components, making it difficult to extend to more complex topologies. In [4], the automatic placement of the two-level three-phase ac converter is implemented by simply placing all switches in a row. However, it lacks optimization, and the decoupling capacitors are not considered. Therefore, there remains a need for an automatic layout design method that can optimize the layout of the entire converter.

The main objective of this work is to propose an automatic layout design implementation method that enables the computer to optimize the converter level layout and provide the estimated parasitics for the design of a three-phase voltage source converter (VSC).

The remainder of this paper is organized as follows. Section II introduces how to formulate the layout problem and the proposed automatic layout design based on the hierarchical tree. The proposed simulated annealing based optimization approach for switching loop layout is discussed in Section III. Section IV introduces the proposed solution for the converter level layout. Section V concludes the paper.

II. FORMULATED PROBLEM AND PROPOSED AUTOMATIC LAYOUT DESIGN

A. Problem Formulation

The three-phase voltage source converter is commonly used in motor driver applications. Fig. 1 shows an example of the two-level voltage source converter topology. It normally consists of three phase legs, bus capacitors C_{bus} , a thermal management system, EMI filters, etc. The layout of the EMI filter part can be decoupled with other parts, which is not within the scope of this research [12]-[13].

The main challenge for the converter-level automatic layout is that different components need to adhere to distinct

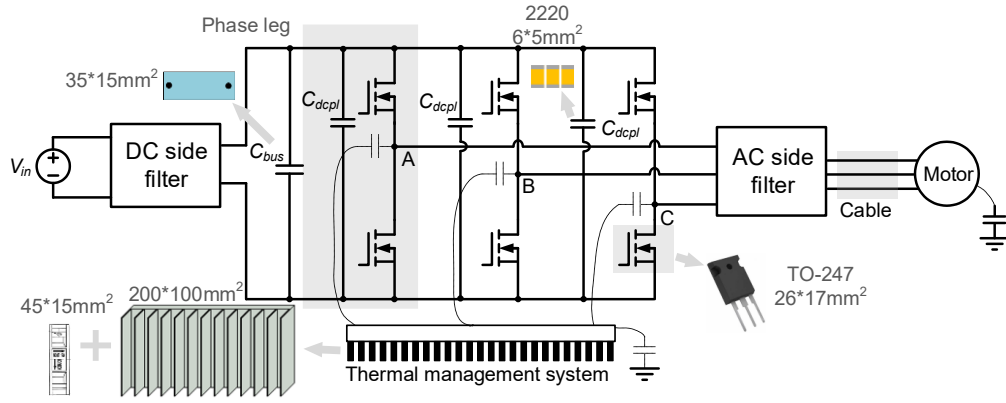


Fig. 1. Three-phase two-level voltage source converter in a DC-fed motor drive application.

placement rules. To formulate the problem, the main design rules are summarized below:

- 1) Switches and decoupling capacitors should be placed close to each other to minimize the commutation loop and switching loop inductance.
- 2) For improved consistency, different phases are preferred to have the same layout configuration.
- 3) Paralleled bus capacitors should be compactly placed together without introducing additional components among them.
- 4) The thermal management would be placed attached to the devices.
- 5) The insulation requirements for each component should be considered.

B. Proposed Automatic Layout Tool

To address this layout problem, the main idea is to categorize the components into different groups and apply specific algorithms based on the design rules. To facilitate this, a hierarchical tree is proposed to formulate the placement relationship for each component as shown in Fig. 2. The tree provides priorities and rules for different components.

At the lowest level of the tree, the layout of the phase leg (or switching cell), including the switches and the decoupling capacitors C_{dcpl} , is implemented first. This layout is critical to determine the switching loop inductance. It is implemented with the simulated annealing (SA) based heuristic optimization approach. It is then taken as an entirety to the higher levels in the tree. Three-phase switching cells are one level above the single switching cell with translational symmetry. The distance between the three switching cells is

determined by the insulation requirement. Then, bus capacitors are placed based on three-phase switching cell placement results, which can be taken as a rectangle packing problem. After that, the thermal management related components are placed. The three phases of the converter components are assumed to be put at the center of the heatsink. The fan is then placed based on the channel direction of the heatsink.

By employing the proposed hierarchical tree based layout optimization, the design rules mentioned in Section A can be satisfied during the design stage to benefit the speed of the automatic placer by reducing the trials of many unreasonable cases. Some assumptions of this placement algorithm include: 1) gate driver boards are independent boards placed on top of the devices; 2) the controller board is an independent board placed on top of the gate driver board.

C. Design Example Problem

A case study is given to demonstrate the proposed automatic layout design. The components in the VSC include 6 semiconductor devices, 9 decoupling capacitors, 5 bus capacitors, 1 heatsink, and 1 fan. The detailed package and/or size information are listed below and also labeled in Fig. 1:

- 1) Semiconductor devices: 6 with TO-247 package (length: 26mm and width: 17mm);
- 2) Decoupling capacitors: 9 in parallel with 2220 package (length: 26mm and width: 17mm);
- 3) Bus capacitors: 5 in parallel (length: 35mm and width: 15mm);
- 4) One heatsink (length: 200mm and width: 100mm);
- 5) One fan (length: 45mm and width: 15mm).

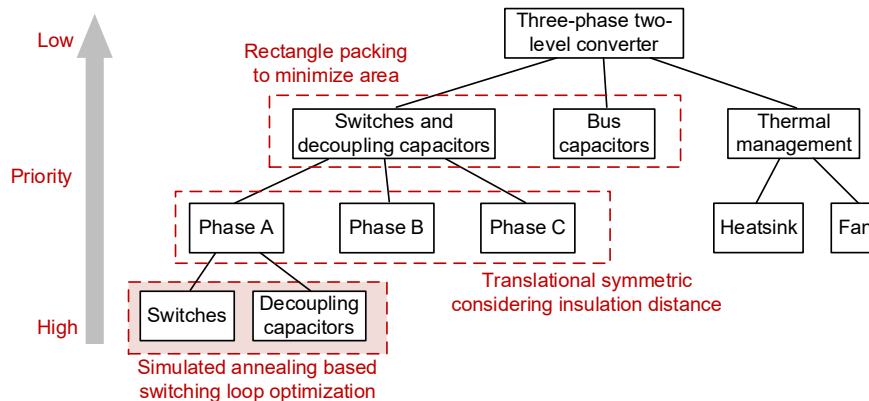


Fig. 2. Proposed hierarchical tree for three-phase two level converter layout.

These geometry information and dimensions of the components, together with the electrical net assigned to each pin of the components, are also the inputs needed for the automatic layout design algorithm.

III. OPTIMIZATION LAYOUT FOR SWITCHING CELLS

The switching cell layout is the most critical part. It is given the highest priority in the hierarchical tree for the layout design. The switching cell includes a half-bridge of semiconductor devices and decoupling capacitors as shown in Fig. 3. The parasitics include switching loop inductance L_{loop} and mid-point to heatsink capacitance C_{ac_out} . Both can influence the switching performance including the switching loss and voltage overshoot during switching. In the switching cell stage, the focus is to minimize L_{loop} . The optimization problem can be formalized as:

- 1) Design variables: component positions and orientations.
- 2) Design conditions: component geometry information, including the size and pin relative positions.
- 3) Design constraints: a) no overlap between each component; and b) the distance between each component needs to be greater than the insulation distance.

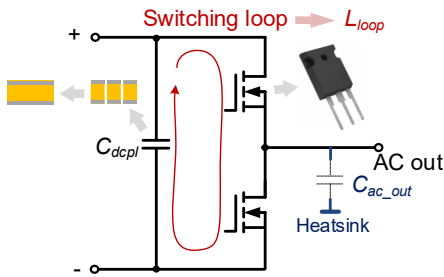


Fig. 3. Switching cell for layout optimization.

A. SA based Optimization for Switching Cell

To solve this optimization problem, the SA algorithm is used [15]. It is a global search optimization algorithm inspired by the annealing technique in metallurgy. The algorithm starts with an initial placement by assigning positions and orientations to each component. Random iterative improvement is then conducted with three possible modifications of the placement: 1) rotate a component; 2) move a component to another place; and 3) swap two components. Each time, only one modification is randomly picked to evaluate the performance after it. The probabilistic swap accept criterion is used to determine whether this modification is accepted as a new placement. The probability of accepting the new placement even when its performance is worse than the current best results is calculated as

$$P = e^{-\frac{\Delta L_{loop}}{T}} \quad (1)$$

where ΔL_{loop} is the change of the performance, which is the switching loop inductance in our case, and T is a constant to scale ΔL_{loop} for a reasonable acceptable rate.

This method simulates the annealing of the crystal with a computer program, which enables the opportunity to find the global optimal solution for complex and strong nonlinear problems. For example, in Fig. 4, if the optimization algorithm

is to only accept the iteration with better performance, it results in the local minimum 2 from the initial point 1 and cannot achieve the global minimum 3 eventually. However, with simulated annealing, the algorithm can go to peak first by accepting the worse performance and finally ends in the global minimum 3.

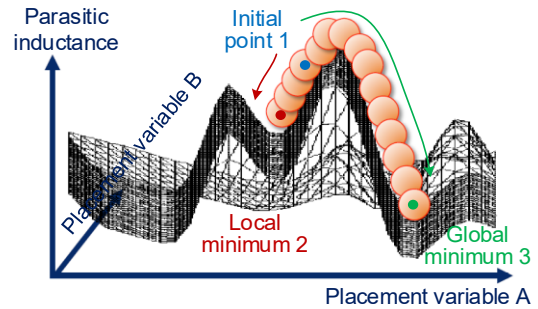


Fig. 4. Illustration of global optimization using simulated annealing algorithm.

B. B* Tree Representation

To implement those modifications of component placement by computer, encoding and decoding need to be applied. In this work, the B* tree is applied to represent the relative position among the components.

Every representation is unique for one placement. An example is shown in Fig. 5. The root node of the B* tree is on the bottom-left corner of the placement, e.g., D in Fig. 5. Left child means that the component is on the right of the parent component, e.g., E to D in Fig. 5. Right child means that the component is above the parent component, e.g., T to D in Fig. 5. The tree is then transferred to code to be processed with the machine language. The number of the code corresponds to the relationship in the tree as labeled in Fig. 5 (b) and (c).

The B* tree can be used to move and swap components. The rotation information is stored in each node. The information follows the element when the element moves from one node to another node.

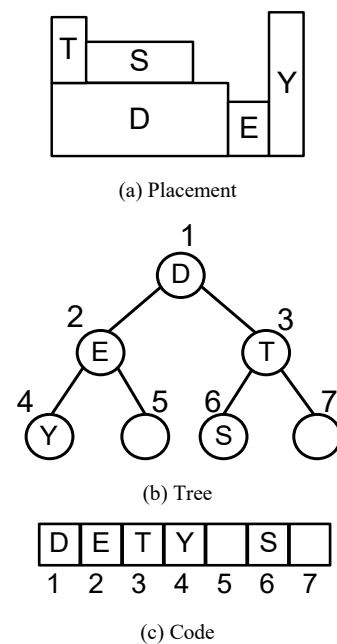


Fig. 5. A B* tree example.

Combined with the SA algorithm, the overall process is to first choose an initial B* tree and then perturb the B* tree to another B* tree to move or swap components or rotate one component randomly until a predefined “frozen” state is reached. Note that the 3 paralleled decoupling capacitors for each phase are placed close to each other in the real design. Thus, they are taken as an entirety as shown in Fig. 3 to reduce some unreasonable placement to simplify the optimization.

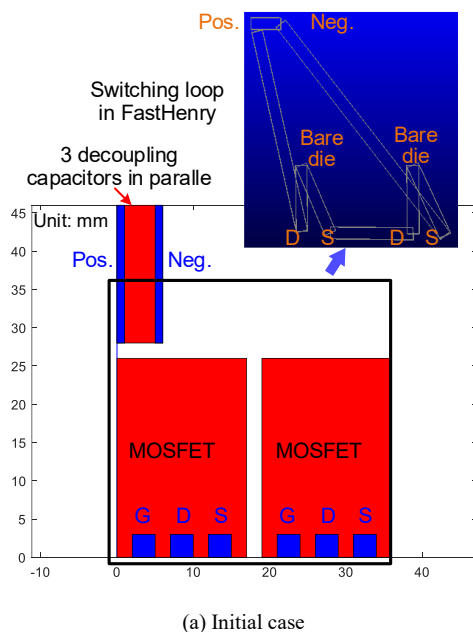
C. Routing and Parasitic Extraction

The parasitic loop inductance needs to be calculated to evaluate the performance of each layout design. The routing is simplified in the switching cell layout part by directly connecting each node. To avoid the overlap between different connections, each node is shifted 0.5 mm on z axis. The width of the trace for connection is 2 mm. Since the evaluation is implemented the same for all cases and the loop inductance is mainly determined by the loop area, this method is reasonable to pick the case with the minimum switching loop inductance.

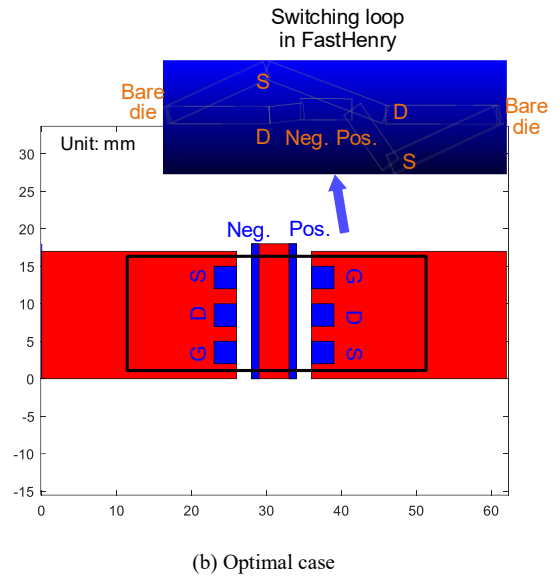
Parasitic inductance extraction is realized by an open-source fast field solver, FastHenry, based on the partial element equivalent circuit (PEEC) method [17]. The switching loop inductance is extracted. Since the routing and the placement of other components are not finalized, the switching node to grounding capacitance is still not determined and not extracted at this time. The subfigures in blue in Fig. 6 are the visualization of the FastHenry simulation with the connecting traces.

D. Design Example

Based on Part B Section II, the SA based algorithm is applied to optimize the placement of the switching cell. The cost function is the commutation loop inductance. PEEC based simulation is linked with the placement of the components to procure the simulated loop inductance. The initial case is randomly selected and represented by the B* tree. The placement is shown in Fig. 6 (a) with the switching loop. The loop inductance, in this case, is more than 50 nH. Fig. 6 (b) shows optimized placement and corresponding switching loop. In this optimized layout, the parasitic inductance has been reduced to 23 nH.



(a) Initial case



(b) Optimal case

Fig. 6. Placement and switching loop of initial and optimal cases.

Fig. 7 shows the SA optimization process. The optimization starts with the original layout and is optimized to 23 nH after 105 trials. Then the optimization stops at that minimized inductance.

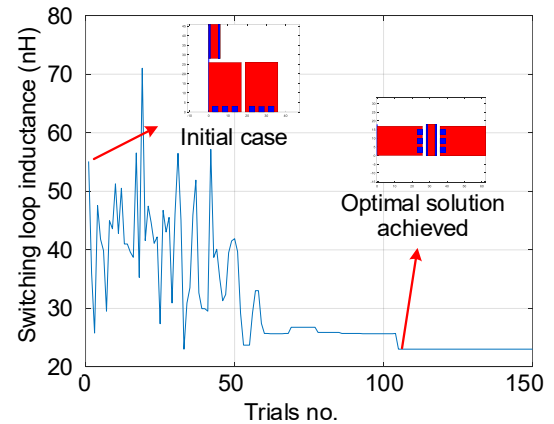


Fig. 7. SA optimization process.

IV. REMAINING LAYOUT OF THE ENTIRE CONVERTER

A. Placement of the Entire Converter

After the switching cell layout has been optimized, it is taken as an entirety to be placed together with other components in the converter. Compared to the placement of the switching part, the entire converter placement has less freedom owing to the design rules defined in Fig. 2. These constraints limit the possible solutions for the converter layout. As shown in Fig. 2, the phased leg is translational symmetric shifted to obtain the other 2 phase legs. The distance for the shift is based on the insulation distance between each phase. Then, the three-phase legs are placed with the bus capacitors, which can be taken as a floor planning or rectangle packing problem [18]. The goal for solving this problem is to achieve a minimum area with the design rules applied. An open-source tool ‘MiniZinc’ is used here to optimize the placement for the minimum area. A screenshot of part of the code to implement the converter level auto

placement is shown in Fig. 8. The tool can automatically solve the optimization problem by defining the design constraints, conditions, and goals.

```

26 %first constraint is about defined rotation
27 constraint forall(i in BLOCK)(shape[i,rot[i]] != {}):
28
29 %second constraint is for defined area
30 constraint forall(i in BLOCK)(forall(r in ROFF)
31 (r in shape[i,rot[i]] ->
32 (x[i] + d[r,1] + d[r,3] <= 1 /\
33 y[i] + d[r,2] + d[r,4] <= h)));
34
35 %third constraint is for no overlap
36 constraint forall(i,j in BLOCK where i < j)
37 (forall(r1,r2 in ROFF)
38 (r1 in shape[i,rot[i]] /\
39 r2 in shape[j,rot[j]] ->
40 (x[i] + d[r1,1] + d[r1,3] + delta <= x[j] + d[r2,1]
41 \
42 x[j] + d[r2,1] + d[r2,3] + delta <= x[i] + d[r1,1]
43 \
44 y[i] + d[r1,2] + d[r1,4] + delta <= y[j] + d[r2,2]
45 \
46 y[j] + d[r2,2] + d[r2,4] + delta <= y[i] + d[r1,2]
47 ));

```

Fig. 8. Code in MiniZinc for the entire converter placement.

For the thermal management related components, they are directly placed below the switching cell related components. The three-phase switching part components of the converter are assumed to be put at the center of the heatsink. The fan is then placed based on the channel direction of the heatsink.

B. Routing of the Entire Converter

Routing for the entire converter is simplified thanks to the power and grounding power plane. This is normally a good practice in real converters. With all these positive and negative networks connected, the only remaining nets are the mid-point of the three phases. Owing to the compact layout optimization of the switching cell part, they can be connected directly using the PCB trace without a complex routing algorithm.

For a converter with more complex nets needing connections. The breadth-first-search based maze algorithm with back-tracking commonly used for VLSI can be implemented [19]. The main challenge is that different trace widths need to be considered because wider copper trace is often used in power loop routing for higher current applications.

C. Visualization and Parasitic Extraction with PEEC Based Open Source Tools

After all placement and routing are finished, the whole converter can be automatically generated in FastHenry for visualization as a virtual prototype. Fig. 9 shows the final designed converter layout. The heatsink is placed below the converter to mount the semiconductor devices and the fan is placed vertically to the channel of the heatsink. They are not shown in the figure.

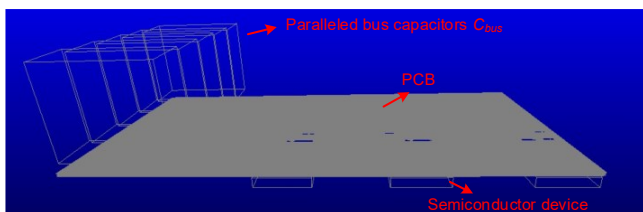


Fig. 9. Visualization in FastHenry.

The parasitic capacitance between the switching node to the ground (heatsink) is extracted with the geometry shown in Fig. 10. A similar open-source tool, FastCap2, based on the PEEC algorithm is utilized. To simplify the geometry and reduce the mesh complexity for the simulation, only the trace connecting the midpoint, semiconductor device, power planes, and the heatsink mounting surface are considered, which are the main contributors to parasitic capacitance. The extracted capacitance is 8 pF for each phase.

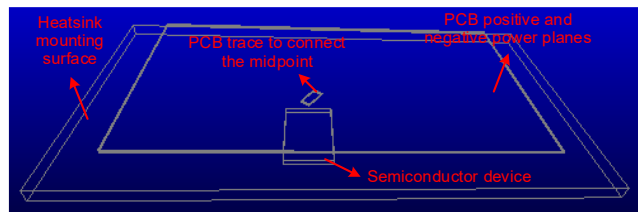


Fig. 10. Capacitance extraction in FastCap2.

V. CONCLUSIONS

A converter-level automatic layout design and implantation method is proposed in this paper. A hierarchical tree is proposed to decouple the layout of different types of components to determine the placement relationship between each component. The most critical part is the switching cell layout, which is optimized with the simulated annealing algorithm. The design example presents an optimized switching loop inductance of 23 nH. For other components, the desired rules for the placement are included in the hierarchical tree to avoid trying many unreasonable placement options. The placement is then formalized as a floor plan problem to minimize the layout area. The design example presents a switching node to ground capacitance of 8 pF. Compared to conventional layout optimization, this work enables the computer to automatically optimize the layout of the converter by formulating the layout problem, transferring the problem to machine language, and utilizing advanced optimization algorithms.

The extracted parasitic inductance and capacitance can be used for a more accurate switching waveform calculation to result in a more reasonable converter design. Moreover, the PCB or bus bar weight not commonly considered in the design stage can be accurately estimated using the proposed algorithm in the paper design. The visualization of the design is also given, which can help users understand the designed converter. Similar design methodology can be extended to other applications.

In future work, this automatic layout design and implementation method will be embedded in the design tool for more accurate and comprehensive converter designs.

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