Grid-tied PV Inverter With Oversized Power Module To Increase Its Low-voltage Ride Through (LVRT) Capabilities and VAR Support

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***Abstract*— This paper proposes a novel design for grid-tied 3-ph Photovoltaic (PV) inverter to improve its low-voltage ride through (LVRT) response while significantly increasing its volt-ampere reactive (VAR) support during voltage sags. The literature available on LVRT for PV inverters can be grouped in solutions that dissipate the excess energy and those that temporary stores this energy. This paper proposes a third solution; oversizing inverter hardware components to safely transferring all the energy excess back to while maintaining the semiconductor under the maximum temperature limits. The advantages of the proposed approach are: 1) Improved LVRT capabilities and stable dc-link voltage control at MPP during sags. 2) Increased VAR support during voltage sags. 3) Increased use of renewable energy as all active power is injected back to the grid during voltage sags. Finally, the proposed solution is more cost effective compared with solutions that incorporate energy storage because only a few inverter components are required to be oversized. This paper also presents a detailed power loss analysis, which determined that that oversizing the power semiconductors has minimal impact in the inverter losses while significatively reducing the diode and IGBT conduction losses during both normal operation and grid fault conditions.**

***Index Terms*—Low-voltage ride through (LVRT), VAR, PV**

I. INTRODUCTION

High penetration of distributed grid-tied PV inverters brings concerns about the voltage and frequency regulation. Short-duration voltage sags that last a few milliseconds can take PV inverters offline for a few minutes. As shown in [1], PV tripping during faults may create cascading effects in the transmission grid in areas where there is a high penetration of PV installations. Grid operators manage transients by static compensation techniques e. g., static synchronous compensator (STATCOM), which adopt large inductive/capacitive arrangement to provide reactive power injection to compensate for the voltage sag/swell. STATCOMs provide dynamic reactive power compensation, injecting or absorbing reactive power into the grid, helping to stabilize voltage levels and regulate power flow.

Through its integrated power electronics, Inverter-based resources (IBRS) such as PV and wind, can provide Volt-Ampere Reactive (VAR) support. These units are well suited for this purpose as they are highly controllable and can handle both inductive and capacitive reactive power. Grid codes recommend that grid-tied IBRs remain connected during low-voltage sags of different magnitudes while also requiring required to provide to provide reactive power support to help the grid recovery [3,6]. For example, IEEE 1547-2018 stipulates the reactive power support PV-inverters should inject during sags as well as the LVRT profiles the inverter must comply with [2].

Riding-through faults pose a challenge for PV inverters. PV inverter typically limit their ac output current to 1.0. p.u [4]. When voltage sags occur, this limited current restricts the power output of the inverter, consequently, an excess of energy at the dc-side is generated due to the operation at maximum power-point tracking (MPPT) during grid faults [6], [8], [9]. To tackle this problem several LVRT solutions for PV inverters have been proposed in the literature. These strategies can be grouped in solutions that dissipate the excess energy and those that use energy storage to temporary store this energy. Solutions that dissipate power include adding circuitry such as crowbar circuits [8], dynamic resistors, or DC-choppers, to dissipate excess power [9]. Active solutions have been proposed such as curtailing PV output current and disable the MPPT during the faults. Solutions to involve energy storage temporary can be achieved thought battery storage or super-capacitors. These methods avoid the unnecessary dissipation of energy by storing the excess energy during a fault and then release it back to the grid after the fault clears. For instance, authors in [7] propose a design to store energy excess into the battery during voltage sags, which allows keeping the MPPT in operation. The advantage of this method is that it can allow inverter ride through faults independent of the sag severity. Although this method maintains stability and operation at the MPPT, the method requires additional and expensive energy storage unit and associated power electronics. Furthermore, energy storage has a much shorter lifetime than the PV components, and additional routines are needed in its daily operation.

This paper proposes another option that has not been yet proposed in the literature, which consist of oversizing the inverter's power module to allow the PV inverter to inject the

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excess energy back to the grid during voltage sags. The advantages of the proposed method are: 1) Improved LVRT capabilities and stable dc-link voltage control with MPPT during sags. 2) increased ancillary support during voltage sags; 3) higher use of renewable energy the active power is injected back to the grid during voltage sags. Finally, the proposed solution is cost effective compared with solutions that incorporate energy storage because only a few inverter components are required to be oversized. Based on the PV inverter breakdown presented in [11], increasing the semiconductor current rating by three-fold would increase the cost of the PV inverter by ~8.7%. Although the cost of the inverter is increased, overrating the semiconductor brings additional benefits that help offset this additional cost. Besides the improvements in the LVRT response and additional ancillary service capabilities, electrothermal simulations shows that compared to a normally rated semiconductor, the total power losses of the overrated power module are significatively lower. These lower losses, combined, the better thermal impedance of the overrated module, translates into lower temperature of the junction during normal operation (1.0. p.u), which may reduce the thermal requirements of the inverter.

II. Effects of Voltage Sags on Commercial PV Inverters

Before introducing the proposed solution, this section discusses experimental results that shows the behavior of a commercial three-phase PV inverter during voltage sags of different magnitudes.

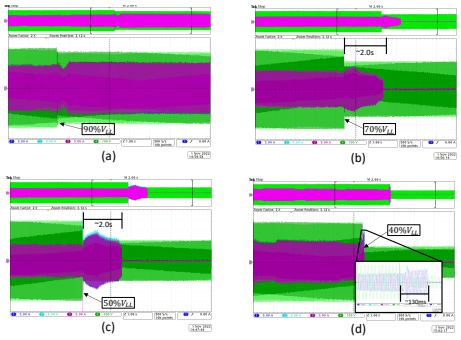

Fig. 1. Experimental results showing LVRT response of commercial PV inverter for a [90%, 70%, 50%, 40%] voltage sag, where 100% is equal to normal operation. Inverter operating at 20% of its rated capacity of 24kW.

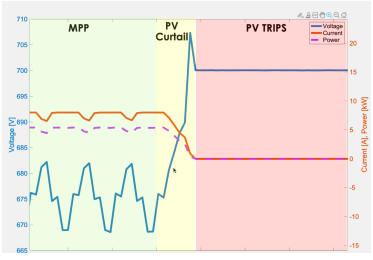

Fig. 2. Experimental results showing DC-link response during voltage sag obtained. The commercial inverter was initially operating at MPP, when voltage dip occurrs, the inverter increasing the dc-link voltage moving the PV curve close to VOC which curtail PV ouput.

The test setup consists of a 24 kW, 480 V three-phase PV inverter, connected on the dc-side to an NHR 9300 emulator, rated at 100 kW,1200 Vdc, and on the ac-side to an NHR 9410 grid simulator, rated at 100 kW and 480 V. The PV inverter was set to operate at 25% of its rated power capacity. Fig. 1 shows experimental results obtained from the 24 kW PV inverter subject to multiple voltage sags.

Fig. 1(a) shows that the inverter has continuous operation for a voltage sag of 90%, as it is specified by IEEE 1547. For a 70% voltage sag, the inverter trips two seconds after the fault was applied, similarly, for a 50% sag. Fig. 2 shows the dc-link voltage during a 50% voltage dip. To mitigate the energy excess in the dc-side this commercial inverter increased the dc voltage to curtails PV power. Finally, for a voltage sag lower than 50%, the inverter quickly disconnects after 7 cycles.

These results show that inverter current injection during fault is very limited and remains regulated close to the pre-fault. Secondly, the inverter quickly disconnects in few cycles for low grid voltages, such as the one caused by low impedance nearby grid faults. This lack of current injection during voltage sags introduces challenges in current-based distribution protection as well as limits the VAR support the inverter can provide.

III. Detailed Study of Effects of Voltage Sags on PV Inverters

Fig. 3 shows a simplified diagram to illustrate the energy excess created during voltage sag applied to a three-phase PV inverter. This simplified diagram assumes that that inverter max current is 1.0. (p.u.), that the inverter is sized at the same power rating as the PV array and that the system is lossless. In the figure, $\delta = 0$ means zero voltage at the point of common coupling (PCC).

Fig. 3(a) shows that during normal operating condition, the inverter output power is equal to the PV power at the maximum power point (MPP). Fig. 3(b) illustrates that when a voltage sag is applied, an energy excess is created the dc-side. This energy excess is generated because the inverter output is limited due to the inverter's reduced current capabilities and the sagging voltage. Because the PV inverter current is limited to 1.0. p.u., the inverter cannot inject all the power available in the dc side back to the grid. The only available path for the surplus current from the PV panels is the inverter's dc-link capacitor. Because the voltage in capacitor is the integral of the current, this excess current is integrated creating a voltage surge in the dc-link. Fig. 3(e) plots the power through the capacitor for different voltage dip magnitudes, notice that the power through the capacitors increase as the voltage sag deepens; δ gets closer to zero. Fig. 3(d) shows the dc-link voltage for different voltage sag magnitudes. Notice that as the voltage sag depends, the dc-link voltage moves towards the panel's open circuit voltage (VOC). Because the power output from PV panels follows the IV curve, the higher the voltage from the MPP, the lower the power as the voltage approaches the panel's VOC. Fig.

3(c), Fig 3(f-g) shows that after a transient created by the sag the inverter reaches a new equilibrium point. Here, the DC-link voltage corresponds the voltage in the I-V curve that balances the power between the ac and dc side.

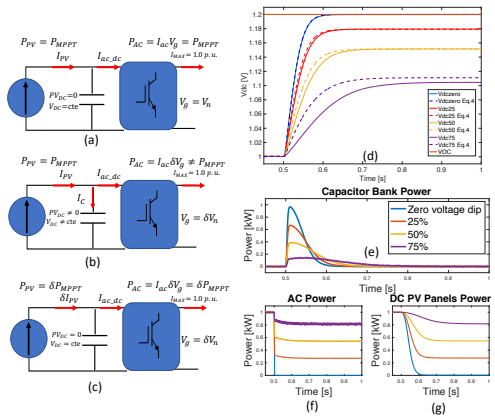

Fig. 3. PV inverter power during sags. (a) normal operation, (b) immediately during a voltage sag, (c) after reaching new power balance setpoint, (d) analytical estimation (E.q. 5) and simulated dc-voltage for different voltage dip magnitudes, (e) capacitor bank power, (f) ac power, (g) PV power.

A. Modelling PV inverter During Voltage Sags

This section presents an analytical solution to determine the dc-link voltage surge during sags. Fig.3(d) showed that the dc-link voltage depends on the magnitude of the voltage sag. To calculate the dc link voltage, it must be determined the excess current that flows through the capacitor during a voltage sag Applying Kirchhoff's Current Law (KCL) to the dc-link circuit,

$$I_C = I_{PV} - I_{ac\_dc} \tag{1}$$

where I_C is the current through the DC-link capacitor, I_{PV} is the current from the PV array, and I_{ac_dc} the inverter side dc current. The maximum rms ac current I_{ac_max} of the inverter can be calculated by (2), where V_{phn} is nominal ac phase voltage and P_{MPPT} the maximum power point of the PV array.

$$I_{ac\_\max\ \_} = {P_{MPPT}}/{3V_{phn}} = {P_{MPPT}}/{3\delta V_{phn}} \tag{2}$$

Based on this maximum current allowed by the inverter, the maximum current that can go through the dc side can be calculated using (3).

$$I_{ac\_dc} = \delta \frac{I_{ac\_\max} V_{phn}}{V_{dc}} \tag{3}$$

where $V_{dc}$is the dc-link voltage. As mentioned, during voltage sags, the PV inverter current is regulated to $I_{ac\_\max} \sim 1.0$ p.u. The current available from the PV array (4) is used to determine I_{PV} [12],

$$I_{PV} = \left(I - I_0\left[exp\left(\frac{V + R_s I}{V_t a}\right) - 1\right] - \frac{V + R_s I}{R_p}\right) \tag{4}$$

where I is the current generated by the incident light, I_o is the saturation current of the array, $V = N_s kT\ /q$ is the thermal voltage of the array with N_s cells connected in series. If the array is composed of N_p parallel connections of cells, the photovoltaic and saturation currents may be expressed as: $I = I_{cell} N_p\ I_o = I_o N_p$. R_s is the equivalent series resistance of the array, and $R_p$is the equivalent parallel resistance.

Finally, the dc-link capacitor voltage can be obtained by combining (2), (3), and (4). Notice that this equation shows a dependency: dc-link voltage is needed to calculate the current from the panels, and vice versa. In simulations this dependency can be implemented with a feedback loop.

$$V_{DC} = \frac{1}{C}\int\left(\left(I_{PV} - I_0\left[exp\left(\frac{V + R_s I}{V_t a}\right) - 1\right] - \frac{V + R_s I}{R_p}\right) - I_{ac\_dc}\delta\right) dt \tag{5}$$

Fig. 3(d) shows the validation of (5) by comparing it with the full model of the PV inverter simulated in Matlab Simulink, where a good fit was obtained.

IV. Proposed Inverter Design to Enhance Grid Support during Voltage Sags

This section presents the proposed solution to increase the LVRT capabilities of PV inverters, which consist of oversizing the current rating of the (IGBTs and freewheeling diodes) to inject the available PV energy from the dc-side to the ac-side during the voltage sags. This paper follows a similar methodology as the one introduced by the authors of this paper in [10]. Through experimental results, this previous work showed that a Voltage Source Converter (VSC) can increase it short-circuit current contribution by three-fold through oversizing the current rating of the power module. Important conclusions can be drawn from this previous work: 1) Normally rated module can inject twice its rated current, however, the temperature swing is very high, which can damage the semiconductor. 2) Overrated modules allow increasing the short-circuit current without degrading the normal operation. 3) No need to overrate inductive filter, but at high currents the inductor's core saturates, which must be addressed in the control.

V. Power Losses in Three-Level Inverter

This section develops an electrothermal model to estimate the temperature response of the power modules during voltage sags. In an inverter, the power losses can be divided into conduction and switching losses of the IGBTs and their associated anti-parallel diodes. For sinusoidal PWM (SPWM), the power losses for the IGBT and diode can be written as [13,14]:

$$P_{IGBTCond} = V_{TO} I\left(\frac{1}{2\pi} + \frac{m_a \cos(\phi)}{8}\right) + R_{CE} I^2\left(\frac{1}{8} + \frac{m_a \cos(\phi)}{3\pi}\right) \tag{6}$$

$$P_{DiodeCond} = V_{FO} I\left(\frac{1}{2\pi} - \frac{m_a \cos(\phi)}{8}\right) + R_{AK} I^2\left(\frac{1}{8} - \frac{m_a \cos(\phi)}{3\pi}\right) \tag{7}$$

$$P_{SW} = \frac{(E_{on\_peak} + E_{off\_peak}) f_{sw}}{\pi} \tag{8}$$

where the IGBT on-state resistance $R_{CE} = \Delta V_{CE}/\Delta I_C$ and diode on-state resistance $R_{AK} = \Delta V_{FM}/\Delta I_{FM}$. V_{CE} is the IGBT collector emitter voltage, I_C collector current, and V_{FM} is the diode forward voltage and I_{FM}diode forward current. ϕ is the phase angle between the inverter's output voltage and current, m_a is the pulse width modulation (PWM) amplitude modulation index. E_{on_peak} and E_{off_peak} are the switching turn on and turn off energies.

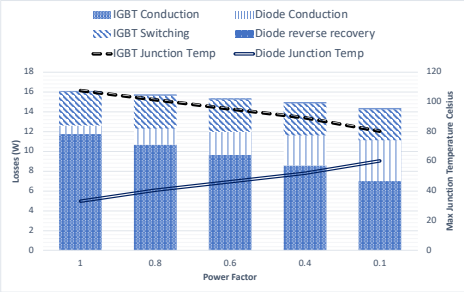

Fig. 4. Effects of power factor on power losses of diode and IGBT Maximum temperature of diode and IGBT for different power factors. $V_{DC} = 400V$, modulation index=1, $Tamb = 25$ ℃.

As shown, the conduction losses (6) and (7) depend on the power factor $\cos(\phi)$. This is graphically shown in shown in Fig. 4, where power losses shift from the IGBT to the diode as the power factor decreases. The diodes in a power module have worse thermal characteristics that the IGBT (higher thermal impedance), which can limit the amount of reactive power the module can provide. Because this work proposes increasing VAR support of the PV inverter, it is important considering the effect of the power factor for properly sizing the freewheeling diode [16].

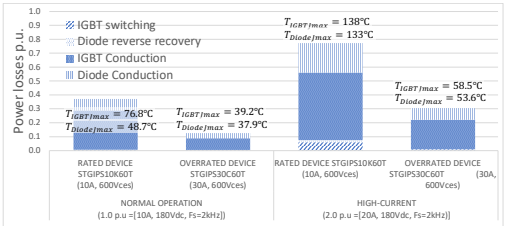

Fig. 5. Power loses comparison. Rated vs. overrated device [15].

Fig. 5 shows that oversizing the semiconductor reduces both the power losses and junction temperature during both normal operation (1.0 p.u) and high current (2.0 p.u) conditions (voltage sags). During normal operation the overrated device improves the efficiency of the inverter and may reduce the cooling requirements of the inverter. The overrated semiconductor also allows injecting the additional active power back to the grid required to maintain the energy balance during voltage dips while allowing the inverter to provide additional reactive power to the grid for grid support.

VI. Simulation Results:

Fig. 6 shows simulation results that show the feasibility of increasing the current output of an inverter to ride through voltage sags. For this simulation, a voltage sag of $\delta = 0.5$ (50%) was applied at $t = 0.2\ s$, the irradiance was set to $1000\ W/m^2$ and the power rating of the inverter is 3 kW. The voltage sag magnitude was set to comply with IEEE 1547-2018 requirements. Fig. 6(a-b) presents the results using a normally rated semiconductor (1.0 p.u. = 10A), and Fig. 6(b-c) shows the results with a power module with overrated current rating (3.0 p.u. =30A).

A. LVRT with VAR support: Normally Rated Power Module

Fig 6(a) shows the result when the inverter current is to 1.0 p.u (typical for PV inverters) and Fig. 6(b) shows the results when the maximum current is increased to 2.0 p.u. Both results use a normally rated semiconductor. As shown in Fig. 6(a-[IV]) and Fig 6(a-[I]), limiting the inverter current to 1.0 p.u. causes an energy excess in the dc-side during the sag. This excess power flows through the capacitor bank increasing the dc-link voltage. During this test the MPPT algorithm remained active, and no countermeasures were implemented.

Fig. 6(b) shows the results when the inverter output is increased to 2.0 p.u. The inverter was also programmed to provide a Q=1.0. p.u. for VAR support during the voltage sag. As shown, increasing the current capability allows the inverter to inject all the current back to the grid, maintaining inverter power balance, and the dc-link voltage constant with the PV panel at its MPP. However, increasing the current output and the reactive power support increases the total power losses for both the IGBT and diode, see Fig 6(b-VI) and Eqs. (6-7). The increase in power loss causes the junction temperature of the diode and IGBT to rise rapidly, eventually reaching the maximum temperature of 150°C specified by the manufacturer [15]. This information is visually represented in Fig. 6 (b-V). These results agree with experimental results previously presented by the authors in [10], which showed that a power module rated at 1.0. p.u can inject twice its rated current, however, the junction temperature of the IGBT and diode rapidly increases and could exceed the thermal limits of the device. For this reason, overrating the module it is a must to prevent permanent damage on the semiconductor during high current operation.

B. Overrated Power Module

Fig. 6(c-d) shows electrothermal simulation results for the inverter with an overrated power module. The module was overrated to three times the nominal current (30 A), the same as in [10], to allow it to ride through deeper grid faults to comply with more stringent grid codes. Fig. 6(c) shows the results for the inverter with overrated power module providng Q=1.0. p.u, and Fig. 6(d) providing Q=3.0. p.u. for increased VAR support. As shown, the overrated module allow the inverter to remain at a lower temperature range during the votlage sag, where the inverter injects the excess power back to the grid. The additional current capabilites of the overrated power module allow the inverter to inject higher reactive power during the voltage while maintaining the dc-lik at the MPP. Compared to the normally rated power module, the overrated power module present lower losses and lower temperature during normal operation, pre fault values. After the voltage sag is applied, the overrated power module has lower losses for the same reactive power support (compare Fig. 6(b) and Fig. 6(c)). As expected, to increased reactive support (Q=3.0 p.u.) the overrated power module increased its power losses, but the junction temperature remains low, which validates this approach for increased ancillary service support. Table I shows a summary of the results presented in Fig. 6.

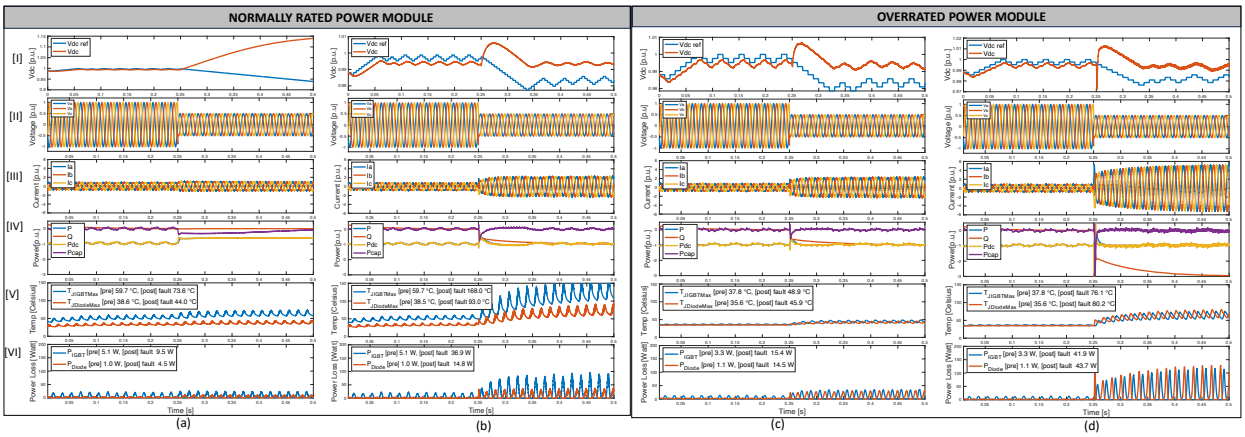

Fig. 6. (a) Normally rated power module, $Isat = 1.0.p.u$, no countermeasures. (b) Normally rated power module, $Isat = 2.0.p.u, Q = 1.0\ p.u.$ (c) Overrated power module, $Isat = 2.0.p.u, Q = 1.0\ p.u.$ (d) Overrated power module, $Isat = 2.0.p.u, Q = 3.0\ p.u.$ (I) dc-link capacitor voltage (II), grid voltage (III), inverter output current (p.u.), (IV) power flow for the ac-side, dc-side and dc-link capacitors, (V) thermal response of the IGBT and

TABLE I: Results Summary

	Normally Rated Power Module		Overrated Power Module	
Q[p.u.]	Q= 0.0	Q= 1.0	Q= 1.0	Q= 3.0
I_{satVdc} [p.u.]	1.0	2.0	2.0	2.0
PT_{IGBT} [pre, post]	[5.1, 9.5] [W]	[5.1, 36.9] [W]	[3.3, 15.4] [W]	[3.3, 41.9] [W]
PT_{Diode} [pre, post]	[1, 4.5] [W]	[1, 14.8] [W]	[1.1, 14.5] [W]	[1.1, 43.7] [W]
Tj_{IGBT} [pre, post]	[59.7, 73.6] [°C]	[59.7, 168] [°C]	[37.8, 48.9] [°C]	[37.8, 76.1] [°C]
Tj_{Diode} [pre, post]	[38.6, 44.0] [°C]	[38.6, 93] [°C]	[36.5, 45] [°C]	[36.5, 80.2] [°C]

VII. CONCLUSIONS

This paper proposed hardware modifications for a three-phase grid-tied PV inverter to ride through faults while increasing its reactive power support during voltage sags. The proposed design oversized the power module current rating to maintain the dc-link voltage at the MPP and to increase the reactive power support during grid faults. The advantages of the proposed method are: 1) enhanced ancillary support during voltage sags; 2) sag-depth independent LVRT and stable dc-link voltage control with MPPT during sags. Additionally, it was shown that devices with higher current capability have better thermal characteristics and lower losses than devices rated at lower currents. This improves the efficiency of the inverter and may reduce the cooling requirements of the inverter during normal operation.

REFERENCES

[1] Y. Yang, P. Enjeti, F. Blaabjerg et al., "Wide-scale adoption of photovoltaic energy: grid code modifications are explored in the distribution grid," IEEE Industry Applications Magazine, vol. 21, no. 5, pp. 21-31, Sept. 2015.

[2] "IEEE Standard for Interconnection and Interoperability of Distributed Energy Resources with Associated Electric Power Systems Interfaces," in IEEE Std 1547-2018, 6 April 2018.

[3] A. Hooshyar and R. Iravani, "Microgrid Protection," in *Proceedings of the IEEE*, vol. 105, no. 7, pp. 1332-1353, July 2017.

[4] S. Gonzalez, N. Gurule, M. J. Reno and J. Johnson, "Fault Current Experimental Results of Photovoltaic Inverters Operating with Grid-Support Functionality," 2018 IEEE 7th World Conference on Photovoltaic Energy Conversion (WCPEC), Waikoloa Village, HI, 2018, pp. 1406-1411.

[5] M. Mirhosseini, J. Pou, and V. G. Agelidis, "Single- and two-stage inverter-based grid-connected photovoltaic power plants with ride-through capability under grid faults," *IEEE Transactions on Sustainable Energy*, vol. 6, no. 3, pp. 1150-1159, Jul. 2015.

[6] M. Easley, S. Jain, M. B. Shadmand et al., "Computationally efficient distributed predictive controller for cascaded multilevel impedance source inverter with LVRT capability," *IEEE Access*, vol. 7, pp. 35731- 35742, Jul. 2019.

[7] M. Talha, S. R. S. Raihan and N. A. Rahim, "A Grid-tied PV Inverter with Sag-severity-independent Low-voltage Ride Through, Reactive Power Support, and Islanding Protection," in *Journal of Modern Power Systems and Clean Energy*, vol. 9, no. 6, pp. 1300-1311, November 2021.

[8] C. T. Lee, C. W. Hsu, P. T. Cheng, "A low-voltage ride-through technique for grid-connected converters of distributed energy resources," *IEEE Trans. Ind. Appl.*, 2011, vol. 47, no. 4, pp. 1821–1832.

[9] N. H. Saad, A. A. El-Sattar, A.E.-A. M. Mansour, "Improved particle swarm optimization for photovoltaic system connected to the grid with low voltage ride through capability," *Renew. Energy*, 2016, 85, pp. 181–194.

[10] M. Ferrari and L. M. Tolbert, "Inverter Design with High Short-Circuit Fault Current Contribution to Enable Legacy Overcurrent Protection for Islanded Microgrids," *2022 IEEE Power & Energy Society General Meeting (PESGM)*, 2022, pp. 1-5.

[11] PV inverter teardown identifies price-reduction opps. https://www.renewableenergyworld.com/storage/grid-scale/pv-inverter-teardown-identifies-price-reduction-opps/#gref. Online. Accessed 06/30/2023.

[12] M. G. Villalva, J. R. Gazoli and E. R. Filho, "Modeling and circuit-based simulation of photovoltaic arrays," *2009 Brazilian Power Electronics Conference*, 2009, pp. 1244-1254.

[13] 3-Phase Motor Control Demonstration Board featuring IGBT intelligent. Available at: https://www.st.com/resource/

[14] Bechtold, J. G. Korvink, E. B. Rudnyi, *Fast Simulation of Electro-Thermal MEMS: Efficient Dynamic Compact Models*, Springer, New York, 2007.

[15] ST-power studio 1.2. Available at https://www.st.com/en/embedded-software/stsw-powerstudio.html

[16] Y. Liu, L. M. Tolbert, P. Kritprajun, J. Dong, L. Zhu, J. Hambrick, K. P. Schneider, K. Prabakar, "Aging Effect Analysis of PV Inverter