

# PCB Rogowski Coil With DC Sensing for Double Pulse Test Applications

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**Abstract**—Accurately measuring the switching current behavior of wide bandgap devices requires a current sensor with a wide bandwidth covering dc to high frequency ranges. However, traditional Rogowski coils (RCs) for current sensing either lack the dc measurement capability or the inclusion of dc sensor largely increases the insertion inductance. This article presents a concept of combining a shielded RC with a dc sensor to improve the dc measurement capability without interfering with the power loop area of a double pulse test (DPT) circuit. The RC and dc sensor are positioned at different locations to capture the high-frequency and low-frequency components, respectively. An analog circuit combines the output of both sensors to recreate the signal. Frequency domain analysis of the prototype confirms the improved dc measurement of the probe. This article also presents the results of a DPT of a half-bridge SiC power module to demonstrate the enhanced dc measurement of the shielded RC, without any parasitic interference in the power loop area.

**Index Terms**—Bandwidth, dc measurement, double pulse test, hall sensor, power loop inductance, Rogowski coil, shielded.

## I. INTRODUCTION

THE emergence of wide bandgap (WBG) devices has led to higher requirements for current sensors' high-frequency bandwidth and size due to their faster switching transients and sensitivity to parasitics [1]. The high-frequency bandwidth requirement of a current sensor in WBG power electronic circuits depends on the transition times ( $t_r/t_f$ ) and the oscillation frequency of the current waveform [2].

$$F_{\text{edge}} = \frac{0.35}{t_r/t_f} \quad (1)$$

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where  $t_r$  and  $t_f$  corresponds to rising edge and falling edge of a signal waveform, respectively. To accurately capture the current waveform without distortion, the bandwidth requirement of the current sensor should have some margin [4]. Providing a margin ensures that the sensors' bandwidth is greater than the calculated  $F_{\text{edge}}$  value, allowing for accurate capture of the full frequency range of the signal. Moreover, the parasitic components in power electronic circuits form  $LC$  circuits that exhibit oscillatory behavior during the transition of the switching devices [3]. The maximum ringing frequency ( $F_{\text{ringing}}$ ) is determined by the power loop inductance ( $L_{\text{loop}}$ ), and the parasitic capacitance of the switching devices ( $C_{\text{oss}}$ ) [5]. The packaging technique for wide bandgap devices has recently focused on reducing power loop inductances [6], [7], but this leads to a higher ringing frequency which poses a higher requirement on the current sensor's bandwidth to cover the maximum ringing frequency. Another key parameter is the size of the current sensor, which may increase the power loop inductance in the system and lead to larger voltage overshoot and switching losses [8]. Therefore, the size of the current sensor must be minimized to reduce the insertion inductance and ensure that the current sensor does not significantly increase the power loop inductance of the system.

A double pulse test (DPT) circuit is a widely used method in power electronics to evaluate the dynamic switching characteristics of power devices [9], [10]. During the DPT, the commutation current waveform generated in the circuit is similar to a pulsed current source. It consists of steep  $di/dt$ , high-frequency ripples, and dc components. To accurately measure the commutation current waveform, it is essential to use a current sensor with a wide frequency range that includes both high and low frequency. The lack of dc measurement of a current sensor results in misalignment of the current waveform or creates a dc offset [11], [12], as illustrated in Fig 1. Fig. 1(b) shows that the larger pulse time or rising time ( $t_r$ ) requires enhanced dc or low-frequency measurement capability. To address this issue, this article proposes a method to improve the low-frequency bandwidth of a shielded PCB RC for the DPT application of WBG devices. The DPT circuit of SiC device is used as an example setup to demonstrate the proposed method.

Various techniques have been proposed to develop wide bandwidth (low frequency–high frequency) current sensors following the “HOKA” principle [11], [12], [13], [14]. The principle involves combining two different sensors to recreate the commutation current. One sensor provides a voltage ( $V_{\text{dc}}$ ) proportional

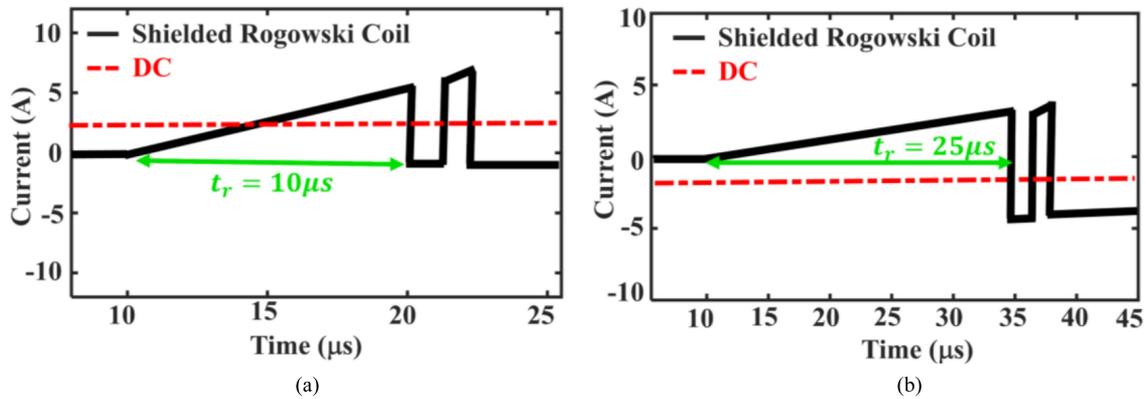


Fig. 1. (a) No misalignment from the real dc value for a rising time of  $t_r = 10 \mu\text{s}$ , and (b) misaligned current waveform for a larger pulse width or rising time of  $t_r = 25 \mu\text{s}$ .

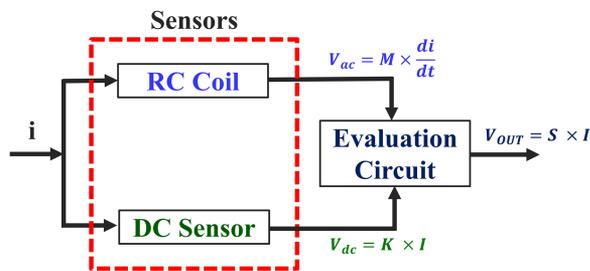


Fig. 2. Block diagram of “HOKA” principle. The  $M$ ,  $K$ , and  $S$  represents the mutual inductance of Rogowski coil, sensitivity of the DC sensor, and the sensitivity of the entire probe system, respectively.

to the current ( $i$ ), while the other sensor outputs a voltage ( $V_{ac}$ ) that is the time derivative of the current ( $di/dt$ ). Both outputs are processed through an evaluation circuit to reconstruct the commutation current ( $i$ ). The block diagram of the “HOKA” principle is illustrated in Fig. 2. To improve the dc measurement bandwidth, a current transformer (CT) and a hall element sensor have been merged [12], [15], [16]. However, the challenge arises in balancing the size of the air-gap of the CT and the hall element since the hall sensor is placed in the air-gap region of the CT. Another technique involves combining a Rogowski coil (RC) and multiple tunnel magneto-resistance (TMR) sensors, where the TMR sensors are mounted on the top surface of the RC. [17]. However, a coaxial housing is used to hold the entire probe which limits the benefit of minimizing stray inductance in the current path [18].

The main contribution of this article is that to address the abovementioned issues, an alternative method is proposed by combining a shielded RC with a dc sensor to enhance the dc measurement capability but without introducing any extra parasitic inductance in the power loop region of a DPT circuit. This is achieved by putting the dc sensor at a different location than the RC that is outside the power loop. The design principles of the dc integration and the optimal location of the two sensors in a DPT circuit are explained in Section II. Then, the frequency and the time domain experimental response of the current sensor are demonstrated in Section III. The experimental results verify the improved dc measurement of the RC in a DPT application with the dc offset issue solved.

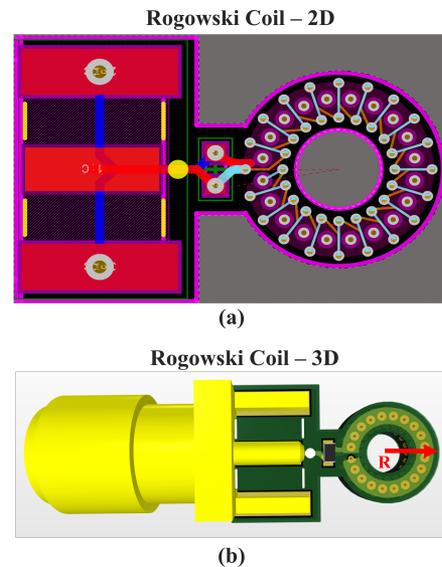


Fig. 3. PCB based Rogowski Coil in (a) two-dimensional, and (b) three-dimensional view.

## II. DESIGN PRINCIPLES OF DC INTEGRATION

Before delving into the principles and design of dc integration, this section provides a brief overview of the design and bandwidth of the self-integrating PCB RC. The structure of the PCB-based RC developed in [19] and [20] is shown in Fig. 3. The main advantage of this RC is the self-integration property, where the coil itself possesses integration capabilities within a specific frequency range, eliminating the need for an external integrator circuit in this frequency range. The PCB based RC has coil windings and the copper shielding layers. These shielding layers completely cover the coil windings, providing a single return path mechanism for the winding-to-shielding layer connection. The coil design results in passive integration at higher frequencies, primarily due to the parasitic capacitance ( $C_g$ ) between the shielding layers and the coil winding [21], [22]. This passive integration extends the high-frequency bandwidth of the coil without presenting additional requirement on the integrators. The linear or self-integrating bandwidth of the coil

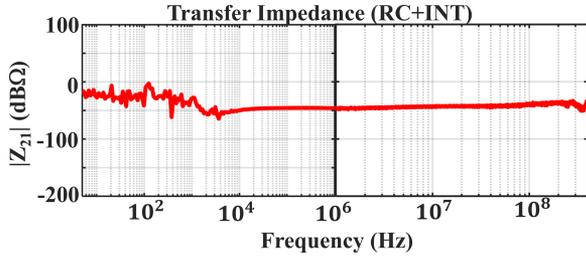


Fig. 4. Transfer impedance ( $Z_{21}$ ) of the Rogowski coil (RC) and integrator (INT) circuit measured using the network analyzer.

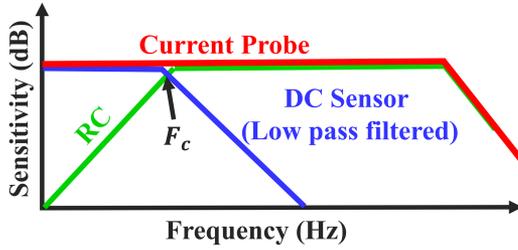


Fig. 5. Illustration of “HOKA” method in frequency domain.

can be expressed by [19]

$$BW_L \approx \frac{R_l}{2\pi L_s} \quad (2)$$

$$BW_H \approx \frac{1}{2\sqrt{L_s C_g}} \quad (3)$$

where  $R_l$  is the load resistance across the end terminal of the RC,  $L_s$  is the self-inductance of the coil, and  $C_g$  is the capacitance between the winding and the shielding layer. With optimized coil parameters, the proposed PCB Rogowski coil has a self-integrating bandwidth ranging from  $BW_L = 7$  MHz to  $BW_H = 300$  MHz [19]. The integrator circuit is designed to stop integration at the transition frequency of  $BW_L$  and provides a unity gain beyond  $BW_L$ . Typically, the performance of an integrator circuit is limited by the op-amp’s bandwidth. Therefore, the self-integrating property of the RC plays a significant role in extending the high frequency bandwidth of the coil. Fig. 4 demonstrates the frequency response of the coil, showing a flat gain curve from 20 kHz to 300 MHz. The noise in the low frequency range is due to the intrinsic noise of the op-amp of the integrator circuit [23]. The subsequent sections will address the dc integration of the shielded PCB RC.

As discussed in Section I, the “HOKA” principle combines two sensors with different frequency responses to achieve a wide bandwidth current sensor. In this article, a dc sensor is used to measure the low-frequency components of the current waveform, while the RC measures the high-frequency components. To combine these two sensors, both sensors must have the same sensitivity ( $Z = V/I$ ) and an adjusted cut-off frequency ( $F_c$ ). Fig. 5 illustrates the “HOKA” principle, where a flat gain curve is achieved (red curve) by adjusting the cut-off frequency while maintaining the same sensitivity. The critical aspect of this implementation is to place the dc sensor outside of the power loop region and use it to capture the low frequency components

of the current waveform. The rationale behind the two separate positions of the sensors in a DPT circuit, a complete design procedure for the current probe, and simulation verifications of the proposed design are discussed in the following sections.

#### A. Location Selection for DC Sensing

In the applications of the DPT circuit, the dc and ac components in the switching current can actually be decoupled. The dc link capacitor ( $C_l$ ) mainly supplies the dc component of the switching current, while the ac component by the dc link capacitor and decoupling capacitor together [24], [25]. Therefore, the dc sensor can be separated from the RC location to avoid introducing extra stray inductance in the power loop. Mostly, the RC coil is placed at the source (S) terminal of the lower device (inside the power loop) to measure the switching current. Fig. 6(a) shows a DPT circuit with arrows indicating the dc ( $I_{Low}$ ) and ac ( $I_{Decap}$ ) components of the switching current ( $I_{SW}$ ) of the device under test (DUT). The time domain waveform indicating  $I_{Low}$ ,  $I_{Decap}$ , and  $I_{SW}$  are shown in Fig. 6(b). The FFT analysis of  $I_{Low}$  and  $I_{SW}$  shows that the low frequency components of the switching current ( $I_{SW}$ ) coincides with the low frequency components of  $I_{Low}$  [see Fig. 6(c)], which validates the concept that the dc component can be measured separately outside the power loop. The dc magnetic sensor can be placed between the dc bulky capacitors ( $C_l$ ) and the decoupling capacitors ( $C_{in2}$ ) [see Fig. 6(a)], which will capture the dc components of  $I_{SW}$ . In contrast, the shielded RC set at the source (S) terminal of the DUT [see Fig. 6(a)] will measure the high-frequency components. These two results added together yields the complete spectrum of the switching current  $I_{SW}$ . Hence, the main advantage of this method is that the dc measurement capability is enhanced for the shielded RC without inserting extra components into the power loop region of the DPT system.

#### B. Design Procedure

Fig. 7. demonstrates the step-by-step frequency response of the current probe system. The RC and integrator circuit exhibits low-frequency noise below 20 kHz, as shown in Fig. 7(a), which can be attenuated by incorporating a high pass filter (HPF) after the RC+INT stage. The cut-off frequency of the HPF can be adjusted by the values of the resistor ( $R_H$ ) and capacitor ( $C_H$ ) components, as given by the following equation:

$$F_{High} = \frac{1}{2\pi * R_H * C_H}. \quad (4)$$

The frequency response of the RC+INT+HPF stage is depicted in Fig. 7(b). Subsequently, the bandwidth of commercially available dc sensors, typically several kHz, is demonstrated by  $F_{HALL}$  in Fig. 7(c). A low pass filter (LPF) is required to adjust the cut-off frequency ( $F_c$ ) of the dc sensor. Similar to the HPF, the cut-off frequency of the LPF can be adjusted by modifying the values of the resistor ( $R_L$ ) and capacitor ( $C_L$ ), as given by the following equation:

$$F_{Low} = \frac{1}{2\pi * R_L * C_L}. \quad (5)$$

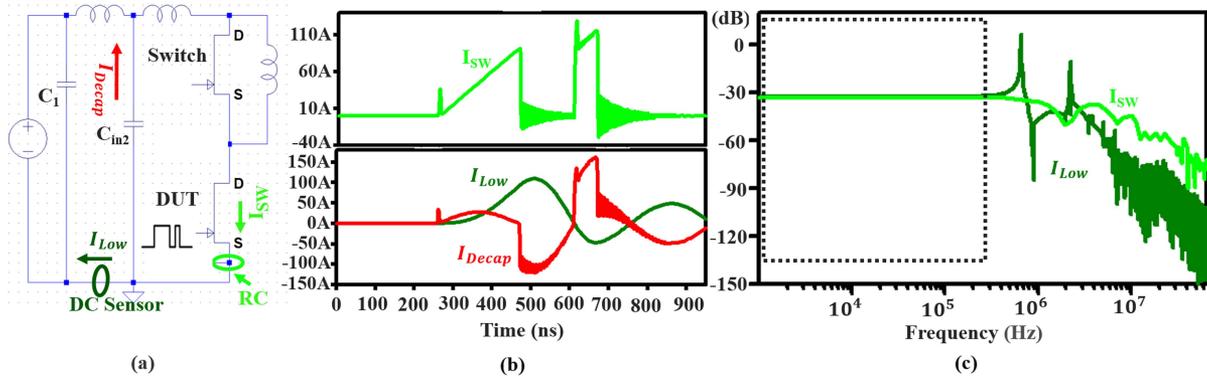


Fig. 6. (a) Double pulse test circuit, (b) time domain waveforms of  $I_{Low}$ ,  $I_{Decap}$ , and the  $I_{SW}$ , and (c) the frequency spectrum of the  $I_{Low}$  and the  $I_{SW}$  waveforms of the DPT circuit showing overlapped low frequency components.

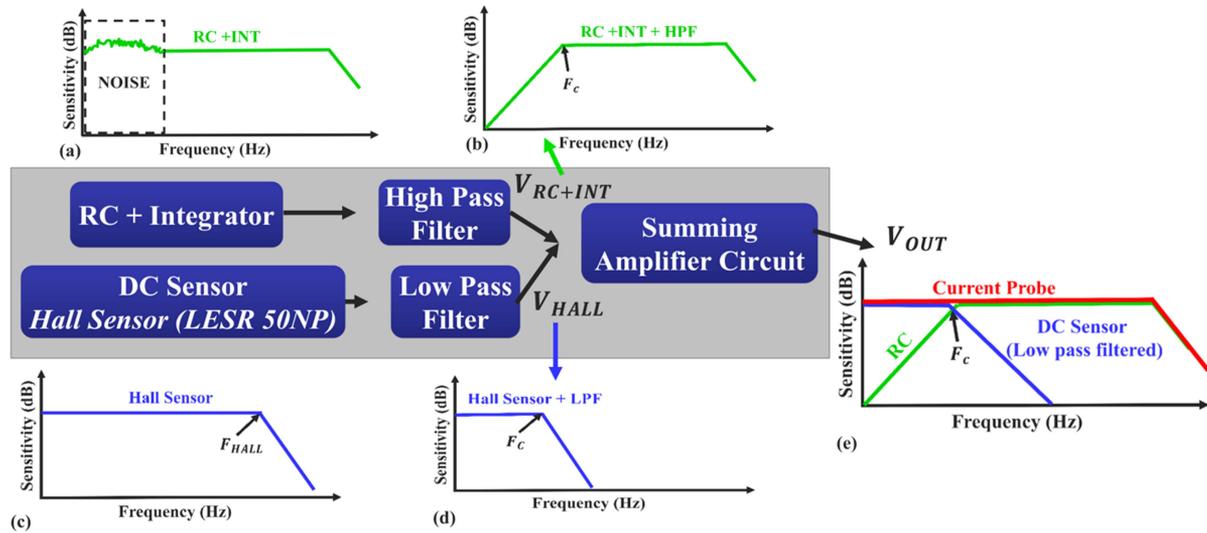


Fig. 7. Step-by-step frequency response of the entire probe system. The illustration of the frequency response of (a) RC+INT, (b) RC+INT with a HPF, (c) hall sensor, (d) hall sensor with LPF, and (e)  $Z_{21} = \frac{V_{OUT} (V_{RC+INT+HALL+ADDER})}{I_{IN}}$ .

The bandwidth of a dc sensor with a LPF is presented in Fig. 7(d). The output of the RC+INT+HPF stage and the dc sensor with a LPF are then combined using a summing amplifier circuit. To avoid overlap between the frequency components, the cut-off frequency of both filters should be set equal to each other, as given by the following equation:

$$F_c = F_{Low} = F_{High}. \quad (6)$$

Finally, by combining the RC and the dc sensor with similar sensitivity and an adjusted cut-off frequency, a flat gain bandwidth of the current probe is achieved, as shown in Fig. 7(e). The comprehensive analysis of the design considerations for the current probe system provided in this section is critical to the study's contribution.

### C. Simulation Verification

The simulation model in Fig. 8 represents the real prototype of the RC and is modeled using the MATLAB algorithm. The coil has a sensitivity of 10 mV/A ( $-40$  dB), and to avoid any

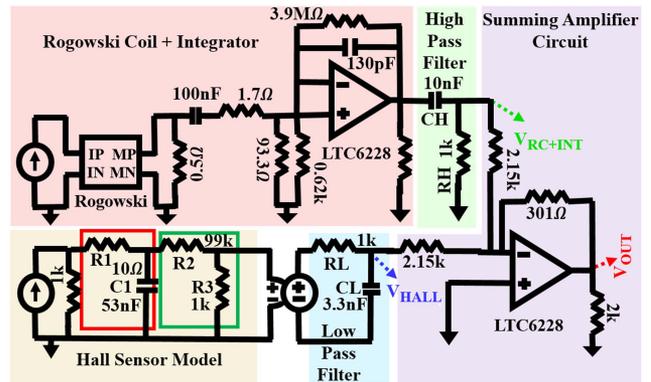


Fig. 8. Simulation model of the current probe system with Rogowski coil and hall sensor.

noise in the system, a margin must be maintained in the selection of the HPF cut-off frequency ( $F_c$ ). Therefore, the HPF cut-off frequency is adjusted to 48 kHz instead of 20 kHz by selecting  $R_H = 10$  k $\Omega$  and  $C_H = 330$  pF (see Fig. 8). Although the

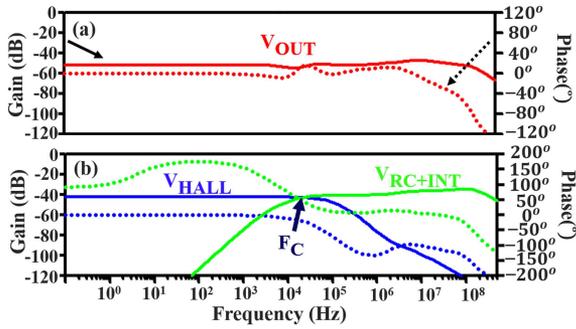


Fig. 9. Simulated waveforms show the gain (solid lines) and phase (dotted lines) of (a) overall output voltage ( $V_{OUT}$ ) and (b) output of the hall sensor ( $V_{HALL}$ ) and output of the integrator ( $V_{RC+INT}$ ), as shown in the circuit in Fig. 8.

cut-off frequency ( $F_c$ ) of the HPF can be obtained from (4), the paralleling effect of  $R_H$  with other nearby resistors shifts the corner frequency to a higher value than 48 kHz. As a result, the values of  $R_H$  and  $C_H$  value have been further adjusted to match the cut-off frequency at 48 kHz.

Since the dc sensor typically behaves like a LPF [12], its frequency response can be compared to that of a LPF. In the simulation, the dc sensor has been modeled using an RC ( $R_1$  and  $C_1$ ) and a voltage divider ( $R_2$  and  $R_3$ ) circuit, which indicate the cut-off frequency and the sensitivity of the sensor (see Fig. 8), respectively. To meet the design parameter requirements, it is essential to maintain the same sensitivity between the dc sensor and the RC. Therefore, a hall sensor (LESR 50NP) with a sensitivity of 12.5 mV/A [20] and a bandwidth of 300 kHz has been chosen as the dc sensor. The cut-off frequency of the hall sensor has been adjusted to 48 kHz using the LPF and selecting  $R_L = 1$  k $\Omega$  and  $C_L = 3.3$  nF shown in (3). To prevent any overlap in the frequency components, both filters (HPF and LPF) must maintain a matched cutoff frequency. The hall sensor will only capture the frequency components from dc to  $F_c$ , while the RC+INT will measure beyond the  $F_c$ . An additional factor to consider while combining two sensors is the phase of the output signals of dc sensor and the RC. To prevent distortion of the measured waveform, the phases of the output signals from the low and high frequency sensors should be zero. The phase diagram of these two sensors is shown in Fig. 9(b). The phase of the hall sensor is zero from dc to  $F_c$ , while the phase of RC+INT is zero beyond the  $F_c$ .

Finally, the adder circuit (see Fig. 8) combines the hall sensor and RC sensor output signals, resulting in a flat gain bandwidth ( $V_{OUT}$ ) from dc to high frequency. To minimize low frequency noise and prevent it from interfering with the low frequency range, an op-amp with this feature should be selected for the adder circuit. The LTC6228 is preferred due to its low noise benefit compared to other op-amps [23]. The simulated frequency response of the probe shows a flat gain curve [see Fig. 9(a)] and verifies the ‘‘HOKA’’ principle. In addition to that, the simulated phase of the entire probe shown in Fig. 9(a) is zero over the desired frequency range, indicating no phase difference between the input and the output signal.



Fig. 10. Prototype system used to verify the HOKA principle in the frequency domain.

### III. EXPERIMENTAL VERIFICATION

This section aims to verify the simulation results presented in Fig. 9 by evaluating the frequency response of the probe prototype. A flat gain curve is expected to be observed in the frequency response of the prototype, which will determine the frequency bandwidth of the current sensor. Subsequently, the sensors will be integrated into the DPT circuit, as depicted in Fig. 6(a). Ultimately, the experimental results will confirm the dc enhancement of the RC without introducing any extra parasitic effects into the power loop of the DPT circuit.

#### A. Frequency Domain Response

A prototype (see Fig. 10) of the current sensor was constructed based on the simulation model presented in Fig. 8. The frequency response of each block was analyzed using a Network Analyzer (E5061B – 3L5), as illustrated in Fig. 7. The S-parameter test port of the Network Analyzer is capable of measuring high frequency response of the system from 300 kHz–GHz range, while the gain-phase test port measures relatively low frequency response ranging from 5 Hz–30 MHz.

The sensitivity of the RC coil was measured to be 10 mV/A (–40 dB) with a low frequency noise below 20 kHz, as shown in Fig. 11(a). As discussed in the simulation model, a HPF was used to attenuate the low frequency noise. It was experimentally verified that the HPF attenuated the low frequency noise, and the cut-off frequency is adjusted to 48 kHz [see Fig. 11(a)]. Fig. 11(b) shows the measured transfer impedance ( $Z_{21} = V/I$ ) of the hall sensor (LESR 50NP). The measured sensitivity of the hall sensor is 12.5 mV/A (–38 dB), which coincides with the given value in the datasheet [20]. As discussed in the simulation, a LPF was included after the hall sensor to adjust the cut-off frequency at 48 kHz, and the experimentally obtained gain curve for the hall sensor with the LPF is shown in Fig. 11(b). The LPF attenuated all frequency components above 48 kHz that passed through the hall sensor.

To experimentally verify the ‘‘HOKA’’ principle, the RC and hall sensor were connected in series so that the same current from the Network Analyzer was measured by both sensors, and the

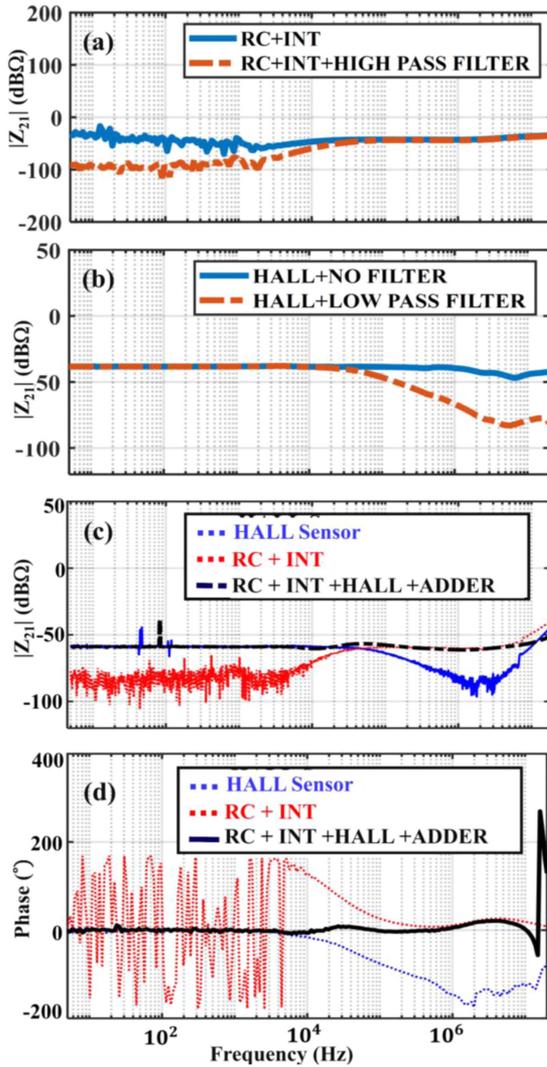


Fig. 11. Measured transfer impedances of (a) Rogowski coil with integrator and HPF; (b) HALL sensor w/o the LPF, (c) the entire system, and the (d) phase measurement of the probe.

outputs of both sensors were sent to the input of the adder circuit. The gain curve of the entire probe is depicted in Fig. 11(c), revealing that the hall sensor dominates from dc to 48 kHz, while the RC+INT dominates beyond 48 kHz. The flat gain curve (black curve) shown in Fig. 11(c) represents the frequency bandwidth of the prototype, extending from low to high frequencies of 20 MHz. This indicates that the dc measurement capability of the RC+INT is enhanced, and the result experimentally verifies the “HOKA” principle. Furthermore, Fig. 11(d) displays the phase measurement for the hall sensor, RC+INT, and the entire probe, confirming zero phase shift across the bandwidth of the probe. The low-frequency noise of the RC+INT system is influenced by the intrinsic noise of the operational amplifier within the integrator circuit.

### B. Time Domain Response

The frequency response analysis of the current probe confirmed its enhanced dc measurement capability with a high

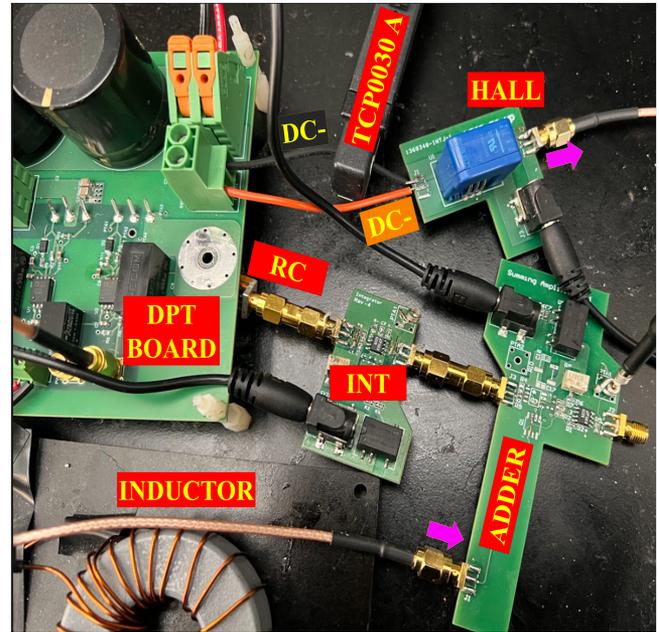


Fig. 12. Implementation of the current probe in a double-pulse test circuit for a half-bridge SiC module.

frequency bandwidth of 20 MHz. To measure the switching current of the SiC device, the probe is integrated into a DPT circuit, as shown in Fig. 6(a). The overall probe connection is illustrated in Fig. 12, where the RC is replaced by a shunt resistor at the power loop location. An external wire is used to place the commercial RC, Tektronix current clamp, and the PCB based RC at the shunt resistor position (see Fig. 12) for measuring the switching current. The hall sensor is placed between the dc-terminals of the decoupling capacitors and the bulky capacitors. This configuration ensures that the current flows through the low resistance path of the hall sensor. Both the RC+INT and the hall sensor generate a voltage that is fed separately to the input terminals of the adder circuit. To convert the output voltage of the probe to current, it needs to be divided by its overall sensitivity (S). In the following sections, the outputs of the probe will be discussed in time domain.

1) *(RC+INT) Output:* To accurately measure the switching current waveform, the bandwidth of the probe must be in the flat gain region, and the relationship between the primary current and output voltage must be linear. This requires a constant mutual inductance ( $Z_{21} = M$ ) between the coil and conductive wire. As the high frequency bandwidth of the RC+INT is 300 MHz, it is capable of measuring high frequency components. To demonstrate the high frequency bandwidth capability of the (RC+INT), the measured switching current waveform of SiC device using RC+INT [see Fig. 13(a)] is compared with a commercial RC, and a Tektronix Current Clamp (TCP0030A). The Tektronix current clamp has a bandwidth ranging from dc to 120 MHz, while the commercial RC is limited to 30 MHz [26]. The captured frequency ripples during turn ON transition using (RC+INT) is 41 MHz, which closely matches with the Tektronix current clamp measurement [see Fig. 13(b)]. The

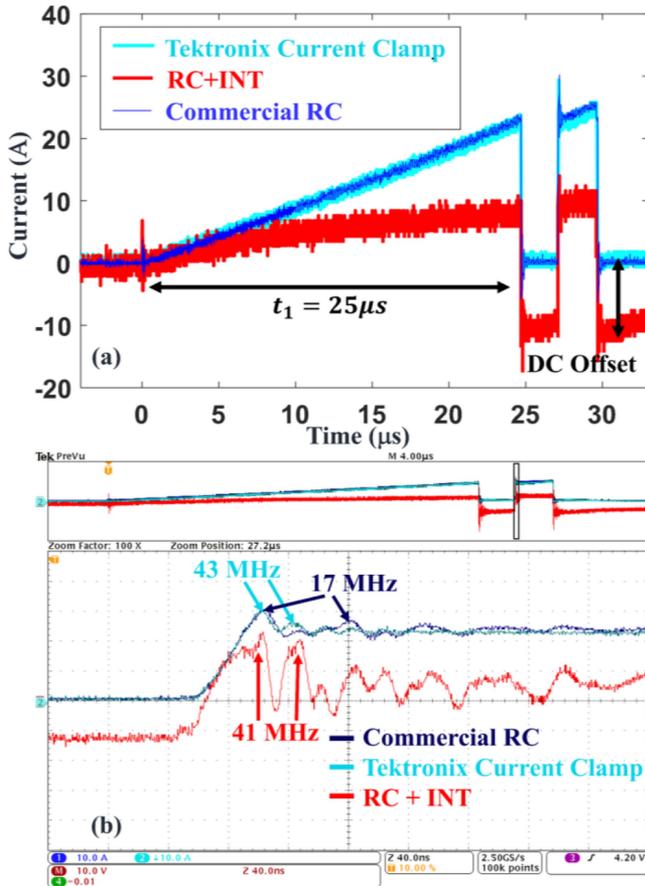


Fig. 13. (a) Output voltage of (RC+INT) at a pulse width of  $25 \mu s$ , and proves the need to improve the dc measurement capability. (b) Measured high frequency ripples using RC+INT and compared with the commercial RC and Tektronix Current Clamp.

precision of the measurement is 4.7%. This verifies the high frequency measurement capability of the (RC+INT). In contrast, the commercial RC measured frequency ripples up to 17 MHz due to the limited high frequency bandwidth [see Fig. 13(b)]. In Fig. 13(a), the RC+INT shows a dc level offset when the pulse width is  $t_1 = 25 \mu s$ . This is because the RC+INT has noise in the required bandwidth region (see Fig. 4) to measure the current at  $t_1 = 25 \mu s$  ( $F_{25 \mu s} = 20 \text{ kHz}$ ). As the (RC+INT) sensor has limited low frequency measurement capability, the higher pulse width waveform starts to create more dc offset. This demonstrates the necessity of improving the dc measurement of RC. Enhancing the dc measurement of the RC will eliminate the dc offset issue, which will be demonstrated in the last section.

2) *Hall Sensor Output*: The position of the hall sensor in the DPT circuit is illustrated in Fig. 6(a). The sensor (LESR-50NP) is placed between dc- terminals of the decoupling and the dc link capacitors (see Fig. 12), and thus, does not interfere in the power loop area. The commercial current clamp is placed at the same location as the hall sensor for the purpose of making a comparison. The measured waveforms from the hall sensor and the Tektronix current clamp are displayed in Fig. 14(a). Other than the low-frequency current captured by the hall sensor, some high-frequency ripples also appear in the waveform. The amount

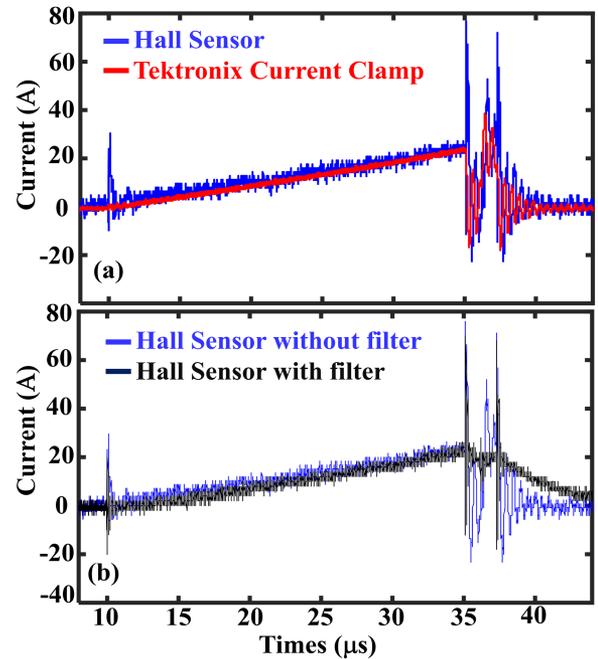


Fig. 14. (a) Comparison between the hall sensor output and the Tektronix current clamp. (b) LPF eliminated the high frequency ripples from the hall sensor output.

of high frequency ripples that leak into the low frequency path depends on the value of the decoupling capacitor, but they will not impact the result since they will be filtered out by the LPF added following the dc sensor [see Fig. 14(b)]. Fig. 14(b) shows the difference between the outputs of the hall sensor with and without the LPF.

3) *(RC+INT+HALL+ADDER) Output*: The entire probe system consists of RC, integrator, hall sensor, the adder circuit, and low and HPFs. The necessity to improve low frequency measurement is depicted in Fig. 13(a) as the RC+INT encountered a dc level shift. The inclusion of the hall sensor improves the dc and low frequency measurement of the RC+INT. The adder circuit combines the low frequency and the high frequency components, reconstructing the real switching current. The output waveform (RC+INT+HALL+ADDER) from the adder circuit is shown in Fig. 15, where the dc level offset is eliminated while keeping the power loop inductance unchanged. This proves that to measure the real switching current, the probe must measure both the low and high-frequency components. The measured sensitivity of the entire probe is  $-58 \text{ dB}$  ( $1.25 \text{ mV/A}$ ), as shown in Fig. 11(c). The measured waveform is compared with the Tektronix current clamp, which verifies the accurate measurement of the switching current waveform. However, the noise is attributed to the increasing gain of the hall sensor at the high frequencies. This fact is further supported by Fig. 14(a) since the spikes are absent when measured with the Tektronix current clamp but present when measured by the hall sensor. The bandwidth of the probe ranges from dc to 20 MHz. The high-frequency issue from the hall sensor will be further studied by employing advanced high-frequency filtering systems to enhance the measurement accuracy.

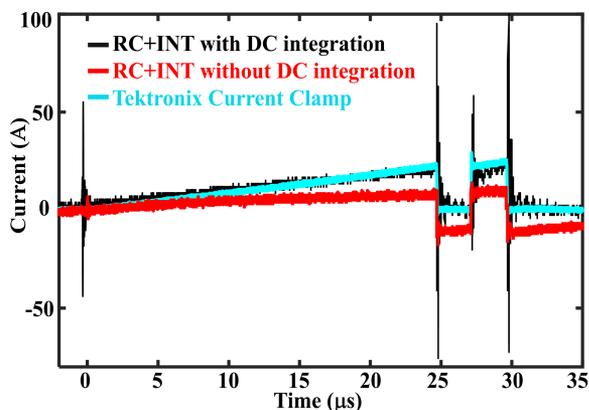


Fig. 15. Improved DC measurement capability after adding the DC sensor showing the DC offset issue is removed from the Rogowski coil and integrator output.

#### IV. CONCLUSION

In summary, this work demonstrates that combining a PCB-based shielded RC with a hall-effect sensor can effectively extend the dc measurement capability of the RC. By placing the RC inside the power loop and the hall sensor outside the power loop, the integration of dc measurement does not aggravate the power loop inductance. Detailed design procedures and considerations are given, and the concept is verified through both simulation and measurement results. The experimental results on a SiC half-bridge power module under DPT system show the successful removal of the dc offset in the current waveform compared to those without the dc sensor added. Future work will focus on eliminating the noises at high-frequency range that arise from the parasitic components of the LPF, which are currently under investigation and will be reported in future publications.

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