A Solid-State Circuit Breaker Without Current Limiting Inductor

Di Zhang, *Senior Member, IEEE*, Yuntao Xu, Jonathan Brandt, Zheyu Zhang, *Senior Member, IEEE*, Dehao Qin, and Dong Dong, *Senior Member, IEEE*

***Abstract*—This paper presents a high-density, high-efficiency megawatt (MW) medium-voltage (MV) solid-state circuit breaker (SSCB) for aviation hybrid electric propulsion applications. The proposed SSCB is based on the mature silicon (Si) insulated gate bipolar transistor (IGBT) devices. With reduced IGBT gate voltage, the proposed SSCB can limit the peak fault current without the fault current limiting inductor. Thus, the specific power density of the SSCB is substantially improved compared with the traditional design. This method has negligible impact on SSCB efficiency, reliability and energy absorbed by the metal-oxide varistor (MOV), while providing additional mechanical layout freedom for power density and insulation enhancement. The potential design challenges due to the extremely high ramp rate of the system fault current and the corresponding solutions are also discussed. The performance of the proposed SSCB is validated with experimental results.**

***Index Terms*—Current limiting inductor, electrified aircraft propulsion (EAP), solid state circuit breaker (SSCB).**

I. Introduction

HYBRID electric propulsion is a promising solution to improving fuel burn efficiency and reducing carbon emission for aviation applications in the near future [1]. The power rating of the electrical power system to support hybrid electric propulsion is in the range of megawatts (MW) to tens of MW. Thus, to reduce the total weight of the electric power system, especially the cable weight, the medium-voltage direct current (MVDC) system is selected due to its numerous advantages compared with the traditional alternating current (AC) system [2].

Manuscript received 28 October 2022; revised 7 February 2023; accepted 28 March 2023. Date of publication 20 April 2023; date of current version 19 July 2023. Paper 2022-TSC-1184.R1, presented at the 2022 IEEE Energy Conversion Congress and Exposition, Detroit, MI, USA, Apr. 20, and approved for publication in the IEEE Transactions on Industry Applications by the Transportation Systems Committee of the IEEE Industry Applications Society [DOI: 10.1109/ECCE50734.2022.9948197]. This paper is an extension of a conference paper, "A Solid-State Circuit Breaker without Current Limiting Inductor", in ECCE 2022. This work was supported by U.S. National Aeronautics and Space Administration (NASA) under Grant 80GRC020T003. *(Corresponding author: Di Zhang.)*

Di Zhang, Yuntao Xu, and Jonathan Brandt are with the Naval Postgraduate School, Monterey, CA 93943 USA (e-mail: zhangdi@ieee.org; yuntao.xu@nps.edu; jonathan.brandt@nps.edu).

Zheyu Zhang and Dehao Qin are with the Clemson University College of Engineering and Sciences, Clemson, SC 29634-0002 USA (e-mail: zheyuz@clemson.edu; dehaoq@g.clemson.edu).

Dong Dong is with the Virginia Polytechnic Institute, Blacksburg, VA 24061 USA (e-mail: dongd@vt.edu).

Color versions of one or more figures in this article are available at https://doi.org/10.1109/TIA.2023.3268646.

Digital Object Identifier 10.1109/TIA.2023.3268646

As in other MVDC applications, hybrid electric propulsion needs protection devices to handle the system short circuit fault. Although the mechanical breaker and hybrid circuit breaker have such benefits as low conduction loss, the solid-state circuit breaker (SSCB) is more desirable mainly due to its superfast response, arc free operation and simple structure [3]. However, the aviation hybrid electric propulsion imposes strict requirements on the specific power of SSCB. For example, a 100 kW/kg is targeted for SSCB to make the hybrid electric propulsion feasible for aviation applications [4].

The traditional SSCB design mainly consists of the semiconductor switches, the voltage clamping circuit and the fault current limiting device. Due to low impedance in the MVDC system, the short-circuit fault can cause transient current with fast rising speed measured as *di/dt*. To limit the dc fault current and gain more time for the fault detection and clearance circuit, the traditional fault current limiting device is a directly installed inductor. Such a method is simple and robust. However, to limit the current rising speed under full dc bus voltage, carry full system current continuously and further handle a transient peak fault current without saturation, such a fault current limiting inductor is very heavy. To meet the specific power target of 100 kW/kg, it would be of necessity to eliminate the current limiting inductor from SSCB while keeping the same current limiting capability.

Extensive studies conducted on SSCB have been reviewed in [3]. As summarized in [3], most of the research focused on the power semiconductor technologies, circuit topology, voltage clamping circuit, gate driver and fault sense and trip electronic circuit. However, the method to eliminate the current limiting inductor is not covered. Most recent studies on SSCB continue to concentrate on the forementioned topics [5], [6], [7], [8], [9], [10], [11], [12], [13], [14], [15], [16], [17], [18], [19], [20], [21], [22], [23], [24], [25], [26], [27]. In these studies, either a fault current limiting inductor is involved, or sufficient system inductance is assumed to limit the fault current rising speed and peak value. For applications where the system inductance is high enough, the fault current limiting inductor can be optional. However, in applications where the breaker is connected directly to a low-impedance source (e.g., a battery or capacitor bank), when a short circuit occurs directly across the output terminals, the fault current limiting device is needed. In hybrid electric propulsion, the battery can be the main or auxiliary source and rectifiers' dc capacitors can be connected to the dc bus directly, so the breaker design cannot depend on the assumption that a high system impedance is always present to limit the fault current.

In [6] an air-core transformer is proposed as the fault current limiter. [7] and [8] discuss the use of a transformer or coupled magnetic components to limit the fault current. In spite of potentially better performance than the traditional inductor, they, as magnetic components, are not substantially lighter than inductors.

It is well-known that the silicon (Si) insulated gate bipolar transistor (IGBT) short circuit current can be limited by reducing the gate voltage [28], [29]. However, no known research has leveraged this IGBT characteristic to eliminate the current limiting inductor inside an SSCB for high specific power which is critical for aviation applications. [30] proposes to use the IGBT with reduced gate voltage to limit the peak fault current regardless of the system impedance. The proposed solution does not involve any additional fault current limiting device. The current limiting function is integrated into the semiconductor device without weight penalty. With the current limiting inductor eliminated, the 100 kW/kg specific power target of SSCB becomes feasible. Also, with the proposed solution, the peak fault current is independent of the fault detection and response time. Thus, a slower response time can be implemented. This simplifies the control system design and improves the immunity to system noise during normal operation. This also brings in additional design freedom for mechanical layout optimization to reduce weight/volume and to meet insulation requirement at high altitude which is another critical metric for the hybrid electric propulsion system. The downside of the proposed solution is higher conduction loss in IGBT under the normal operating conditions, higher thermal stress inside IGBT during fault transients and some new design issues related to the extremely high fault current ramping rate. This paper is an extension of [30] with more design details, challenges, and experimental results. The analysis and test results presented in the paper clearly prove that the penalty and risks are negligible compared with the benefits of the proposed solution.

This paper is organized as follows: Section II presents the operation principle of the proposed SSCB in an example system. The benefits and penalties are discussed in Section III. Section IV focuses on one challenge due to the super-high current rising speed and the corresponding solution. All the analysis and feasibility of the proposed solution are verified with experimental results in Section V, followed by conclusions in Section VI.

II. Operation Principle of the Proposed Solid-State Circuit Breaker

A. Traditional Design

To better illustrate the improvement of the proposed SSCB, the operation principle of the traditional SSCB design is briefly reviewed first. As mentioned in Section I, the traditional SSCB design mainly consists of the semiconductor switches, voltage clamping circuit and fault current limiting device. One example is depicted in Fig. 1. There are two identical SSCBs, with one installed in each pole of the dc system. Each SSCB consists of two anti-series Si IGBTs with anti-parallel diodes to carry and break bi-directional currents. The metal-oxide varistor (MOV) is

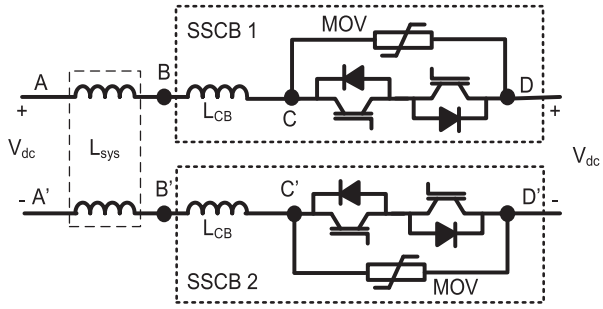

Fig. 1. Topology of the tradition SSCB.

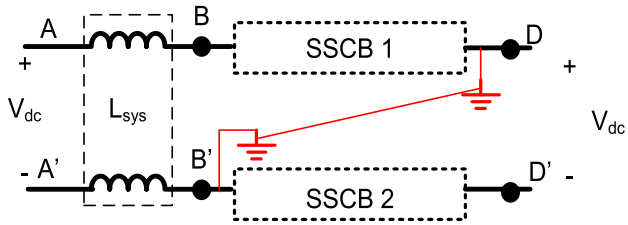

Fig. 2. Impact of double system ground faults.

connected in parallel with the semiconductor devices to clamp the peak voltage. L_{sys} represents the system inductance from the dc power system components, such as long cables, and L_{CB} represents the fault current limiting inductor inside the SSCB. Other types of semiconductor switches, voltage clamping circuits and/or fault current limiting device can be considered in the SSCB implementation. But the operation principle stays the same.

The reason to install one SSCB in each pole is to enable the system to handle single point ground fault. As a flight critical component for the hybrid electric propulsion, the MVDC system needs to continue running at full power with single point ground fault. In other words, even if there is a ground fault in the system, the SSCB must have the capability to clear the fault current when a second ground fault occurs. As shown in Fig. 2, the SSCB on the negative dc pole can be bypassed by the second system ground fault at point D together with the first system ground fault at point B'. Thus, it is of critical necessity to involve one SSCB on each dc pole. But this also doubles the power loss and weight of SSCB in each bus location, which make it even more challenging to meet the efficiency and specific power targets.

When both SSCBs are functional, each one only needs to block half the dc link voltage. When only one SSCB is functional, such as the case in Fig. 2, the SSCB must be able to clear the fault by itself. This is the worst case when designing the SSCB. In this paper, only the worst case is analyzed and the dc system can be simplified as shown in Fig. 3. Here, L_{Line} is the total inductance consisting of L_{sys} and L_{CB} as introduced in Fig. 1, which limits *di/dt* of the system fault current.

The typical switching waveforms of the traditional SSCB are shown in Fig. 4. The top figure depicts the waveform of the voltage across SSCB (V_{SSCB}) and the bottom figure depicts the waveforms of the current flowing through IGBT(I_1) and MOV(I_2).

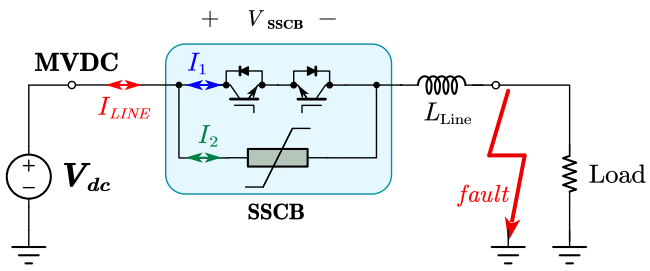

Fig. 3. SSCB in a MVDC system.

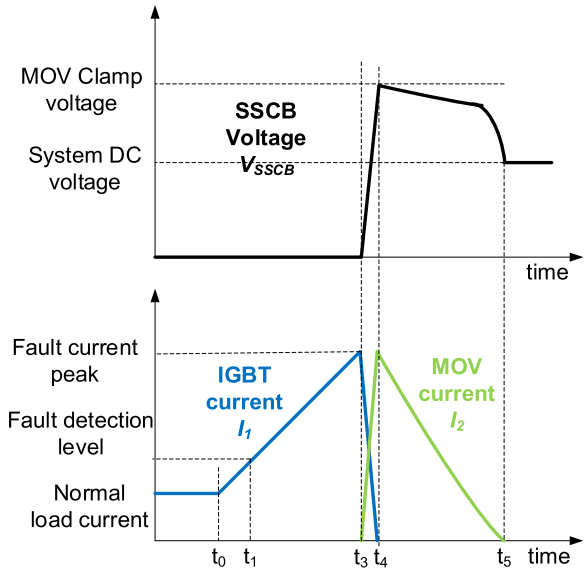

Fig. 4. Typical switching waveforms of the traditional SSCB.

As shown in Fig. 4, before t_0, the system is under normal operation, V_{SSCB} is close to zero and the system current only flows through the IGBT. At t_0, a short circuit fault occurs, and the IGBT current (I_1) will increase rapidly. The rising speed is determined by the dc bus voltage (V_{dc}) and the total value of system inductance (L_{sys}) and current limiting inductor (L_{CB}) as in (1).

$$\frac{di}{dt} = \frac{V_{\rm dc}}{L_{\rm sys} + L_{CB}} \tag{1}$$

Once the fault current exceeds the predefined protection threshold (I_{th}) at t_1, the fault protection scheme is activated. After that, the fault current will keep increasing until the IGBT is turned off at t_3 and the fault current is fully commutated from IGBT to MOV around t_4. The time difference between t_1 and $t_4>$ is called the response time t_d, which includes the process time of the control circuit to generate the turn-off command and the time to fully turn off the IGBT.

The peak fault current can be estimated as

$$I_{pk} = I_{th} + \frac{V_{dc}}{L_{sys} + L_{CB}} t_d \tag{2}$$

After the fault current is commutated to MOV, the MOV's clamping voltage is higher than the dc bus voltage. Thus, after $t_4>$, the MOV's clamping voltage will drive the current down and eventually clear the fault at t_5.

Based on (2), if L_{sys} is close to zero in the worst case, a current limiting inductor must be installed to limit *di/dt*, so that the peak current will not exceed the maximum value within t_d. Although a lower I_{th} and t_d can help to limit the fault current, which means the protection system can respond to a system fault earlier and faster, their impact is limited if the system current rising speed is very high. In addition, a lower I_{th} or t_d could make the SSCB sensitive to the system noise, especially in a harsh EMI environment, such as the converter based high power system.

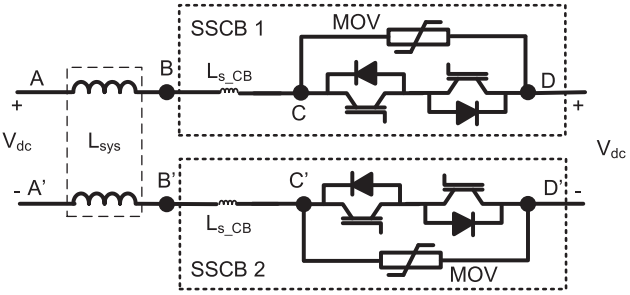

Fig. 5. Topology of the proposed SSBC in an example system.

B. Proposed SSCB

The circuit diagram of the proposed SSCB is depicted in Fig. 5. Compared with the traditional design, the current limiting inductor is eliminated, and L_{s_CB} only represents the stray inductance inside the SSCB which is typically in the range of tens of nanohenries. The current limiting function is realized with reduced IGBT gate voltage.

As is well known, the IGBT normally operates in the saturation region when the load current is within its rated range, and the voltage drop across the device usually is only a few volts. However, once the current is sufficiently high, IGBT will exit the saturation region and enter the active region. Consequently, the IGBT terminal voltage will increase dramatically with the load current, until the load current reaches the IGBT saturation current level. In other words, the system current is only determined by the IGBT's saturation current level and the IGBT acts similar to an ideal current source. To maintain the saturation current level, IGBT can adapt its terminal voltage automatically until there is no net voltage to drive the system current up or down, like an active current limiter. The IGBT's saturation current level is mainly determined by the gate voltage and device temperature. By adjusting its gate voltage, the peak system fault current can be selected.

The typical switching waveforms of the proposed SSCB are shown in Fig. 6.

Just like in Fig. 4, the top figure in Fig. 6 shows the waveform of the voltage across the SSCB and the bottom figure shows the waveforms of the current flowing through the IGBT and MOV. Before t_0, the system is under normal operation, the voltage across the SSCB (V_{SSCB}) is close to zero and the system current

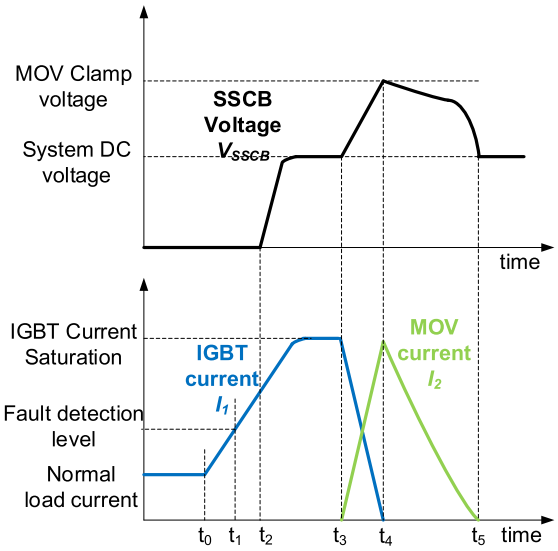

Fig. 6. Typical switching waveforms of the proposed SSCB.

TABLE I
KEY SPECIFICATIONS OF AN EXAMPLE SSCB

Rated dc bus voltage	2 kV
Rated dc current	1.2 kA
Protection Threshold Current	3 kA
Peak fault current	5 kA
Specific power	100 kW/kg
Efficiency	99.5%
Fault response time	>1.5 µs

only flows through the IGBT. At t_0, a short circuit fault occurs, and the IGBT current (I_1) starts to increase. Compared with the results in Fig. 4, without the current limiting inductor, the system fault current rising speed is much higher. Like the case with the traditional design, the fault current is detected at t_1 and after t_d, the IGBT is turned off at $t_4>$. After that, the system fault current is cleared in the same way as in the traditional design.

Unlike in the traditional SSCB, in the proposed SSCB, when the system fault current is high enough between t_1 and t_3, the IGBT exits the saturation region and enters the active region around t_2. Consequently, the voltage across the IGBT increases rapidly together with the system fault current until it reaches the system dc voltage level as shown in Fig. 6. At this moment, the voltage drop across the system inductance is zero, so the system fault current will stop increasing and be clamped at the IGBT saturation current level until the IGBT is turned off. In this process, the IGBT replicates the same current limiting function without a current limiting inductor.

III. IMPACTS OF THE PROPOSED SSCB

To better explain the impacts of the proposed SSCB, a solid state circuit breaker is detailed as the example in this section with key specification summarized in Table I.

A. Power Density

One key benefit of the proposed SSCB is its high specific power, which is undoubtedly critical for aviation applications, due to the elimination of current limiting inductors.

To meet the 100 kW/kg specific power target, the total weight of two 2 kV 1.2 kA SSCBs on two dc poles is only 24 kg, or 12 kg each.

In this design, the response time (t_d) is selected to be 1.5 μs, the peak fault current is limited to 5000 A, and the fault detection level is set to be 2000 A. If no system inductance exists, to achieve this goal, the value of current limiting inductor can be calculated as

$$L_{CB} = \frac{V_{dc} t_d}{\Delta i} = \frac{2000\text{V} \times 1.5\mu\text{s}}{(5000 - 2000)\,\text{A}} = 1\ \mu\text{H} \qquad (3)$$

Such a 1 μH inductor needs to carry 1200 A current continuously and to handle a transient current of 5 kA without significant core saturation. In addition, as mentioned in Section II, the current limiting inductor is inside the SSCB and can be bypassed upon double ground faults. Thus, one inductor is needed for each dc pole to allow continuous operation of the system with a single point ground fault.

Without a detailed inductor design, the weight of such a 1 μH inductor can be estimated based on the existing design with similar current ratings. As reported in [31], a 1.5 μH 430 A inductor weighs 3.3 kg so the energy density is 42 kJ/kg. With a similar energy density, the weight of such 1 μH 1200 A inductor is about 17 kg, which has not even considered the requirement to handle the peak transient current that is 4 times the nominal value. With a much larger core size to handle the peak current, it would be no surprise if the actual weight of the inductor is higher than 20 kg.

With an optimized design, the inductor weight could be lighter than the estimated value. But it is obvious that with the traditional current limiting inductor, it is impractical for each SSCB to meet the 12 kg weight or 100 kW/kg specific power density target. Thus, the traditional design cannot meet the aviation application requirements.

B. Efficiency

Most of the device vendors recommend driving their IGBTs with a 15 V gate voltage. Although a higher gate voltage can further reduce the IGBT conduction loss, too high a gate voltage could damage the device gate. 15 V happens to strike a good balance between the device conduction loss and gate voltage safety margin.

With a reduced gate voltage, the IGBT conduction loss will increase. However, a detailed analysis can demonstrate that with a carefully chosen gate voltage, such additional power loss or efficiency penalty is negligible in the intended load range due to the nature of minority carrier devices.

In the example SSCB design, to carry 1.2 kA continuously, block 2 kV dc and meet the efficiency target of 99.5%, the 3.3 kV 1500 A FZ1500R33HL3 IGBT module by Infineon is selected. With 15 V gate voltage, the IGBT saturation current level is 6.4 kA at 150 °C junction temperature [32]. At lower junction temperature, the saturation current level is even higher, which cannot meet the 5000 A peak current requirement.

The gate voltage selection is a trade-off between the IGBT current saturation value and conduction voltage drop. Lower gate voltage results in lower IGBT saturation current during faults but

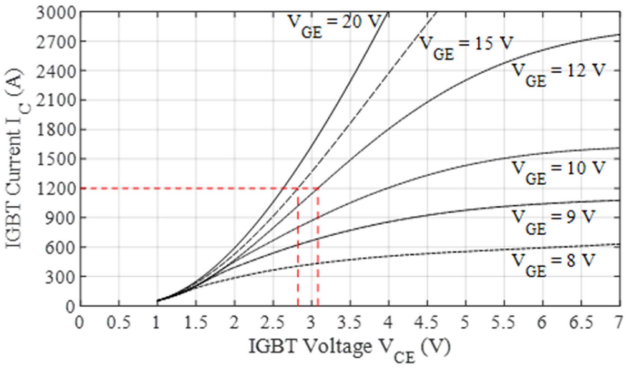

Fig. 7. V-I curve of FZ1500R33HL3 dependence on gate voltages at 150 °C junction temperature [32].

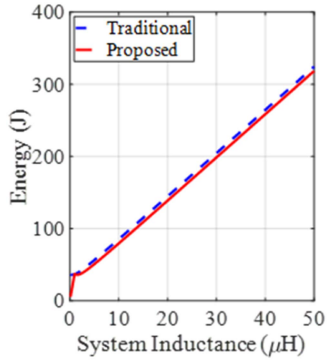

Fig. 8. MOV energy comparison.

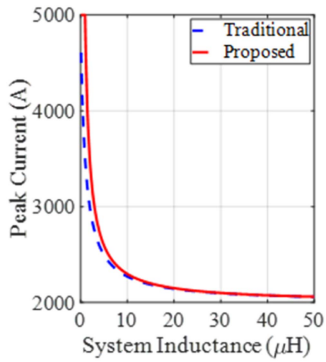

Fig. 9. Peak current comparison.

higher dissipation during normal conduction. The final selection of V_{GS} aims to achieve a good compromise to meet the SSCB design requirements. 12 V is picked based on a series of testing. With 12 V gate voltage and 25 °C die temperature, the IGBT starts to enter active region when carrying 3 kA and the IGBT terminal voltage (V_{ce}) increases to 20 V correspondingly. This is shown as the moment of t_2 in Fig. 6. The IGBT can enter active region when carrying only 2.5 kA if the die temperature is increased to 125 °C [32]. The datasheet doesn't provide the saturation currents with different gate voltages. Thus, tests are conducted to measure the saturation currents at different gate voltages at room temperature.

The V-I curve of the IGBT module with different gate voltages are shown in Fig. 7.

As shown in Fig. 7, when carrying 1200 A the typical voltage drop is 2.8 V with 15 V gate voltage and 3.1 V with 12 V gate voltage, resulting in a voltage difference of 0.3 V. In other words, the reduction of gate voltage from 15 V to 12 V introduces an additional power loss of 360 W per IGBT. The impact on the overall SSCB efficiency is only 0.03% in the 2.4 MW system.

A 0.03% efficiency loss in the semiconductor devices is negligible especially considering that the power loss in the current limiting inductor is eliminated in the proposed solution. In addition, the data in Fig. 7 is for 150 °C junction temperature. Since the device junction temperature is lower under normal operation, the additional loss could be even lower.

C. MOV Energy

Energy absorbed by the MOV is another design constraint. Repetitive absorption of excessive energy is a "lifetime-threatening" process that may cause overheating, nonlinear degradation, and mechanical failure in a MOV structure [33], [34], [35], which may determine the reliability of the SSCB.

As shown in Fig. 6, if the MOV clamp voltage is approximated to be constant at V_{clamp}, the system current or MOV current will decrease with a constant speed, and it can be modeled as a function of time

$$i_{MOV} = I_{peak} - \frac{V_{clamp} - V_{dc}}{L_{sys} + L_{CB}} t_{clear} \tag{4}$$

where I_{peak} is the peak value of fault current, L_{sys} is the system inductance, L_{CB} is internal inductance of SSCB and t_{clear} is elapsed time after the current is fully commutated from the IGBT to the MOV (i.e., from $t_4>$ to t_5 in Fig. 6).

Since the energy absorbed by the MOV is the integration of the product of the instantaneous voltage across the MOV and the instantaneous current through the MOV, the total energy absorbed by the MOV can be calculated as

$$E_{MOV} = \frac{1}{2} \left(L_{sys} + L_{CB}\right) I_{peak}^2 \frac{V_{clamp}}{V_{clamp} - V_{dc}} \tag{5}$$

From (5), when the MOV clamping voltage and system voltage are fixed, the MOV energy is proportional to the sum of system inductance and SSCB internal inductance and the square of the peak current.

Based on (2) and (5), the peak current and energy absorbed by the MOV as a function of system inductance for the traditional design and proposed design are summarized in Figs. 8 and 9. In both cases, the MOV's clamp voltage is set to be 3 kV, the system dc voltage is set to be 2 kV, fault response time is 1.5 μs and the system inductance varies in the range of 200 nH and 50 μH. In the traditional design, the current limiting inductor is assumed to be 1 μH; 50 nH is assumed to be the SSCB's internal parasitic inductance in the proposed design.

As can be observed, although the peak current is higher with the proposed SSCB solution, the MOV in the proposed SSCB design absorbs similar or lower energy compared to that in the

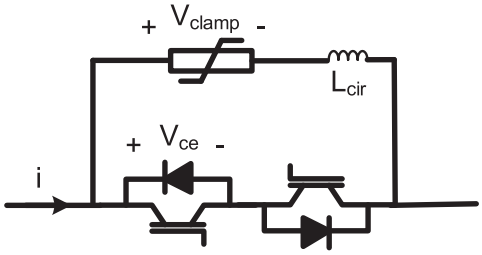

Fig. 10. Commutation loop between IGBT and MOV.

traditional SSCB. This is mainly because the energy stored in the current limiting inductor is eliminated.

D. Mechanical Design Freedom

As demonstrated in Figs. 4 and 6, after the IGBT is turned off, the system current is commutated from the IGBT to the MOV between t_3 and t_4. As in any converter power stage, there is parasitic inductance in the commutation loop between the IGBT and the MOV as shown in Fig. 10. In Fig. 10, the current flows from left to right and the left IGBT needs to be turned off. The commutation loop parasitic inductance is represented as L_{cir}. Such parasitic inductance cannot be eliminated, and its value is mainly determined by the mechanical layout. When the system fault current is commutated from the IGBT to the MOV, a transient voltage is generated due to high *di/dt*. Such a transient voltage together with the clamping voltage across MOV determines the maximum voltage across the IGBT.

Thus, the peak voltage across the IGBT can be estimated as

$$V_{peak} = V_{clamp} + L_{cir}\frac{di}{dt} \tag{6}$$

where L_{cir} is the commutation loop inductance and V_{clamp} is the MOV's clamping voltage when carrying the fault current.

It is critical to limit such voltage below IGBT's maximum voltage rating to avoid IGBT damage. From (6), to reduce the transient voltage, either the current is commuted with a lower speed, or the mechanical structure needs to be optimized to reduce the parasitic inductance.

As mentioned above, to limit the peak fault current below 5 kA with 1 μH inductance, the response time needs to be 1.5 μs or lower, which includes the fault detection time and IGBT turn-off time. Thus, the IGBT needs to be turned off in less than 1μs. In other words, the *di/dt* is higher than 5 kA/μs. To limit the transient over voltage across the parasitic inductance below 500 V, the parasitic inductance needs to be below 100 nH.

Such low parasitic inductance can be realized with a compact mechanical layout and/or laminated busbars, which works for most applications. However, these methods can introduce big challenges for aviation applications. First of all, a compact mechanical layout and laminated busbar will introduce insulation challenges, such as partial discharge (PD), and require special design for high altitude operation [36], [37]. If additional encapsulation material is used to enhance the insulation performance, the weight of SSCB will increase, leading to a lower power density. In addition, the laminated busbar can be much heavier than regular busbar, because the current path cannot be fully controlled and not all the conductor material can be fully leveraged to carry current evenly.

With the proposed SSCB solution, the peak current is limited to IGBT's saturation current level independent of the fault response time. Thus, it is safe to apply a fault response time much longer than 1.5 μs, so the IGBT can be turned off in a much slower manner. For example, if the turn-off time is increased to 4 μs, the parasitic inductance can be increased to 400 nH while still limiting the transient voltage below 500 V.

Please note that such slow turn-off will introduce additional switching loss but have negligible impacts on the SSCB's performance or reliability.

However, this can provide tremendous design freedom for mechanical layout. The component layout can be optimized for easy assembly and higher clearance to handle insulation challenges at high altitude instead of low parasitic inductance. In addition, non-laminated busbar with special shapes can be used to accommodate the mechanical layout for volume and weight reduction.

E. Reliability

With the rated gate voltage, e.g., 15 V, the typical IGBT saturation current level is around 5 times of its rated current and the IGBT can only carry such current for a very short time, e.g., 10 μs. During this short period of time, the IGBT blocks full dc voltage and carries high current simultaneously. In the example design, each IGBT can carry 5 kA and block 2 kV at the same time, leading to a 10 MW power loss. Such a high-power loss can transiently increase the IGBT's die temperature. Although the IGBT module's reliability is typically related to thermal stress quantified as temperature swings occurring in the semiconductor dies and the power module structure, the temperature surge caused by the proposed solution can also potentially impact the device lifetime and reliability.

In the proposed SSCB, this issue is mitigated with lower gate voltage and shorter duration time. With 12 V gate voltage, the short circuit current is reduced by roughly 30% compared with the typical case with 15 V gate voltage, and the duration is limited to be less than 10 μs, e.g., around 5 μs. In addition, the IGBT only blocks up to 2 kV instead of 2.5 kV and the junction temperature is much lower than 150 °C as specified in the short-circuit test condition in [32]. Therefore, the total accumulated loss is reduced to be less than 50% of the worst case listed on the datasheet with additional junction temperature margin. If both SSCBs operate identically, each SSCB only needs to block half of the dc link voltage so the power loss can be further reduced by half.

There is no systematic study on the negative impact of simultaneous high voltage and high current, or high power dissipation, on device reliability. According to [38], the IGBT can tolerate thousands of short circuit pulses if E_{SC}, the energy incurred during the short circuit, is below the critical energy E_C. But this is only for one specific device. More analysis and experimental evaluation are needed to quantify the impact.

For the proposed SSCB, the worst case is when one SSCB pole is bypassed and the remaining pole has to clear the fault. This is a very rare case in the operation lifetime of SSCB, since two ground faults need to occur at specific locations to bypass one SSCB pole. Usually a single ground fault can be detected by voltage monitoring, followed by proper procedure to eliminate the fault condition prior to a second fault. The SSCB is intended to be used as a current interruption component in all the conceivable application scenarios, including but not limited to the short circuit faults. In most cases, the SSCB only needs to cut normal current with the IGBT not in active mode. For example, a scheduled load shedding or an overload could necessitate current interruption, which is less stressful compared with short circuit fault clearing.

Due to the low probability of worst case scenario, its negative impact on the overall reliability of SSCB is very limited. By the time this paper is prepared, the same IGBT module has been tested in this condition for more than 100 times. No failure or performance degradation has been observed, which can partially support the conclusion. Even though the operation of IGBT in this mode reduces the lifetime of the SSCB, as long as such negative impact can be quantified, the SSCB can always be replaced after a certain number of operations. Considering its benefits, the proposed method still is a practical and advantageous solution.

IV. Design Challenges With High System Current Rising Speed

The proposed SSCB can limit the peak fault current. However, due to the lack of current limiting impedance, the system fault current can rise with a high speed. Such high *di/dt* can introduce new challenges which do not exist in the traditional design. Most of them are related to the control of IGBT gate voltage. For MW MV applications, multiple IGBT chips are packaged inside one module and controlled as one device. The gate drive can only access the gate terminal of the module, not the gates of individual IGBT chips due to their distributed nature. This can result in nonuniform current distribution and potential oscillation during the high *di/dt* transient. In addition, magnetic coupling between the gate loop and the power circuit becomes significant at high *di/dt* and varies with the detailed current flow pattern.

Although Kelvin terminals are provided at the IGBT module for the gate drive connection and the common source inductance is eliminated, the coupling between the gate loop and power circuit is apparent from the Infineon IGBT module layout as shown in Fig. 11. The fault current flowing through busbars inside and outside the IGBT module generates a magnetic field which could be coupled to the gate loop. Due to the extremely high ramp rate of the fault current, such magnetic field can induce a voltage between the module gate terminal and the actual gate terminal of the IGBT chips. The current flow pattern in the power circuit depends on the busbar design and power cabling external to the IGBT module and affects the magnitude and polarity of such magnetic coupling.

Although V_{ge} cannot be measured directly, its impact on the IGBT saturation current level can be observed. If V_{ge} is increased because of the magnetic field, the peak fault current becomes higher than the expected value with V_{ge_ext}. Reversely, the peak fault current becomes lower if V_{ge} is decreased due to magnetic coupling. As presented in the next section, the system fault current peak value can vary by a factor of two with different busbar configurations.

Fig. 11. Infineon IHM/IHV B module package and internal layout [39].

The mutual coupling between the gate loop and power circuit is dependent on the module internal structure as well as external busbar design. Although such coupling theoretically can be leveraged to reduce the gate voltage at the fault moment to further limit the peak fault current, in this SSCB design, the busbar is optimized to mitigate the coupling between the fault current and the gate loop, so that the peak fault current is only dependent on the external gate drive voltage.

Because there is no detailed information of module internal layout, the busbar is designed and optimized based on the trial-and-error method. The experimental results presented in the next section verify the design.

The high *di/dt* of system fault current may also cause oscillation in the gate loop. The issues, analysis and solutions have been reported in [40]. For this paper, the gate driver has been properly designed and optimized. Thus, no oscillation issues are observed in the test results.

V. Prototyping and Experimentation

A. Power Stage Description

An 2 kV/1 kA SSCB prototype is built and tested for performance evaluation. Fig. 12 presents the SSCB test circuit diagram, and a photograph of the test setup is shown in Fig. 13.

The SSCB consists of two IGBT modules (Infineon P/N FZ3300R33HL3) connected back-to-back, an RC snubber, and an electronically triggered MOV (eMOV) [41]. The eMOV can reduce the peak clamping voltage inside the SSCB during fault clearing, enabling the use of 3.3 kV IGBT for the 2 kV system. This is the key technology to improve the SSCB's efficiency. The RC snubber (R $= 0.47\ \Omega$ and C $= 1.5\ \mu$F) limits the transient

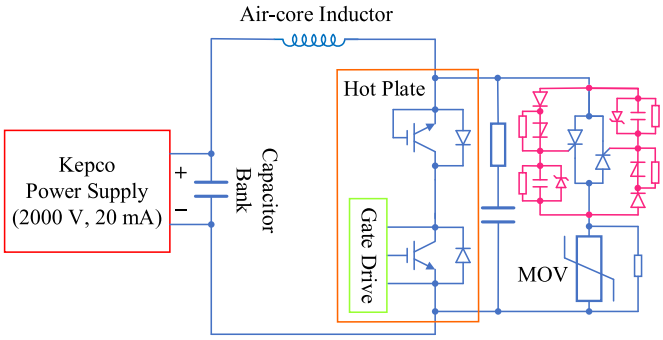

Fig. 12. Circuit diagram of the switching test bed.

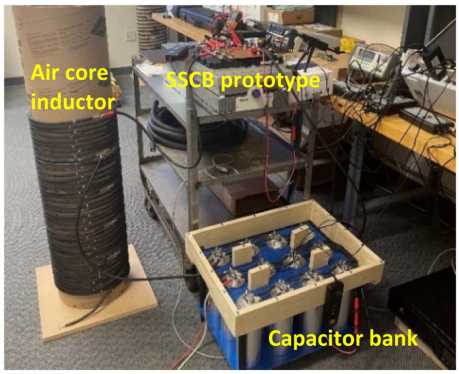

Fig. 13. Photograph of the switching test bed.

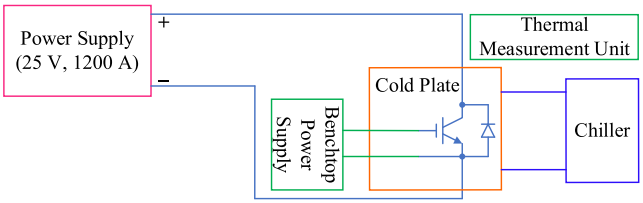

Fig. 14. Circuit diagram of the thermal test bed.

voltage rise during IGBT turn-off and helps to mitigate the stress on the IGBT. The eMOV consists of a thyristor module as well as a MOV. The gates of the thyristor module are controlled by a passive circuit consisting of breakover diodes (BOD). Compared with the conventional MOV, the eMOV allows the use of a MOV of lower clamping voltage without incurring excessive static dissipation during the SSCB off-state, thus optimizing the overall SSCB performance. A capacitor bank is utilized to emulate the DC source and an air-core inductor represents the system inductance, which is adjustable between 0–50 μH. Switching test results are detailed in subsection D.

B. Thermal Evaluation

In addition to switching test, the SSCB conduction loss and thermal behavior are also evaluated. Figs. 14 and 15 present the circuit diagram and photograph of the thermal test setup, respectively.

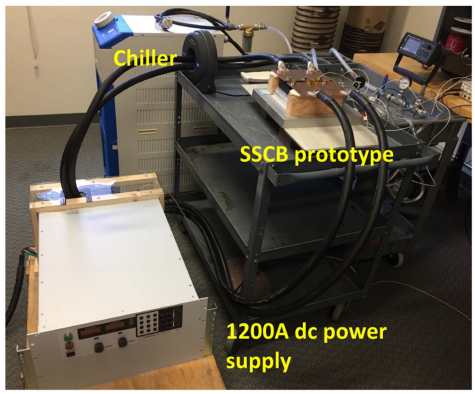

Fig. 15. Photograph of the thermal test bed.

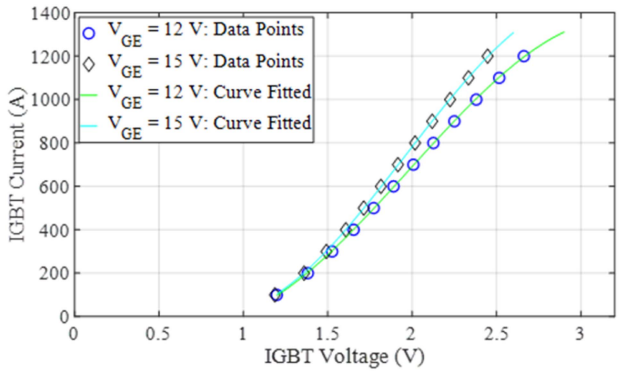

Fig. 16. Measured IGBT saturation voltage vs current.

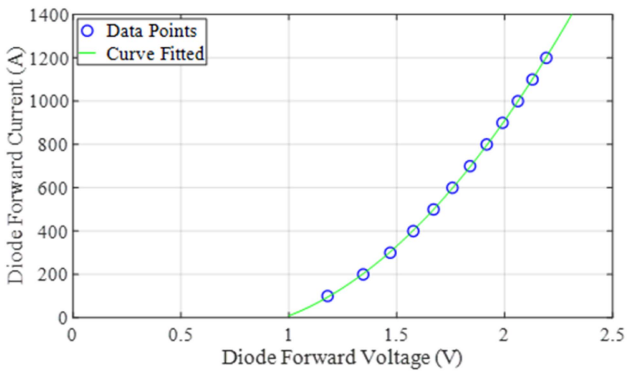

Fig. 17. Measured diode forward voltage vs current.

A single IGBT module suffices. It is mounted on a cold plate cooled by a chiller. The IGBT saturation voltage and conduction loss are recorded over the load current range up to 1200 A with different gate voltages. The freewheeling diode forward voltage drop and power dissipation are evaluated with the high-current power supply cabling reversed and the IGBT gate negatively biased. Figs. 16 and 17 plot the measured voltage drop across the IGBT and diode respectively as a function of load current. As shown in Fig. 16, the increase in IGBT saturation voltage is insignificant when the gate voltage is decreased from 15 V to 12 V. At the full load current of 1200 A and nominal DC system

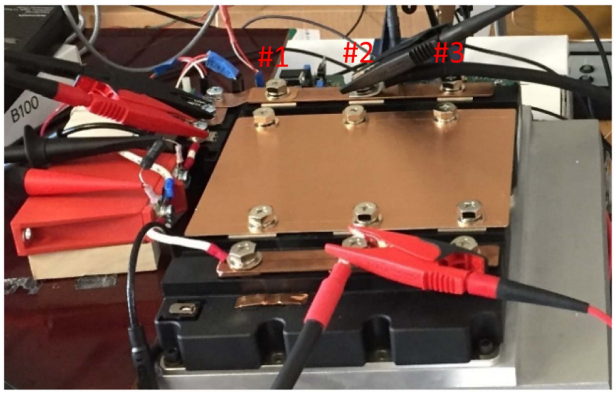

Fig. 18. Narrow emitter busbar.

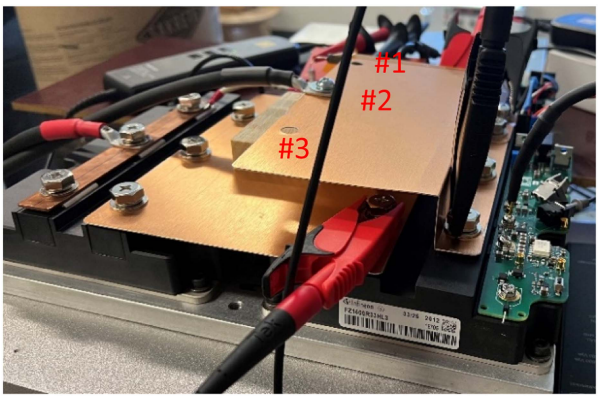

Fig. 19. Wide emitter busbar.

TABLE II
IGBT PEAK SHORT CIRCUIT CURRENT VS EMITTER BUSBAR SHAPE, *WITH* $V_{GE\_ON} = 12$ *V*

Emitter Busbar Shape	Narrow bus bar as in Fig. 18			Wide bus bar as in Fig. 19		
Termination Point	#1	#2	#3	#1	#2	#3
Peak IGBT Current (A) with V_{dc}=1400 V	3922	6169	>7613*	4930	5232	4723
Peak IGBT Current (A) with V_{dc}=1600 V	3980	6365	N/A**	4663	5152	4389
Peak IGBT Current (A) with V_{dc}=2000 V	4204	6148	N/A**	4962	5213	4744

*: current exceeds current sensor measurement range
**: Data point not available due to safety concern.

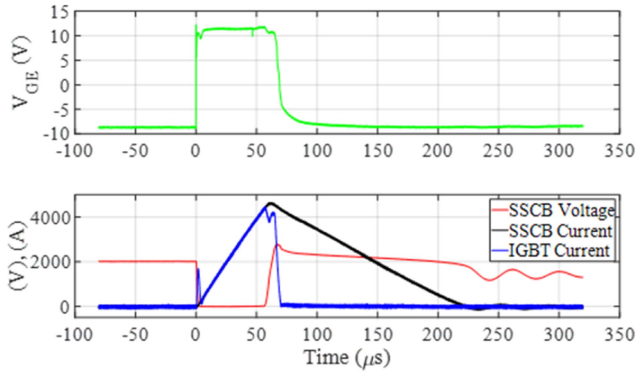

Fig. 20. Switching waveforms, $L_{System} = 25\ \mu H$, $V_{DC} = 2000$ V, $T_{Junction}$ is room temperature.

voltage of 2 kV, the efficiency of the complete SSCB as shown in Fig. 5 is ∼99.5%, considering the conduction losses incurred in two IGBTs and two freewheeling diodes, with the coolant temperature at the cold plate inlet set at 15 °C.

C. Busbar Shape

The busbar shape has a significant impact on the profile of the short-circuit current and its distribution among the IGBT chips. Upon a short-circuit fault, especially when the short-circuit impedance is low, high *di/dt* would result in strong magnetic coupling between the gate loop and power loop inside the multi-chip IGBT module. This can affect not only the internal current distribution among the IGBT chips, but also the total fault current in the external circuit. For the IHM-B IGBT module selected for the SSCB prototype, both the collector and emitter terminals have three termination points. Figs. 18 and 19 show the IGBT emitter busbar as a narrow copper strip and a wide copper plane properly shaped for power cable termination, respectively.

The difference in the short-circuit current profile is summarized in Table II, where the termination points 1, 2 and 3 refer to the IGBT emitter power terminal farthest from, in the middle, and closest to the IGBT module gate terminal, shown in Figs. 18 and 19, respectively. Detailed switching waveforms with minimum short circuit impedance are presented in the next subsection.

It is apparent that if a single power cable is used together with the narrow copper strip as shown in Figs. 18 and 19 for external circuit connection, significantly different current profiles would result depending on which of the three terminals is used for cable termination. With the power cable terminated at position 3, the peak current value almost doubles compared with the case when the power cable is terminated at position 1. A wide copper plane as shown in Fig. 19 eliminates such ambiguity. The peak saturation current is very close to 5 kA.

D. Switching Test Results

The switching performance of the SSCB prototype has been evaluated with the wide emitter busbar under various operating conditions, including different short circuit impedances, different junction temperatures, and different gate drive parameters. As detailed in Section III, reduced gate voltage provides significant advantages in SSCB applications without incurring too high a penalty. For this reason, an on-state gate voltage of 12 V is selected. The test results are presented in this subsection. Figs. 20 and 21 show the SSCB voltage and current waveforms during the interruption of a short circuit developed with a system inductance of 25 μH and DC source voltage of 2000 V when the IGBT junction temperature is at room temperature and 100 °C, respectively. The short circuit is detected and then acted upon by the gate drive's desaturation protection circuit. The system

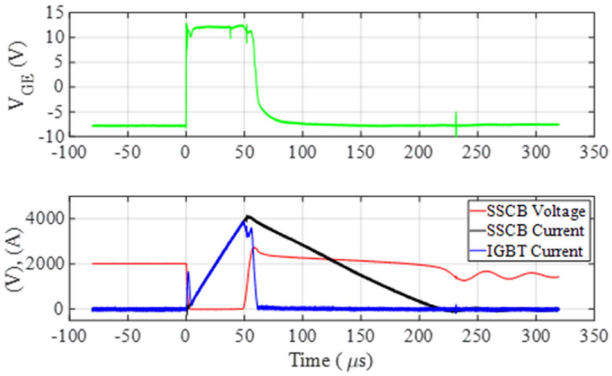

Fig. 21. Switching waveforms, $L_{System} = 25\ \mu H$, $V_{DC} = 2000$ V, $T_{Junction} = 100$ °C.

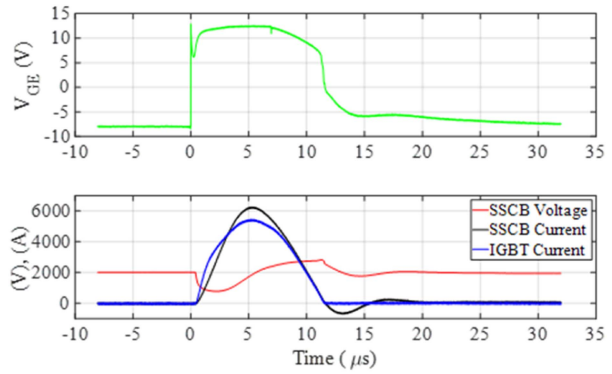

Fig. 22. Switching waveforms, $L_{System} = 0\ \mu H$, $V_{DC} = 2000$ V, $T_{Junction}$ is room temperature.

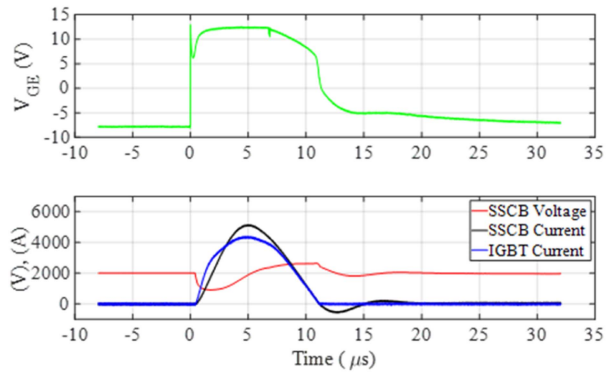

Fig. 23. Switching waveforms, $L_{System} = 0\ \mu H$, $V_{DC} = 2000$ V, $T_{Junction} = 100$ °C.

inductance is sufficiently high, so the fault current is interrupted before the IGBT enters the active region. The IGBT voltage and current trajectories during the short circuit current interruption stay well within its reverse bias safe operating area, thanks to the eMOV as well as properly sized RC snubber. At a higher junction temperature, the short circuit condition is detected sooner, and the fault current peak value is lower.

Figs. 22 and 23 present the SSCB voltage and current waveforms during the interruption of a short circuit developed with minimum system impedance, with the air-core inductor shown in Fig. 12 bypassed. The system inductance is only 300 nH, mainly due to the power cabling. And the parasitic inductance inside SSCB is about 200 nH. Thus, the total inductance limiting the fault current is around 500 nH. As seen in these figures, the IGBT enters the current saturation mode shortly after the fault initiation and before the gate drive circuit detects the fault and responds to turn off the gate. The IGBT voltage stays well above zero during the short circuit. The initial ramping rate of the fault current is contained below 3 kA/μs. And the peak fault current flowing through the IGBT is effectively limited to 5 kA which consequently is interrupted after the protection circuitry is triggered. Such peak fault current is further reduced to 4 kA with higher junction temperature, which is closer to the real case.

VI. Conclusion

The paper proposes a high-density solid-state circuit breaker without current limiting inductor. The proposed SSCB can limit the maximum peak fault current level with reduced IGBT gate voltage, thus achieving a high specific power density for hybrid electric propulsion applications. The carefully chosen gate voltage effectively limits the IGBT saturation current with insignificant efficiency penalty. The impact of the inductor-less design on the SSCB mechanical layout, gate drive control and operational reliability is discussed in depth. Detailed design and analysis of the proposed SSCB are presented.

Both the thermal and switching performances of the proposed SSCB have been experimentally validated. The thermal test confirms that the efficiency penalty due to reduced gate voltage is extremely limited, and the specifications can be satisfied with a sufficient margin. Test results of both normal load current turn-off and short circuit clearing show satisfactory transient performance with switching trajectories well contained in the IGBT module's safe operating area (SOA). The experimental results prove the feasibility and effectiveness of the proposed solution.

References

[1] R. J. C. Bowman and A. Jankovsky, "Sizing power components of an electrically driven tail cone thruster and a range extender," in *Proc. 16th Amer. Inst. Astronaut. Aviation Technol. Integr. Oper. Conf.*, 2016, pp. 1–9.

[2] M. Kempkes, I. Roth, and M. Gaudreau, "Solid-state circuit breakers for medium voltage DC power," in *Proc. IEEE Elect. Ship Technol. Symp.*, 2011, pp. 254–257.

[3] R. Rodrigues, Y. Du, A. Antoniazzi, and P. Cairoli, "A review of solid-state circuit breakers," *IEEE Trans. Power Electron.*, vol. 36, no. 1, pp. 364–377, Jan. 2021.

[4] T. C. Cano et al., "Future of electrical aircraft energy power systems: An architecture review," *IEEE Trans. Transp. Electrific.*, vol. 7, no. 3, pp. 1915–1929, Sep. 2021.

[5] J. Zhu, Q. Zeng, X. Yang, M. Zhou, and T. Wei, "A bidirectional MVDC solid-state circuit breaker based on mixture device," *IEEE Trans. Power Electron.*, vol. 37, no. 10, pp. 11486–11490, Oct. 2022.

[6] M. Yang, X. Wang, W. Sima, T. Yuan, P. Sun, and H. Liu, "Air-core-transformer-based solid-state fault-current limiter for bidirectional HVdc systems," *IEEE Trans. Ind. Electron.*, vol. 69, no. 6, pp. 4914–4925, May 2022.

[7] X. Xu, J. Ye, Y. Wang, X. Xu, Z. Lai, and X. Wei, "Design of a reliable bidirectional solid-state circuit breaker for DC microgrids," *IEEE Trans. Power Electron.*, vol. 37, no. 6, pp. 7200–7208, Jun. 2022.

[8] I. V. Raghavendra, S. N. Banavath, C. N. M. Ajmal, and A. Ray, "Modular bidirectional solid-state DC circuit breaker for next-generation electric aircrafts," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 10, no. 5, pp. 5486–5497, Oct. 2022.

[9] K. Liu, X. Zhang, L. Qi, X. Qu, and G. Tang, "A novel solid-state switch scheme with high voltage utilization efficiency by using modular gapped MOV for DC breakers," *IEEE Trans. Power Electron.*, vol. 37, no. 3, pp. 2502–2507, Mar. 2022.

[10] D. Li and A. Ukil, "Adaptive solid-state circuit breaker without varistors in VSC-interfaced DC system," *IEEE Trans. Ind. Electron.*, vol. 69, no. 5, pp. 4824–4835, May 2022.

[11] X. Xu, W. Chen, C. Liu, R. Sun, Z. Li, and B. Zhang, "An efficient and reliable solid-state circuit breaker based on mixture device," *IEEE Trans. Power Electron.*, vol. 36, no. 9, pp. 9767–9771, Sep. 2021.

[12] U. Mehrotra, B. Ballard, and D. C. Hopkins, "Bidirectional solid-state circuit breaker using super cascode for MV SST and energy storage systems," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 10, no. 4, pp. 3652–3661, Aug. 2022.

[13] R. Kheirollahi et al., "Capacitive couple-based transient current commutation in solid-state circuit breakers," *IEEE Trans. Power Electron.*, vol. 37, no. 5, pp. 4973–4978, May 2022.

[14] X. Xu, W. Chen, H. Tao, Q. Zhou, Z. Li, and B. Zhang, "Design and experimental verification of an efficient SSCB based on CS-MCT," *IEEE Trans. Power Electron.*, vol. 35, no. 11, pp. 11682–11693, Nov. 2020.

[15] R. Kheirollahi, S. Zhao, H. Zhang, and F. Lu, "Fault current bypass-based DC SSCB using TIM-pack switch," *IEEE Trans. Ind. Electron.*, vol. 70, no. 4, pp. 4300–4304, Apr. 2023.

[16] R. Xie and H. Li, "Improved MVDC breaker operation by active fault current sharing (FCS) of existing power converters for shipboard applications," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 9, no. 3, pp. 2620–2631, Jun. 2021.

[17] R. Rodrigues, U. Raheja, Y. Zhang, P. Cairoli, and A. Antoniazzi, "Power loop busbars design and experimental validation of 1 kV, 5 kA solid-state circuit breaker using parallel connected RB-IGCTs," *IEEE Trans. Power Electron.*, vol. 57, no. 3, pp. 1920–1927, May/Jun. 2021.

[18] G. E. Mejia-Ruiz, M. R. A. Paternina, A. Zamora-Mende, J. C. Rosas-Caro, and G. Bolivar-Ortiz, "A novel GaN-based solid-state circuit breaker with voltage overshoot suppression," *IEEE Trans. Ind. Electron.*, vol. 69, no. 9, pp. 8949–8960, Sep. 2022.

[19] Z. Zhou, J. Jiang, S. Ye, C. Liu, and D. Zhang, "A Γ-source circuit breaker for DC microgrid protection," *IEEE Trans. Ind. Electron.*, vol. 68, no. 3, pp. 8949–8960, Mar. 2021.

[20] J. Shu, S. Wang, J. Ma, T. Liu, and Z. He, "An active Z-source DC circuit breaker combined with SCR and IGBT," *IEEE Trans. Power Electron.*, vol. 35, no. 10, pp. 10003–10007, Oct. 2020.

[21] R. Kheirollahi, S. Zhao, H. Zhang, and F. Lu, "Fault current bypass-based DC SSCB using TIM-pack switch," *IEEE Trans. Ind. Electron.*, vol. 70, no. 4, pp. 4300–4304, Apr. 2023.

[22] S. Zhao, R. Kheirollahi, Y. Wang, H. Zhang, and F. Lu, "Implementing symmetrical structure in MOV-RCD snubber-based DC solid-state circuit breakers," *IEEE Trans. Power Electron.*, vol. 37, no. 5, pp. 6051–6061, May 2022.

[23] V. R. I, S. N. Banavath, and S. Thamballa, "Modified Z-source DC circuit breaker with enhanced performance during commissioning and reclosing," *IEEE Trans. Power Electron.*, vol. 37, no. 1, pp. 910–919, Jan. 2022.

[24] Y. Ren, F. Zhang, X. Yang, X. Han, and W. Chen, "Modular DC circuit breaker with master−slave concept for gate driver simplification: Topology and implementation," *IEEE Trans. Ind. Electron.*, vol. 69, no. 9, pp. 8915–8924, Sep. 2022.

[25] J.-Y. Yu, J.-Y. Kim, S.-M. Song, Z. Ayubu, and I.-D. Kim, "New DC solid-state circuit breaker with natural charging operation," *IEEE Trans. Ind. Electron.*, vol. 68, no. 11, pp. 10360–10368, Nov. 2021.

[26] Z. Ayubu, J.-Y. Kim, J.-Y. Yu, S.-M. Song, and I.-D. Kim, "Novel bidirectional DC solid-state circuit breaker with operating duty capability," *IEEE Trans. Ind. Electron.*, vol. 68, no. 10, pp. 9104–9113, Oct. 2021.

[27] A. Giannakis and D. Peftitsis, "Overvoltage suppression scheme for minimized snubber requirements in MVDC solid-state breakers with series-connected IGBTs," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 10, no. 4, pp. 4603–4613, Aug. 2022.

[28] R. S. Chokhawala, J. Catt, and L. Kiraly, "A discussion on IGBT short-circuit behavior and fault protection schemes," *IEEE Trans. Ind. Appl.*, vol. 31, no. 2, pp. 256–263, Mar./Apr. 1995.

[29] S. Mohsenzade, M. Zarghani, and S. Kaboli, "A series stacked IGBT switch to be used as a fault current limiter in HV high-power supplies," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 9, no. 5, pp. 6300–6314, Oct. 2021.

[30] D. Zhang, Y. Xu, J. Brandt, Z. Zhang, D. Qin, and D. Dong, "A solid-state circuit breaker without current limiting inductor," in *Proc. IEEE Energy Convers. Congr. Expo.*, 2022, pp. 1–7.

[31] D. Zhang, J. He, and D. Pan, " A megawatt-scale medium-voltage high efficiency high power density "SiC+Si" hybrid three-level ANPC inverter for aircraft hybrid-electric propulsion systems," *IEEE Trans. Ind. Appl.*, vol. 55, no. 6, pp. 5971–5980, Nov./Dec. 2019.

[32] FZ1500R33HL3 datasheet, Oct. 26, 2021. [Online]. Available: https://www.infineon.com/cms/en/product/power/igbt/igbt-modules/fz1500r33hl3/

[33] S. M. Seyyedbarzegar and M. Mirzaie, "Thermal balance diagram modelling of surge arrester for thermal stability analysis considering ZnO varistor degradation effect," *Inst. Eng. Technol. Gener. Transmiss. Distrib.*, vol. 10, no. 7, pp. 1570–1581, 2016.

[34] J. He, J. Lin, W. Liu, H. Wang, Y. Liao, and S. Li, "Structure-dominated failure of surge arresters by successive impulses," *IEEE Trans. Power Del.*, vol. 32, no. 4, pp. 1907–1914, Aug. 2017.

[35] Z. Topcagic, M. Mlakar, and T. E. Tsovilis, "Electrothermal and overload performance of metal-oxide varistors," *IEEE Trans. Power Del.*, vol. 35, no. 3, pp. 1180–1188, Jun. 2020.

[36] Y. Xu, R. Burgos, and D. Boroyevich, "Insulation design and evaluation via partial discharge (PD) test for power electronics application," in *Proc. IEEE Elect. Ship Technol. Symp.*, 2017, pp. 394–400.

[37] Z. Yuan et al., "Insulation and switching performance optimization for partial-discharge-free laminated busbar in more-electric aircraft applications," *IEEE Trans. Power Electron.*, vol. 37, no. 6, pp. 6831–6843, Jun. 2022.

[38] S. Lefebvre, Z. Khatir, and F. Saint-Eve, "Experimental behavior of single-chip IGBT and COOLMOS devices under repetitive short-circuit conditions," *IEEE Trans. Electron. Devices*, vol. 52, no. 2, pp. 276–283, Feb. 2005.

[39] Infineon Technologies, "Application and mounting instructions for IHM and IHV modules," Application Note 2014-12 V1.1, Dec. 2014.

[40] D. Qin et al., "Analysis and suppression of voltage oscillation of solid-state circuit breaker entering active region," in *Proc. IEEE Energy Convers. Congr. Expo.*, 2022, pp. 1–5.

[41] L. Ravi, D. Zhang, D. Qin, Z. Zhang, Y. Xu, and D. Dong, "Electronic MOV-based voltage clamping circuit for DC solid-state circuit breaker applications," *IEEE Trans. Power Electron.*, vol. 37, no. 7, pp. 7261–7565, Jul. 2022.