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Assessing the vulnerability of solar inverters to EMPs: Port testing, PCI modeling, and protection strategies

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ABSTRACT

Renewable energy sources are becoming an ever-larger contributor to the power grid. These renewable energy sources depend upon the power electronic devices, specifically inverters, being essential for connecting Photovoltaic (PV) generation to the grid. However, the Electromagnetic Pulses (EMPs) caused by the high-altitude nuclear explosions can generate fast broad-band pulses with nanosecond rise time, potentially causing damage or destruction to electronic components. To assess the vulnerability of PV inverters to high-altitude EMPs, the port testing and Pulsed Current Injection (PCI) modeling schemes are proposed based on the port impedance analysis. Wide-band frequency measurements are achieved by fusing impedance results from three vector network analyzers. Then, a PCI model is used to simulate the induced response to EMP, with two typical immunity levels of EC5 and EC8 tested. The experiment successfully excites the induced voltage and current under EMP, where the voltage and current can reach 1500V/40A and 8000V/150Aunder EC5 andEC8, respectively. The port vulnerability analysis results demonstrate that only some ports can survive under EC5. To defend against the impact of EMP, three protection strategies are discussed.

1. Introduction

To enhance the sustainability of the energy sector, many countries have proposed road maps to increase the proportion of renewable energy sources [1]. For example, the United Arab Emirates aims to achieve 50% renewable energy sources by 2050 [2], with solar and wind power being the two primary sources. However, the electricity infrastructure of the power system, such as the transformers, transmission lines, and controllers, would be significantly impacted and even damaged by an Electromagnetic Pulse (EMP) [3]. Solar inverters, as one of the critical devices responsible for converting the generators' Direct Current (DC) to the power grids' Alternating Current (AC), have been widely used in Photovoltaic (PV) systems [4,5]. The PV panels, cables, as well as solar inverters of PV farms, and rooftop PV systems, are at risk of exposure to EMP without sufficient shielding, and therefore, they can be easily disturbed. It is necessary to conduct a vulnerability analysis of critical devices.

The EMP is a high-intensity burst of energy that emits a strong electromagnetic field [6]. It is usually caused by natural sources such as Geomagnetic Disturbance (GMD) or man-made sources such as the microwave generator, an explosively pumped flux compression generator, and high-altitude nuclear detonation (called High Altitude Electromagnetic Pulse or HEMP), and solar corona mass ejections [7,8].

The HEMP consists of three stages named E1, E2, and E3 [9]. The E1 is the beginning of the explosion and varies quickly in hundreds of nanoseconds. The energy of E1 (field strengths may reach tens of kilovolts/meter) is much higher than E2 and E3, it also has the greatest impact on the grid. E1 can reach its peaking energy of 50 kV/m after approximately 2.56 ns [10]. The next stage, E2, has similarities to lightning strikes which peak at about 100 V/m and last for milliseconds [10], and it may cause an induced current that exceeds the maximum tolerance of electric equipment. The primary difference between E1 and E2 is the energy burst capability. For example, the lightning impulse current should be at 8/20 μs and 10/350 μs with about 20 kA peak current according to the standard IEC 62305 [11] and some IEEE standards [12]. E3 is similar to GMD, it can last several minutes and has a field value near 10's volts per km [9,13]. Additionally, the failing inverters themselves may belong to the equipment level, whereas the EMP belongs to the system level and has a wider range of influence. To investigate the equipment vulnerability to the most potentially damaging stage of EMP, E1 is selected as the objective of this research.

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Nomenclature

Acronyms

AC	Alternating Current
DC	Direct Current
DUT	Device Under Test
EMP	Electromagnetic Pulse
FDTD	Finite-Difference Time Domain
GMD	Geomagnetic Disturbance
GTEM	Gigahertz Transverse Electromagnetic Simulator
HEMP	High Altitude Electromagnetic Pulse
IEC	International Electrotechnical Commission
IFT	Inverse Fourier Transform
LCR	Inductance Capacitance Resistance
PCI	Pulsed Current Injection
PV	Photovoltaic
VNA	Vector Network Analyzers

Variables

Z_K	Measured impedance
$\varphi_{k,Zdut}$	Measured phase
$Z_{dut}(\omega)$	Impedance of DUT
$Z_c(\omega_k)$	Impedance of capacitor
$Z_L(\omega_k)$	Impedance of inductor
U_{dut}	Voltage in the frequency domain
I_{dut}	Current in the frequency domain
F_s	Sampling frequency

The EMP can damage the devices through direct illumination by the strong electric field or by the induced surge current through exposed conductors such as cables and ports [14]. In 1962, the United States tested a nuclear detonation above the South Pacific Ocean. Even at 400 km altitude, this detonation (Starfish Prime) affected infrastructure in Hawaii, where streetlights almost 1500 km from the detonation lost power. Additionally, the GMD from two strong solar storms lasting 19 h caused a power disruption in Sweden in 2003 [15]. That event demonstrates that even for a lower magnetic field, the power system can be affected. Therefore, it is critical to identify the points of vulnerability coupling from the damaging EMP-induced signals.

To investigate the effects of EMP, various simulation and experimental schemes have been studied. In [16], open-source software has been designed to analyze the impacts of both GMD and E3 from HEMP events on the power grid. Similarly, Sandia National Laboratories has developed a Monte-Carlo-Simulation-based methodology to quantify the transient response of the power grid [17] and a transformer model to capture the input and output response of the high-voltage transformers to an HEMP event [18]. Additionally, the Gigahertz Transverse Electromagnetic Simulator (GTEM) platform has been established by the Sandia National Laboratories, which can be used to measure equipment susceptibility, radiated emissions, and operation across a wide frequency range (DC to GHz) [14]. However, constructing this experimental equipment is quite problematic due to its high cost.

Apart from the aforementioned technologies, simulation methods provide insight into the distribution of the electromagnetic field and response analysis. For instance, the Finite-Difference Time Domain (FDTD) is proposed to calculate the EMP propagation and stroke current distribution [19]. To test the over-voltages of the large-scale PV power plants caused by lightning, a reduced 1:10 scale model is established and verified using the FDTD analysis [20]. However, using FDTD to model EMP-cable coupling would be time-consuming. Instead, a hybrid Electromagnetic (EM) numerical method is proposed in [21] to accelerate the calculation by implementing the transfer functions. A 3D semi-analytical method is also proposed to model the DC/DC converter and calculate the induced transient response due to the lightning strike [22]. However, the voltage levels of lightning are lower than the E1 HEMP.

To accurately assess the impact of EMP, the Pulsed Current Injection (PCI) setup is derived for immunity testing caused by lightning, HEMP, switching operations, etc. It is an effective technique to test the vulnerability of different electronic devices to HEMP [23]. In [24], a PCI test setup is developed to reproduce intense transient electromagnetic disturbances. The PCI achieves accurate detection of problems with critical cables by using the charge/discharge capacitors and injection probes. Based on the MIL-STD-461G test program, a DC to AC inverter is tested using radiated test methods, where the Device Under Test (DUT) is completely immersed under the electromagnetic environment [25]. Compared with the radiated test method, the PCI tests can be more attractive in terms of cost and convenience. Although some research has been conducted on the effects of EMP on PV panels, the vulnerability analysis of solar inverters still needs to be further explored.

To explore the impact of EMP on critical devices in the power system, a port vulnerability analysis scheme is proposed and tested on solar inverters. Compared to the previous research [3], there are two differences and two improvements. Two primary differences are the objective difference and the impedance measurement model. The objective of this research is solar inverters which a necessary equipment in renewable energy systems, where the Ref. [3] is programmable logic controllers. Besides, only the common model is tested in [3] where both the common model and differential model are tested in this research. The impedance measurement demonstrates that the impedance and phase results are more diverse where the impedance pattern is single in Figure 12 of [3]. Importantly, two steps in aspects of vulnerability analysis and protection measures are further carried out to assess the vulnerability of solar inverters, where the [3] are not discussed.

The contributions of this paper are as follows,

1. A port impedance testing method is implemented using three different Vector Network Analyzers (VNAs) to achieve a wide frequency range measurement and overcome the board-band effects of EMP.
2. Based on the tested impedance, a pulsed current injection model is established to simulate the inducted response of the solar inverters. The port vulnerability is evaluated through its spectrum and cumulative energy, and the advantage of the PCI model is that it can quickly analyze the transient response.
3. Finally, the proposed method and port vulnerability are verified by testing three different solar inverters under two immunity levels, EC5 and EC8. The experimental results reveal the port vulnerability.

The rest of the paper is organized as below. Section 2 introduces the proposed framework. Section 3 presents the details of the PCI model. Then Section 4 describes the tested inverters. The experiments of the impedance and inducted transient response are shown in Section 5. Finally, conclusions are drawn in Section 6.

2. Impedance testing platform

2.1. Discussion of inverter in the grid

Inverters are widely used in PV, electric vehicle chargers, and energy storage units. They can be designed with a similar topology [26]. This means they will have similar modules and circuits inside. Here, the solar inverters are discussed in detail. It is worth mentioning that the proposed measurement, calculation, and response analysis are also

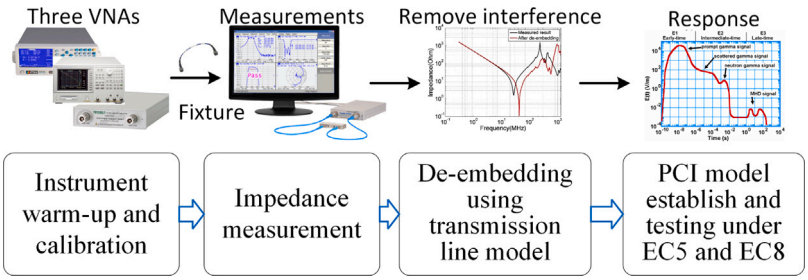

Fig. 1. Framework of the port vulnerability analysis scheme.

suitable for the inverters of other scenarios. The solar inverter is an electrical converter that transforms the DC generated by the PV panel into AC by utilizing an H-bridge topology and pulse width modulated wave controller [27]. Detecting the vulnerability of the inverters is critical for applying protective measures against EMP damage.

To this end, the repetitive fast transient test can demonstrate the immunity of electronic equipment due to its low cost, convenience, and security features. To construct a complete PCI model, the load impedance of the DUT across different frequency ranges is necessary to implement the circuit diagram. Yet, the limited measurement range of VNAs can cause output response disturbance during the PCI test.

2.2. Testing platform and de-embedding

To explore the PCI response of the solar inverters, the impedance, and phase are measured [28]. The proposed impedance measurement and PCI testing scheme are presented in Fig. 1.

Two vector network analyzers are used (the Planar TR1300/1 and HP 4395A) and one inductance capacitance resistance (LCR) meter is used (MCR-5200). Here, the LCR meter is denoted as a VNA for convenience. The motivation for using three VNAs is that each device only covers a limited frequency band. Using three VNAs for a wider frequency band gives a complete impedance result. For example, the frequency range of Planar TR1300/1 mainly focuses on the high-frequency located between 300 kHz and 1.3 GHz. The HP 4395A can measure the impedance between 10 Hz to 500 MHz but it has a maximum magnitude limit (no more than 10^4 Ω). The MCR-5200 would provide a low-frequency band ranging from 40 Hz to 200 kHz, where the maximum magnitude can reach 99.99 MΩ. Therefore, the theoretical frequency range can cover from 10 Hz to 1.3 GHz while the maximum magnitude can reach 99.99 MΩ.

As can be seen from Fig. 1, the impedance measurement scheme contains four steps:

1. First, the VNAs need to be warmed up and then calibrated using the N1.2 Calibration Kit.
2. Then inverters should be connected with VNAs using the fixture. Different ports of the solar inverters are tested including the common model and wire-to-ground interfaces.
3. The de-embedding is performed to remove the influence of the fixture, where the fixture is modeled using the transmission line model. Then the parameters of the transmission line structure will be derived using the open-short and short-open methods.
4. PCI model is established to simulate the induced voltage and current of EMP, where two immunity levels are tested under EC5 and EC8.

2.3. Standard introduction for PCI modeling

To protect against the EMP impacts, the International Electrotechnical Commission (IEC) has published various standards to evaluate and test the defensive capabilities. IEC 6100-4-18, and IEC 61000-4-25 are the primary standards where 12 immunity test levels EC1 to ECX are provided [29,30]. The voltage and current levels range from 100 V to 160 kV, and 1 A to 3200 A, respectively. Considering that the EC1 to EC5 is the damped sinusoidal waveform, and EC7 to ECX belong to the electrical fast transient, two immunity test levels (EC5 and EC8) are selected as the tested levels. The detailed parameters are listed in Table 1 and the damped sinusoidal contains two frequencies: 1 MHz and 10 MHz.

Table 1
Early time conducted immunity test levels EC5 and EC8.

Immunity test level	Vol. (V)	Cur. (A)	Waveform
EC5	2000	20	Damped sinusoids
EC8	8000	160	5/50 ns

3. PCI modeling of solar inverters

3.1. Structure of the PCI model

The open voltages of EC5 and EC8 levels are 2000 V and 8000 V, respectively. The simplified circuit diagrams of PCI are demonstrated in Figs. 2 and 3.

The circuit in the dashed box represents the pulsed current generator. Capacitor C_0 is pre-charged. Then, the gap switch is triggered to generate pulsed voltage and current. The output of the generator is connected to the DUT through a 50 Ω coaxial cable. Z_{dut} represents the port impedance of DUT. For simplicity, the length of the coaxial cable connecting the generator and DUT has been set to 0.2 m, as illustrated in Fig. 2. Minor adjustments are needed to ensure consistent output waveform if the influence of cable is considered.

The primary parameters are demonstrated to ensure that the output waveform applied to DUT meets the requirements of the IEC standard. For EC5, an example of the waveform of the damped oscillatory wave is shown in Fig. 4(a). The performance characteristics of the generator are listed in Table 2.

For EC8, a single pulse with a rise time of $t_r = 5$ ns and pulse width of $t_w = 50$ ns is considered, as illustrated in Fig. 4(b). The generator's performance characteristics are listed in Table 3. It is important to note that the measured output voltage with a 50 Ω load is 0.5 times the open-circuit voltage.

3.2. Result analysis in PCI circuit

The voltage is applied to the load once the gap switch is closed, and there exists voltage and current responses. A frequency based method is carried out to calculate the induced response. The basic process is to use discrete calculation in the frequency domain, and then the results are converted to the time domain. In this research, the frequency range starts from 50 Hz to 1.3 GHz, and a total of 500,000 tested points are generated by using interpolation technology.

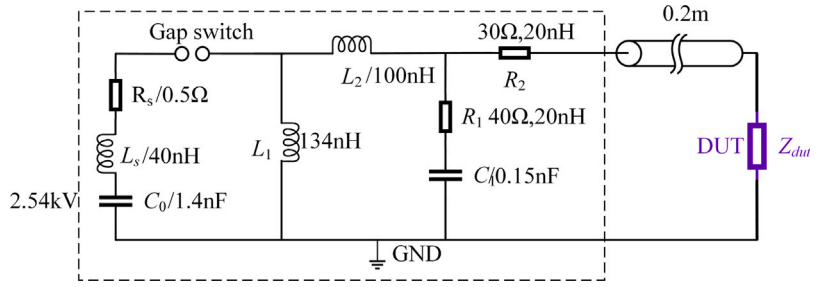

Fig. 2. The circuit diagram of the PCI model for EC5 level.

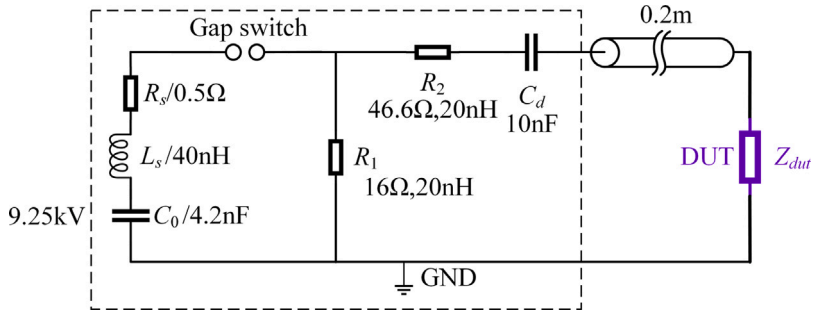

Fig. 3. The circuit diagram of the PCI model for EC8 level.

Table 2
Performance characteristics of generator for EC5 level.

Parameters of the damped oscillatory	Voltage (V)	Current (A)
Rise time (T_1)	5 ns ± 30%	3 MHz :< 330 ns, 10 MHz :< 100 ns, 30 MHz :< 33 ns
Oscillation (MHz)	(3, 10 and 30) ± 10%	(3, 10 and 30) ± 30%
Decaying (T_2)	$Pk_5 > 50\%\ of\ Pk_1, Pk_{10} < 50\%\ of\ Pk1$	$Pk_5 > 25\%\ of\ Pk_1, Pk_{10} < 25\%\ of\ Pk1$
Amplitude (V or A)	2000 ± 10%	40 ± 20%

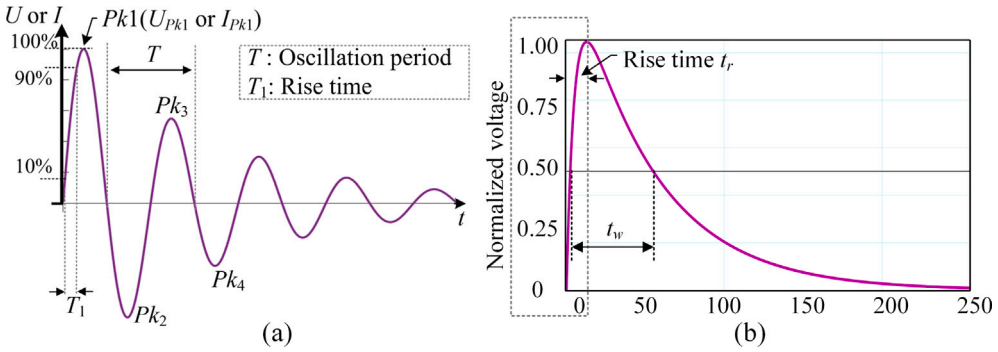

Fig. 4. (a) Example of the waveform of the damped oscillatory wave, (b) Ideal waveform of a single pulse with nominal parameters t_r = 5 ns and t_w = 50 ns.

Table 3
Performance characteristics of generator for EC8 level.

	Rise time t_r (ns)	Pulse width t_w (ns)	Peak voltage (kV)
Into 50 Ω load	(5 ± 1.5)	(50 ± 15)	4 ± 20%
Into 1000 Ω load	(5 ± 1.5)	50 with a tolerance of − 15 to+100	7.6 ± 20%

Given the measured impedance and phase after interpolation as Z_k and $\phi_{k,Z_{dut}}$, the impedance of the DUT can be expressed as

$$Z_{dut}(\omega) = \sum_{k=1}^{n} |Z_k| e^{j\phi_{k,Z_{dut}}} \tag{1}$$

Then the impedance of the capacitor and inductor in the designed circuit can be calculated as

$$\begin{aligned} Z_c(\omega_k) &= 1/j\omega_k C \\ Z_L(\omega_k) &= j\omega_k L \end{aligned} \tag{2}$$

where ω_k denotes the angular frequency and it follows

$$\omega_k = 2\pi f_k \tag{3}$$

where C and L are the capacitance and inductance, respectively. With the known impedance of each branch circuit and applied voltage, the voltage and current response on Z_{dut} can be obtained using frequency

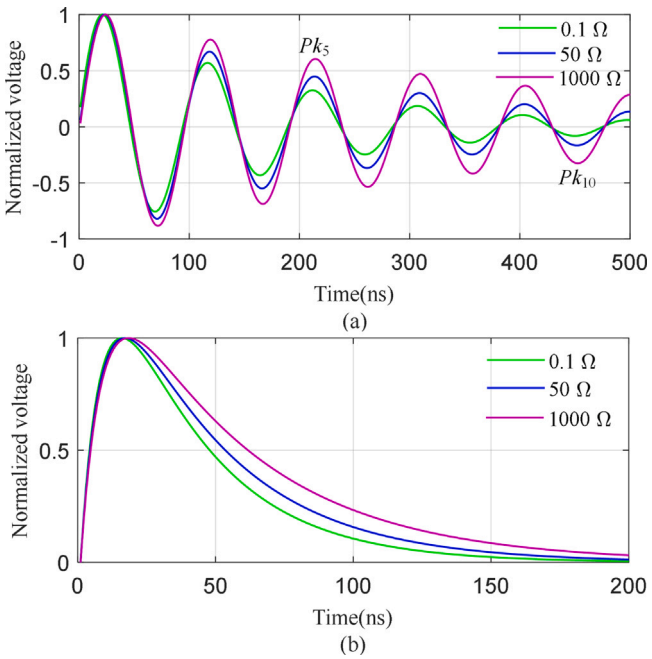

Fig. 5. Normalized output voltage waveforms of the generator, (a) EC5 level, (b) EC8 level.

components as follows

$$\begin{cases} U_{dut}(\omega) = \sum_{k=1}^{n} |U_k| e^{\phi_{k,U}} \\ I_{dut}(\omega) = \sum_{k=1}^{n} |I_k| e^{\phi_{k,I}} \\ |I_k| e^{\phi_{k,I}} = \frac{|U_k| e^{\phi_{k,U}}}{|Z_k| e^{\phi_k}} \end{cases} \tag{4}$$

where U_{dut} and I_{dut} are the expression of voltage and current in the frequency domain. The corresponding time domain waveform can be obtained by Inverse Fourier Transform (IFT) of them, which can be calculated as

$$\begin{cases} U_{dut}(t) = \frac{2F_s}{n} \sum_{k=1}^{n} |U_k| \cos\left(\omega_k + \phi_{k,U}\right) \\ I_{dut}(t) = \frac{2F_s}{n} \sum_{k=1}^{n} |I_k| \cos\left(\omega_k + \phi_{k,I}\right) \end{cases} \tag{5}$$

where F_s is the sampling frequency, namely the upper limit frequency of 1.3 GHz; $\frac{2F_s|U_k|}{n}$ and $\frac{2F_s|I_k|}{n}$ denote the voltage and current magnitude of kth component in the frequency domain, respectively, which forms the frequency spectrum, $\phi_{k,U}$ and $\phi_{k,I}$ are the related phase angle.

Usually, 0.1 Ω, 50 Ω, and 1000 Ω loads are used to check if the output of the generator meets the requirements. To verify the output response of the generator, the voltage is calculated under different load impedance.

For the EC5 level, there are three oscillation frequencies including 3 MHz, 10 MHz, and 30 MHz. The 10 MHz waveform is illustrated and the normalized waveforms are shown in Fig. 5(a) for a typical load of 0.1 Ω, 50 Ω, and 1000 Ω. With the main capacitor charged to 2.54 kV, the short current is 20 A and the open voltage is 2000 V.

Similarly, normalized waveforms of the EC8 level are given in Fig. 5(b) for a typical load of 0.1 Ω, 50 Ω, and 1000 Ω. With the main capacitor charged to 9.25 kV, the short current is 160 A and the open voltage is 8 kV.

3.3. Uncertainty analysis

As measurement and calculation are both conducted in this paper, uncertainty analysis is important before the presentation of the results. Uncertainty may come from both measurement and calculation processes. Impedance measurement accuracy relates to impedance amplitude and frequency. Large and small impedance is more difficult to measure accurately. For the amplitude and frequency range mainly considered (several Ω to kΩ levels, 100 kHz to 100 MHz range) in this paper, accuracy is about 5% seen from the user's manual of the instrument.

Uncertainty in the calculation process can be analyzed by comparing calculated results with simulated ones in ATP-EMTP software. The same circuit with Fig. 3 and typical 0.1 Ω, 50 Ω, and 1000 Ω loads are used. The simulation timestep is set to as small as 0.001 ns and results therefore can be treated as accurate ones. The average difference of waveform parameters between calculated and simulated results is only 0.2%. The maximum difference is less than 1%, occurring in the rise time of 1000 Ω load.

In general, the total uncertainty considering measurement and calculation is less than 6%.

3.4. Vulnerability evaluation

To evaluate the results of the PCI model, the spectrum and cumulative energy of voltage and current are calculated. Denoted the simulated voltage as U_{dut}, the cumulative energy can be expressed as

$$E_{pci} = \frac{\sum \left[(2F_s/(n|U_{dut}|))^2\right]}{max(\sum \left[(2F_s/(n|U_{dut}|))^2\right])} \tag{6}$$

The current has a similar form as Eq. (6). Besides, based on the exponential pulse based waveform defined in [29], the frequency-domain spectral magnitude can be obtained.

4. Solar inverters introduction

To investigate the effect of EMP on inverters, the tested solar inverters in the grid-connected PV power system and three different types of solar inverters are selected, as presented in Fig. 6. To protect the inverter, surge protection such as surge arresters, surge-protective devices, and capacitors might be installed in the enclosures for a specific duty according to the NEC 2017 [31].

Usually, the induced current can be easily coupled into the devices from the lines and ports. Therefore, the following ports can be tested, including the DC input, AC output, power source, and network ports.

An example of the tested impedance and phase using three VNAs is demonstrated in Fig. 7. It can be seen that the results of the Planna TR1300/1 are in line with the HP 4395A. However, when the frequency is lower than 10 kHz, the results of the HP 4395A is tended to be the noise, especially for the phase because the measurements have exceeded the range. To make up for this defect, the LCR meter has good linearity and its result is consistent with the HP-4395A when the frequency ranges from 10 kHz to 200 kHz. The fusion curve indicates that the final measurement can defend against the inaccurate low frequency for HP-4395A and it can also cover both the low and high-frequency bands. It is worth emphasizing that the proposed technique can also be used to study other devices.

5. Experiments

Based on the aforementioned solar inverters, the DC input, AC output, power source, and network ports are tested. To compare the performance among three inverters, where they are named D_1, D_2, and D_3, similar ports will be tested as listed in Table 4. Meanwhile, considering that there are various connections between the ports, the unique impedance results under EC5 and EC8 will be listed in this research.

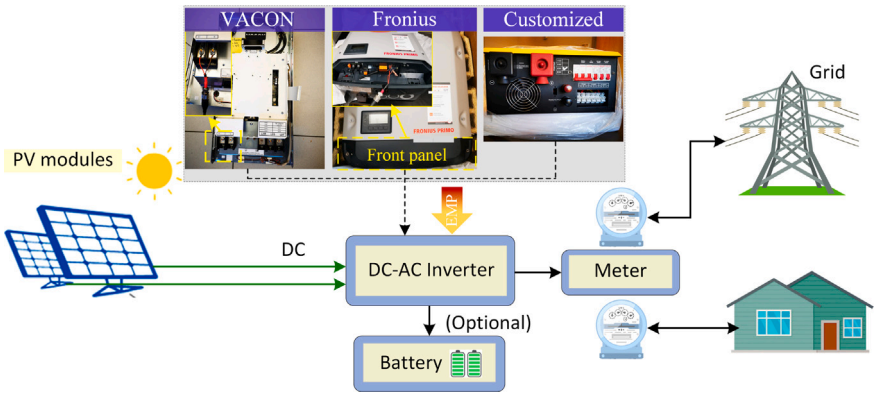

Fig. 6. Tested solar inverters in the grid-connected PV power system.

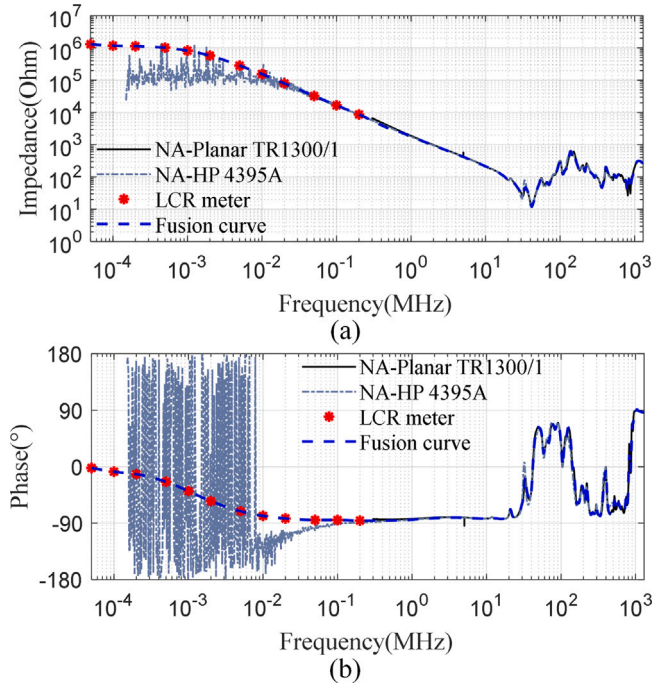

Fig. 7. Tested example of the third inverter (self-made) for DC input port using three different VNAs, (a) magnitude of the impedance, (b) phase.

Table 4
The tested ports of the inverters.

Inverter number	Tested ports		
	DC input	AC input	Power source
D_1 (VACON)	B+-B−	L1-GND	DC+-DC−
D_2 (Fronius)	DC-GND	L1-GND	Green-Blue (Network)
D_3 (Self-made)	DC-GND	L2-N	DC-GND

5.1. Response of PCI modeling for solar inverters

For the solar inverter D_1 as depicted in Fig. 6(a), the impedance and phase results are demonstrated in Fig. 8(a) and (d). It can be seen that the impedance and phase are totally different from each other. The input ports tend to be the capacitive impedance when the frequency is lower than 30 MHz because the phase is lower than 0°. The impedance appears to be decreased with increasing frequency. The maximum impedance of the input port reaches 1×10^6 Ω in the low-frequency band, indicating an open circuit condition. One of the reasons might be because there is capacitance deployed into the input port to maintain the DC voltage stability and eliminate ripple.

Surprisingly, the impedance of the output AC port changes drastically and there are many resonance points, such as the point located as the frequency 300 Hz. For the power source port, the impedance is lower than 1 Ω when the frequency is lower than 0.1 MHz. Then the impedance changes from capacitive to inductive resistance since the phase changes from negative to positive. The majority of the impedance is pretty lower indicating that it will have a higher electromagnetically induced current under HEMP.

The tested impedance and phase results of the solar inverter D_2 are depicted in Fig. 8(b) and (e). It is apparent from the input DC and output AC that the impedance and phase results are similar. The primary difference is that the input DC contains three resonance points, indicating that the induced voltage and current can easily overshoot under EMP. With a frequency lower than 10 kHz, these two ports show a capacitive state, indicating it is an open circuit. Conversely, the network port is extremely stable because the impedance is a fixed value near 1×10^2 Ω and the phase is 0°.

Fig. 8(c) and (f) illustrate the impedance and phase of the inverter D_3. As can be seen from Fig. 8(c), the impedance of the output AC and power source decrease to a lower level from $1{\times}10^6$ Ω and $1{\times}10^4$ Ω to 1 Ω and 0.1 Ω. The phase results reveal the pure capacitive characteristics because the phase is −90°. The input DC has a lower impedance and most of the frequency range belongs to the inductive reactance. Overall, compared with the three inverters, only the output port of the inverters D_2 and D_3 obtain the similarly tested impedance. The other ports have different modes.

5.2. Response of PCI modeling for solar inverters under EC5

Thereafter, the results of the PCI tests are conducted to verify their immunity levels. The voltage and current results of the inverter D_1 under EC5 are demonstrated in Fig. 9(a) and (d). From Fig. 9, the voltage and current are attenuated changes as a sinusoidal waveform. The output and power source ports obtain similar voltage and current profiles. The maximum voltage and current values are higher than 1000 V and 20 A, respectively. Additionally, the input DC obtains the highest voltage and lowest current because its impedance is the highest as observed in Fig. 8.

The PCI-tested results under EC5 for the inverter D_2 are presented in Fig. 9(b) and (d). Surprisingly, the output AC and network ports have almost the same response curves. The maximum voltage and current are 1500 V and 16 A, respectively. However, the input AC has a higher current (more than 20 A) because the transient performance is drastic if the circuits have more resonance points.

For the inverter D_3, the induced voltage and current of EC5 are demonstrated in Fig. 9(e) and (f). It shows that the power source, as well as the output AC, obtain an extremely lower voltage. The

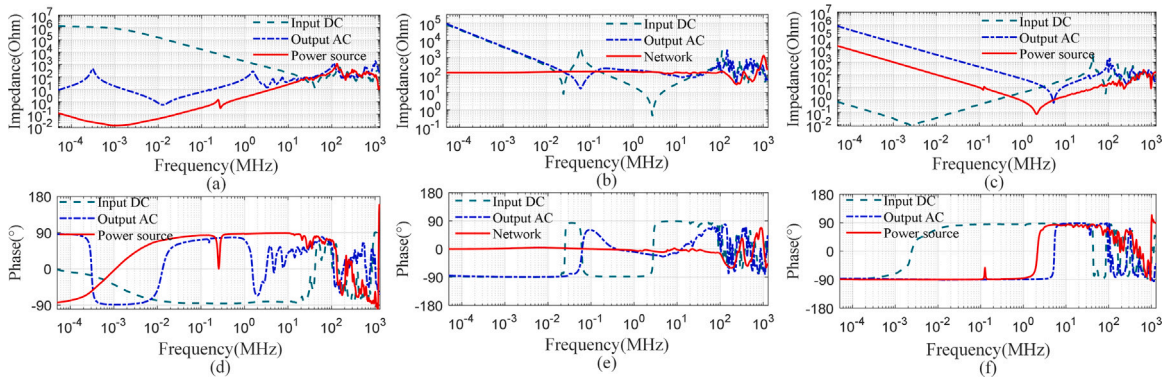

Fig. 8. (a) and (d) are the tested results of the inverter D_1; (b) and (e) are the tested results of the second inverter D_2; (b) and (e) are the tested results of the third inverter D_3; (a)–(c) are the magnitude of the impedance, (d)–(f) are the phase.

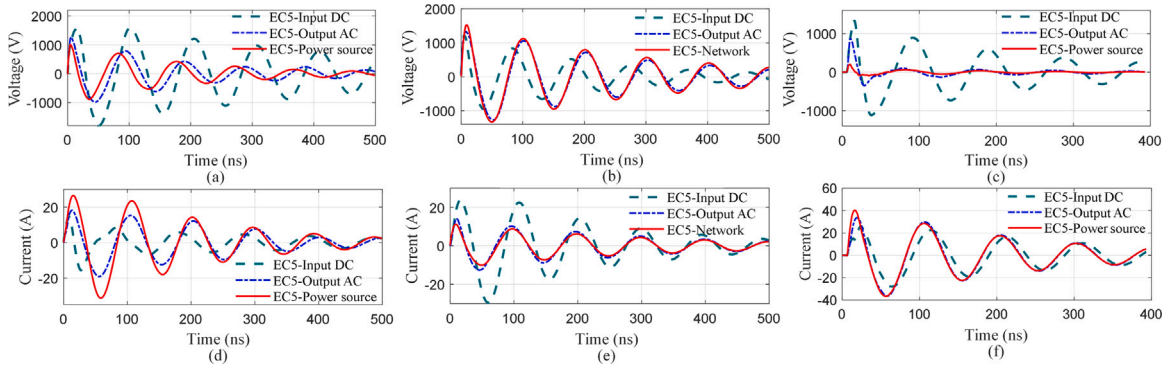

Fig. 9. (a) and (d) are the induced voltage and current of EC5 for inverter D_1; (b) and (e) are the induced voltage and current of EC5 for inverter D_2; (b) and (e) are the induced voltage and current of EC5 for inverter D_3.

main reason is that the small capacitive impedance cannot store much energy. Meanwhile, the maximum current is 40 A which is lower than the inverter D_2. At this stage, the input DC port has a similar response to the above two inverters.

The majority of all the aforementioned responses under EC5 indicates a similar sinusoidal waveform. The magnitude levels of the PCI testes are different which depends on the measured impedance.

5.3. Response of PCI modeling for solar inverters under EC8

Different from the EC5, the EC8 has a higher immunity level. For the inverter D_1, as shown in Fig. 10(a) and (d), the voltage quickly rises to the maximum and then decays slowly. The rise time is slower than 10 ns and the decay time may last for hundreds of nanoseconds. The maximum voltages of the three ports are 4500 V, 5000 V, and 7800 V, respectively. Both the voltage and current levels observed in this investigation are far higher than (4 to 5 times) those observed under EC5.

Besides, there were also differences in the ratios of the slope change, as shown in Fig. 9(d), it takes nearly 50 ns to change from the minimum value to the maximum value whereas it only takes 20 ns in Fig. 10(d). These findings revealed that higher protection levels need to be considered to defend the effect of HEMP.

For the inverter D_2 under EC8, in Fig. 10(b), a 6000 V/10 ns voltage rate is generated. This value is much higher than the EC5 and also 500 V higher than Fig. 10(a). The results show that a higher protection level is required for the inverter D_2. Similarly, the voltage is slowly damped and the voltage of the output DC and network tends to be 0 after 200 ns.

The induced voltage and current of EC8 for the inverter D_3 are demonstrated in Fig. 10(c) and (f). Only a small induced voltage occurs for the power source port but with an induced current higher than 150 A, which is the highest among all the inverters. For the inverter D_3, the induced voltage shown in Fig. 10(c) has three obvious immunity levels including 800 V, 3800 V, and 5000 V. The PCI results under EC8 indicate that the most vulnerable interface needs to be considered to defend the EMP. The ports of the inverter D_3 can survive if a lower rise time is designed such as 5 ns or be damaged if a lower voltage limit is designed such as 1 kV.

Different from EC8, EC5 will last for more than 500 ns while EC8 only lasts for 150 ns. The main reason is that its oscillating form makes the energy not easily damped out. Overall, the voltage and current under EC8 can be higher and damaged whereas EC5 shows a lower magnitude level with a slower decay rate.

5.4. Port vulnerability analysis

To investigate the port vulnerability frequency, the cumulative energy and spectrum are calculated, as demonstrated in Figs. 11 and 12. As illustrated in Fig. 11, the cumulative energy of the induced voltage and current are concentrated at 10 MHz, where the peak spectrum has the same phenomenon. The primary reason is that the EC5 consists of the 10 MHz damped oscillation wave.

Conversely, it can be found from Fig. 12 that the frequency range of primary energy is widely distributed from 0.1 MHz to 100 MHz. Meanwhile, the spectrum contains rich components because the burst electromagnetic pulse is composed of multiple consecutive frequencies, indicating it is challenging to defend the EMP with EC8.

Next, to show what exactly the voltage level that the inverter can withstand, the rated voltage and current of the two inverters, as well as the fast transient burst are listed in Table 5.

The designation of the inverters fulfills the immunity requirements based on the IEC 61800-3, IEC/EN 60947-3, and IEC 62109-1 [32,33].

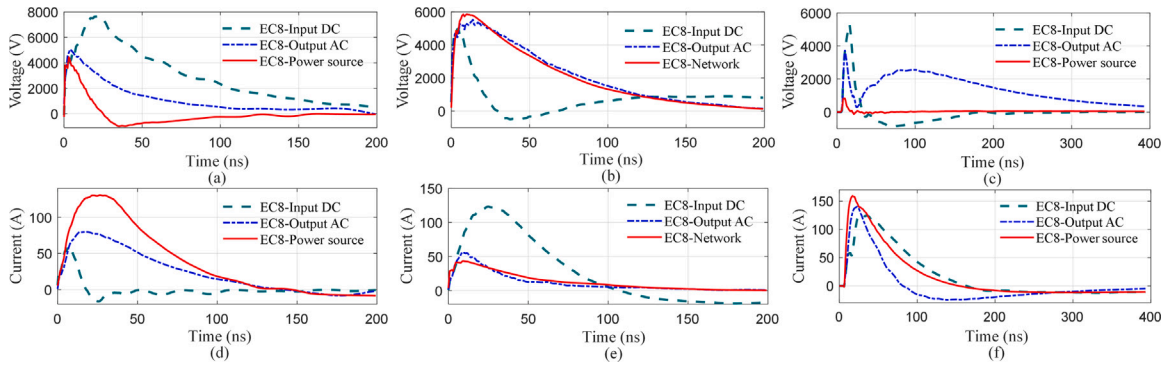

Fig. 10. (a) and (d) are the induced voltage and current of EC8 for inverter D_1; (b) and (e) are the induced voltage and current of EC8 for inverter D_2; (b) and (e) are the induced voltage and current of EC8 for inverter D_3.

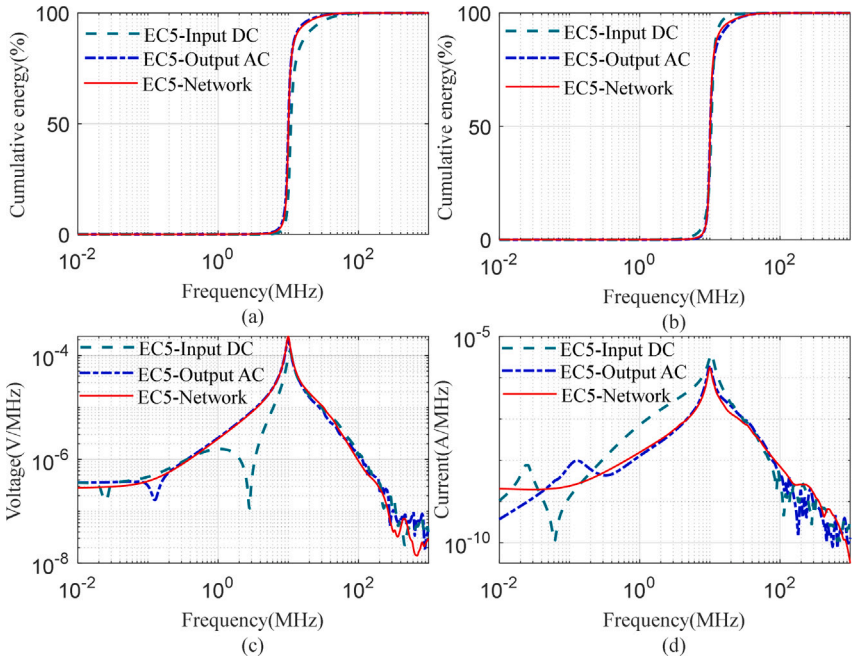

Fig. 11. The cumulative energy and spectrum of EC5 for inverter D_2 (Fronius), (a) and (b) are the cumulative energy of the voltage and current responses, respectively.

Table 5
The rated voltage, current, and the fast transient-burst.

Inverter	Rated parameters		Reference standards
	Voltage	Current	
D_1: VACON	200–690 V	20–129 A	IEC 61800-3: 1 kV/2 kV, 1.2/50 μs [32]
D_2: Fronius	1000 V	18 A	IEC/EN 60947-3: 8 kV, 1000 A for 2 poles

For example, the maximum input DC voltage and current of Fig. 6(c) can reach 1000 V and 18 A, respectively [34]. It is worth noting that the inverter from Fig. 6(b) is a self-made inverter, the immunity requirements have not been tested.

According to standard immunity response listed in Table 5, Figs. 9 and 10, all ports of the inverter D_1 can withstand the voltage under EC5 due to the voltage is always lower than 2 kV. Similarly, the inverter D_2 can tolerate a voltage of 8 kV and a current with 1000 A, indicating that all the ports can survive under EC5.

Basically, all voltages for different ports have exceeded 2 kV, indicating that the ports of the inverter D_1 would be damaged under the EC8 scenario. Additionally, the rise time is lower than 25 ns, which is shorter than the rise time 1.2/50 μs defined in IEC 61800-3. Similarly, for the inverter D_2, although the value voltage and current are within the range of standard, the rise time is less than 10 ns which means that the ports can survive because a lower rise time means a low power as can be seen from Fig. 10(b). Additionally, event through it is challenging to know the tolerable immunity level of inverter D_3, it still clear to see that the power source port can withstand a higher immunity level and the input port can be damaged easily.

Instead, for an immunity level higher than EC8, e.g., the EC10, it has a 25 000 V and 500 A voltage and current levels. Thus, all the inverters would be damaged under such a high scenario.

5.5. Research on protection measures

The aforementioned analysis reveals that a quality voltage and current effect of EMP are carried out. It is obvious that not all the ports can withstand the impact of EMP. For the inverter D_2, the technical details are mainly designed according to IEC 62109-1 [33]. The impulse voltage test is intended to simulate the over-voltages induced by lightning [35]. The voltages can reach 6000 to 8000 V for overvoltage category II. However, the voltage has a 1.2/50 μs waveform which means that the rise time is much higher than the EMP (about 10 ns), indicating that the inverters could be damaged under such a severe scenario.

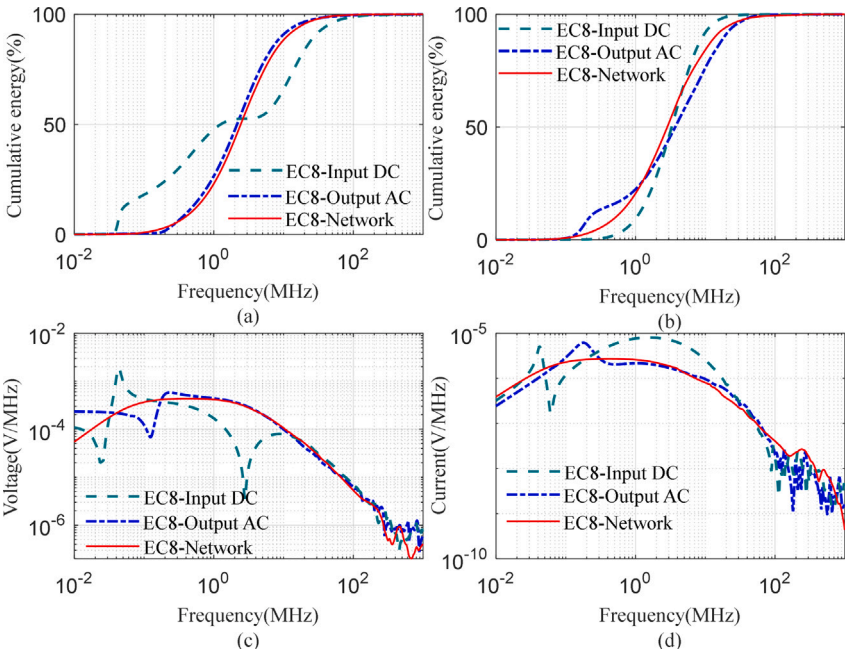

Fig. 12. The cumulative energy and spectrum of EC8 for inverter D_2 (Fronius), (a) and (b) are the cumulative energy of the voltage and current responses, respectively.

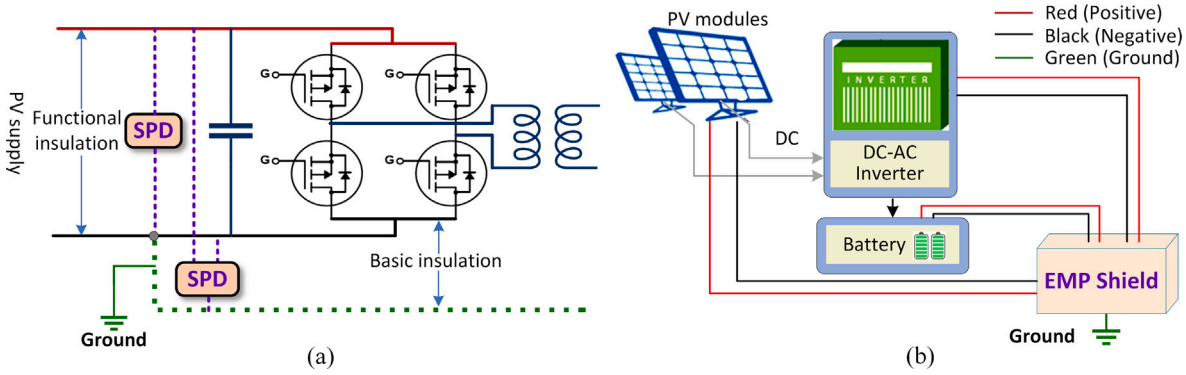

Fig. 13. The induced voltage and current of EC8 for the solar inverter, where the SPD demotes the surge protection device.

For the inverter D_1, it considers the emission of Electromagnetic Compatibility (EMC) based on the standard the EN61800-3 [36] and IEC 61800-5 [37]. However, the voltage of the EMC is usually located in the E2 or even E3 of the EMP, where the E1 of the EMP is much higher than the EMC. This also means that some ports of solar inverters may not survive. Therefore, some necessary measures need to be taken to defend the EMP.

To further investigate the surge protection ability, the IEC 62109-1 recommends the surge protection device to reduce the impulse voltage for functional and basic insulation, as shown in Fig. 13(a).

Shielding and grounding are also suggested practices. EMP shield is the world's only public military tested EMP protection technology [38]. It is usually a metal box used to attenuate electromagnetic fields to protect devices inside. For example, a $5000\text{A}/2\times10^{-8}$(rise)s short pulse for the common mode and a $250\text{A}/1.5\times10^{-6}$(rise)s short pulse for the wire-to-ground could be complied in the EMP shield [39]. Besides, the PV modules and the battery can also be protected by the EMP shield, as shown in Fig. 13(b).

As wires or cables need to be connected with the devices, e.g. inverters, these wires and cables also need shielding. Grounding is then necessary to mitigate the induced conducted overvoltage or current. Grounding resistance, grounding position, and space between grounding points are mainly considered factors [40]. Proper grounding requires small grounding resistance and more grounding points. Short and flat grounding wires should be buried deep underground to reduce resistance and inductance. The space between two adjacent grounding points should be small. And one grounding point should be as close as possible to the protected device.

6. Conclusion

To investigate the effects of EMP on key devices in a PV system, a port vulnerability analysis scheme is proposed. First, the port impedance measurements scheme is tested using three VNAs, with a wide frequency range from 50 Hz to 1.3 GHz and 99.99 MΩ magnitude achievable. The impedance measurement results of different VNAs agree with each other, indicating that an effective measurement scheme has been implemented. Then, a pulsed current injection model is established, and parameter experiments show that a pulse with an extremely short rise time (less than 10 ns) is generated. The port impedance of the common mode and wire-to-ground are compared based on three solar inverters. Under the immunity levels EC5 and EC8, the PCI test results show that the maximum voltage and current under EC5 can reach 1500 V and 40 A, respectively, while EC8 can reach 8000 V and 150 A, respectively, revealing that EC8 can lead to serious vulnerabilities. The port vulnerability analysis results demonstrate that the inverters can be damaged due to higher voltage or lower rise time,

Table 6
Main characteristics of the three tested inverters.

Parameters	Inverters		
	D1: VACON	D2: Fronius	D3: Customized
Input voltage (max)	690 V	1000 V	160 V
Input current (max)	129 A	18 A	120 A
AC output current	208 A	35.7 A	50 A
AC nominal output	22 kW	8200 W	6000 W

and also reveal that EC8 is challenging to defend against due to its wider energy frequency ranging from 0.1 MHz to 100 MHz. Finally, three surge protection measures are discussed, providing insight into the protection of solar inverters and defense against EMP.

CRediT authorship contribution statement

Wei Qiu: Conceptualization, Methodology, Writing – original draft. **Liang Zhang:** Methodology, Writing – original draft. **He Yin:** Visualization, Investigation, Reviewing. **Dahan Liao:** Investigation, Reviewing. **Lawrence C. Markel:** Supervision, Project administration. **Ben W. McConnell:** Resources, Project administration. **Yilu Liu:** Supervision, Reviewing, Funding acquisition, Project administration.

Declaration of competing interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

Data availability

Data will be made available on request.

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Appendix

To present the main characteristics of different inverters, some rated parameters are given below in Table 6. The maximum input voltage and current are presented.

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